



## ADPCM VOICE SYNTHESIZER (ROM-LESS *PowerSpeech II*)

### GENERAL DESCRIPTION

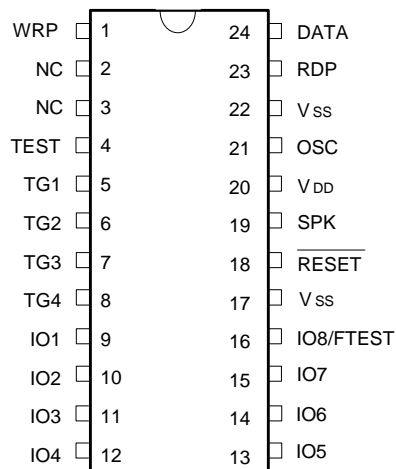
The W52900 is a CMOS IC used solely for the purpose of demonstrating the W529xx series *PowerSpeech II* products.

The W52900 is a 4-bit ADPCM and/or 8-bit PCM ROMless voice synthesizer that provides basic *PowerSpeech* instructions and a number of more powerful commands, including basic ALU operations, data move, branch, and random number generation. When used with a Winbond OTP or flash EPROM, the W52900 allows users to create demonstration devices quickly and easily.

### FEATURES

- ROMless structure, used with Winbond OTP or serial flash EPROM for demonstration
- Powerful programmable speech synthesizer
- Wide operating voltage range: 2.4 to 5.5 volts
- Both 4-bit ADPCM and 8-bit PCM synthesis methods can be used
- Provides 4 trigger pins with separate control of falling/rising edges
- Two trigger input debounce times (160 to 320  $\mu$ S or 20 to 40 mS) can be set
- Eight multiplexed pins can be set as SCAN, FTEST, LED, STOP, or INPUT
- Supports ALU operations, including
  - Branch decisions
  - Logic operations
  - Binary addition/subtraction
  - Data move
  - Bit operand
- Eight general-purpose registers: R0 to R7
- Four special registers: EN, MODEn (n:1, 2), OUTPUT, and ACC
- Maximum 32 matrix keys can be defined by H/W or S/W
- Provides random number generation by H/W
- Section control provided for each GO instruction
  - Variable frequency: 4.8/6/8/12 KHz
  - LED: ON/OFF
- Three LED flash types provided: 3 Hz/Circular/Random
- System clock uses 1.5 MHz frequency
- Total of 256 label entries available for programming
- Packaged in 24-pin skinny DIP

### PIN CONFIGURATION



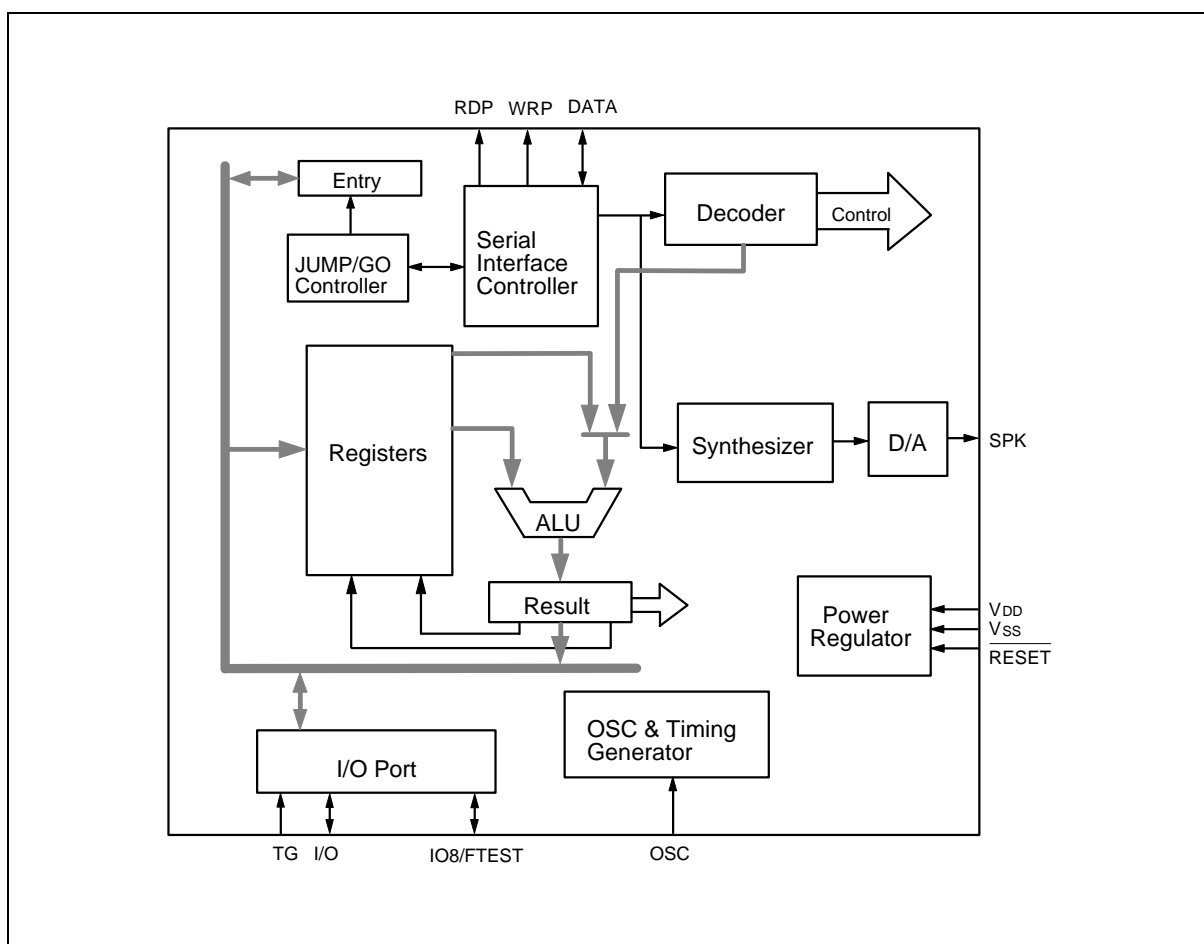
## PIN DESCRIPTION

NO.	NAME	I/O	DESCRIPTION
1	WRP	O	Write clock output pin for serial interface
2	NC	-	Not connected
3	NC	-	Not connected
4	TEST	I	Test pin, internally pulled low
5	TG1	I	Direct trigger input 1, internally pulled high
6	TG2	I	Direct trigger input 2, internally pulled high
7	TG3	I	Direct trigger input 3, internally pulled high
8	TG4	I	Direct trigger input 4, internally pulled high
9	IO1	I/O	SCAN/LED/STOP/INPUT multiplexed pin 1
10	IO2	I/O	SCAN/LED/STOP/INPUT multiplexed pin 2
11	IO3	I/O	SCAN/LED/STOP/INPUT multiplexed pin 3
12	IO4	I/O	SCAN/LED/STOP/INPUT multiplexed pin 4
13	IO5	I/O	SCAN/LED/STOP/INPUT multiplexed pin 5
14	IO6	I/O	SCAN/LED/STOP/INPUT multiplexed pin 6
15	IO7	I/O	SCAN/LED/STOP/INPUT multiplexed pin 7
16	IO8/FTEST	I/O	LED/STOP/INPUT multiplexed pin 8 or frequency test pin



Pin Description, continued

NO.	NAME	I/O	DESCRIPTION
17	VSS	-	Negative power supply
18	RESET	I	Reset; functions as POR; low active
19	SPK	O	Current type output for speaker
20	VDD	-	Positive power supply
21	OSC	I	Oscillator input, connect ROSC to VDD
22	VSS	-	Negative power supply
23	RDP	O	Read clock output pin for serial interface
24	DATA	I/O	Bidirectional data pin for serial interface

**BLOCK DIAGRAM**



## FUNCTIONAL DESCRIPTION

### Trigger Inputs

The W52900 provides four direct trigger input pins that are pulled high internally. All of these trigger inputs can be independently defined to be enabled or disabled by the rising or falling edge. The debounce time of the trigger inputs can be set as 160  $\mu$ S to 320  $\mu$ S or 20 mS to 40 mS.

### SPK Output

This pin is a current-type voice output that is connected to the output of the internal D/A converter. The full-scale output of the 8-bit D/A converter is 5 mA, which is sufficient to drive an external 8  $\Omega$  speaker through the amplification of a low-power NPN transistor with a  $\beta$  of 120 to 160 (an 8050D transistor is usually appropriate).

### I/O Pin

The I/O pins, IO1 to IO8, are multiplexed for four different functions: SCAN/FTEST, LED, STOP, and INPUT. All of these pins can be defined independently as shown in the following table.

GROUP	IO8	IO7	IO6	IO5	IO4	IO3	IO2	IO1
0	INPUT/STOP				INPUT/LED			
1	FTEST/LED	SCAN/LED			SCAN/LED			
2	INPUT/LED				SCAN/STOP			
3	LED/STOP				LED/STOP			

### Oscillator

The oscillator is used to generate the system frequency of around 1.5 MHz. The OSC pin is connected directly to VDD by an ROSC resistor, which is used to provide a bias current for the oscillator.

### RESET

This is an active low reset input with an internal pull-high resistance. If customers turn the W52900 off and then on again without discharging the VDD to ground level, the chip may function abnormally, causing unpredictable operation. Users may reset the W52900 by sending a pulse through the RESET pin to restart the operation from the beginning.

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITIONS	RATED VALUE	UNIT
Power Supply	VDD–VSS	-	-0.3 to +7.0	V
Input Voltage	VIN	All Inputs	VSS -0.3 to VDD +0.3	V
Storage Temp.	TSTG	-	-55 to +150	°C
Operating Temp.	TOPR	-	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

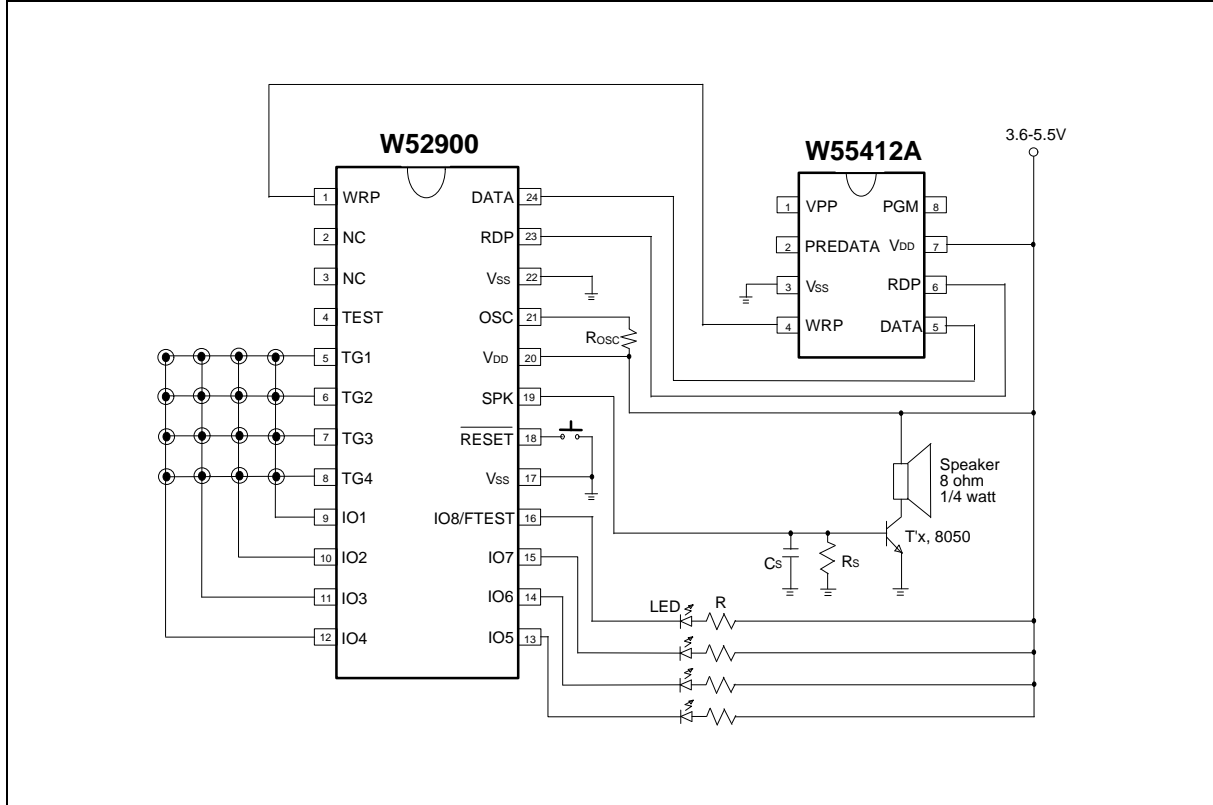
## DC CHARACTERISTICS

(T<sub>A</sub> = 25° C, V<sub>SS</sub> = 0 V)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Operating Voltage	V <sub>DD</sub>	-	2.4	4.5	5.5	V
Input Voltage	V <sub>IL</sub>	All Input Pins	V <sub>SS</sub> -0.3	-	0.3 V <sub>DD</sub>	V
	V <sub>IH</sub>		0.7 V <sub>DD</sub>	-	V <sub>DD</sub>	
Standby Current	I <sub>DD</sub>	V <sub>DD</sub> = 5 V, No Playing	-	-	1	μA
Operating Current	I <sub>OP1</sub>	V <sub>DD</sub> = 3 V, No Load	-	-	400	μA
	I <sub>OP2</sub>	V <sub>DD</sub> = 5 V, No Load	-	-	800	
Input Current for TGn	I <sub>IN</sub>	V <sub>DD</sub> = 3 V, V <sub>IN</sub> = 0 V	-	-	-3	μA
SPK (D/A Full Scale)	I <sub>O</sub>	V <sub>DD</sub> = 4.5 V, R <sub>L</sub> = 100 Ω	-4.0	-5.0	-6.0	mA
Output Current for IOn	I <sub>OL</sub>	V <sub>DD</sub> = 3 V, V <sub>OUT</sub> = 0.4 V	1	-	-	mA
	I <sub>OH</sub>	V <sub>DD</sub> = 3 V, V <sub>OUT</sub> = 2.7 V	-0.5	-	-	
Oscillation Frequency	F <sub>OSC</sub>	R <sub>OSC</sub> = Typ.	1.35	1.5	1.65	MHz
Oscillation Frequency Deviation by Voltage Drop.	$\frac{ \Delta F_{OSC} }{F_{OSC}}$	$\frac{ F(3\text{ V}) - F(2.4\text{ V}) }{F(3\text{ V})}$	0	4	7.5	%
Input Debounce Time	T <sub>DEB1</sub>	F <sub>OSC</sub> = 1.5 MHz	20	30	40	mS
	T <sub>DEB2</sub>		160	240	320	μS

Note: R<sub>osc</sub> = Typ. = 120 KΩ.

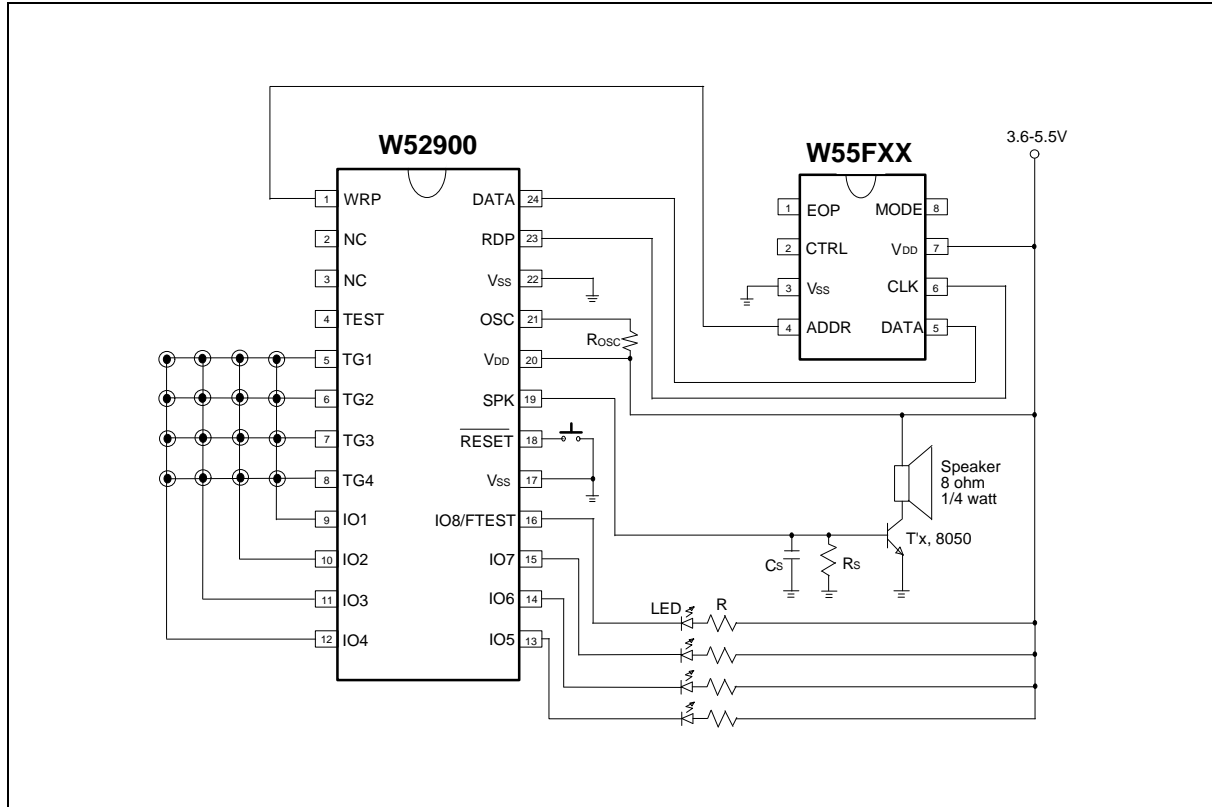
## TYPICAL APPLICATION CIRCUIT\_(I)



### Notes:

1. In principle, the playing speed determined by  $R_{osc}$  should correspond to the sampling rate during the coding phase. The playing speed may be adjusted by varying  $R_{osc}$ , however.
2.  $R_s$  is an optional current-dividing resistor. If  $R_s$  is added, the resistance should be between 470 and 750  $\Omega$ .
3.  $C_s$  is optional.
4. The DC current gain  $\beta$  of transistor 8050 ranges from 120 to 160.
5. All unused trigger pins can be left open because of their internal pull-high resistance.
6.  $R$  is used to limit the current on the LED.
7. Typical  $R_{osc}$  is 120 K $\Omega$ .

## TYPICAL APPLICATION CIRCUIT\_(II)

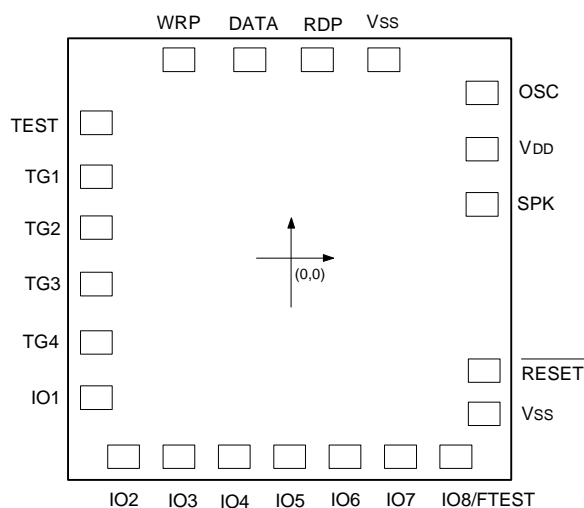


### Notes:

1. In principle, the playing speed determined by R<sub>osc</sub> should correspond to the sampling rate during the coding phase. The playing speed may be adjusted by varying R<sub>osc</sub>, however.
2. R<sub>s</sub> is an optional current-dividing resistor. If R<sub>s</sub> is added, the resistance should be between 470 and 750 Ω.
3. C<sub>s</sub> is optional.
4. The DC current gain β of transistor 8050 ranges from 120 to 160.
5. All unused trigger pins can be left open because of their internal pull-high resistance.
6. R is used to limit the current on the LED.
7. Typical R<sub>osc</sub> is 120 KΩ.



## BONDING PAD DIAGRAM



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Note: All data and specifications are subject to change without notice.