偉詮電子股份有限公司
Weltrend Semiconductor, Inc.

WT6802

Monitor OSD with Auto-calibration

Data Sheet

REV. 1.0

April, 9, 2001

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DESCRIPTION

WT6802 is designed to interface with a MCU to do the OSD (On Screen Display) function in CRT Monitor, besides the fancy auto-calibration function is also included.
The on-chip PLL generates a wide-ranged system clock up to 60MHz to meet the resolution requirements(OSD resolution is programmable) of different display modes. The full OSD screen size is 30 columns x 15 rows, and the OSD position can be freely programmed by setting the interal registers. Special functions include color font, character bordering, shadowing, blinking, double height, double width, all blanking effect, row to row spacing control, 4 windows with shadowing, and programmable fin in/fan out effect.
WT6802 has 8 channels of PWM DAC, each PWM DAC can be respectively controlled by an 8-bit register which contains a 5-bit PWM and 3-bit BRM, and the PWM clock is also programmable.
The horizonal back/front porch and vertical black/front porch data can be read by MCU through the I^2C bus in order to do the horizontal size/center and vertical size/center auto-calibration.

FEATURES

- Input horizontal synchronous frequency …..15k-130kHZ
- Dot Frequency generated by On-chip PLL ….up to 160MHz
- Resolution ….programmable, up to 2040 dots/line
- Screen ……30 columns x 15 rows
- Character ….12(H) x 18(V) dot matrix
  Fonts ……512 characters and 16 color fonts
  MCU interface I^2C bus
- Color(R, G, B with intensity attribute)
  Character foreground 8(R, G, B)
  Character background 7(no blank)
  Window 8(R, G, B)
  Window shadowing 8(R, G, B)
- PWM DAC 8 channels
- Row to row spacing control
- Double character height and width
- Programmable character height control 18-69 lines
- Character blinking, bordering(or shadowing)
- 4 programmable background windows with multi-level operation
- Horizontal/vertical size and center Auto-calibration

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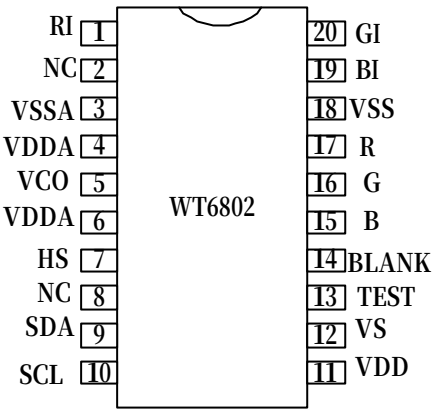
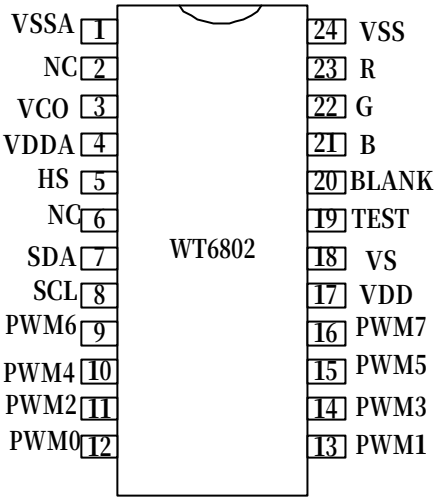
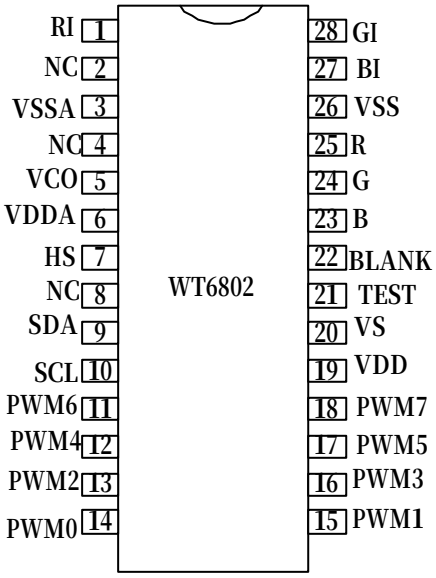
PIN CONFIGURATION



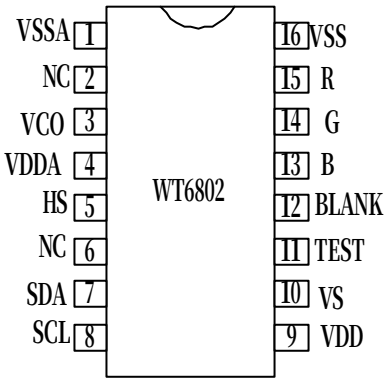
WT6802 (DIP-20)



WT6802 (DIP-24, 300mil)



WT6802 (DIP-28, 300mil)



WT6802 (DIP-16)

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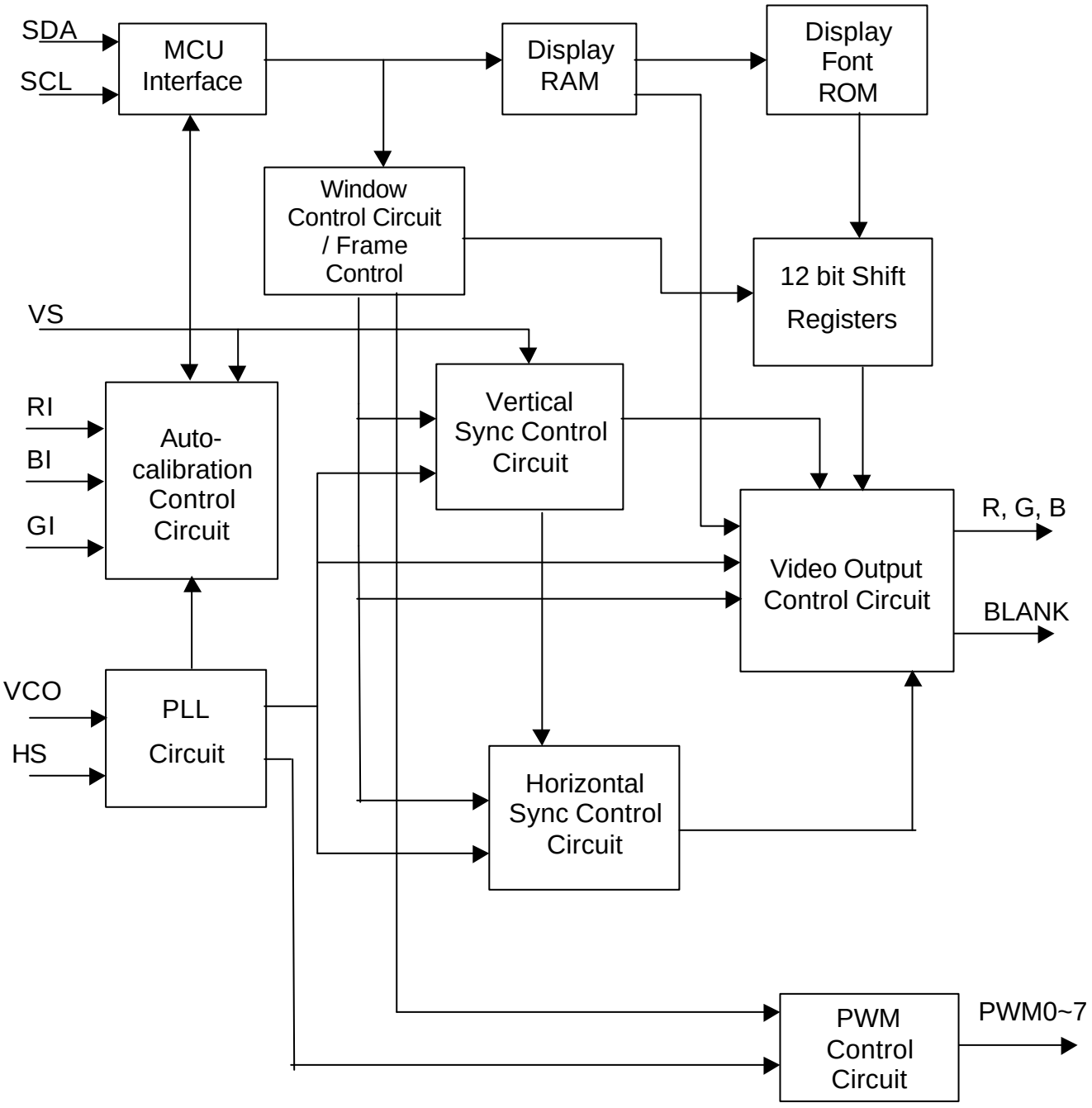
BLOCK DIAGRAM



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PIN DESCRIPTION

PIN No				Symbol	Pin Name	Input/ output	Description
28 pin	24 pin	20 pin	16 pin				
1	--	1	--	RI	Red Input	input	Video Red input from Pre-AMP
2	--	2	--	NC			
3	1	3	1	VSSA	Analog ground	—	
4	2	4	2	NC	No connection	—	
5	3	5	3	VCO	VCO	—	Connected to external loop filter circuit
6	4	6	4	VDDA	Analog power	—	+5 V
7	5	7	5	HS	Horizontal SYNC	Input	Horizontal synchronous input signal
8	6	8	6	NC	No connection	—	
9	7	9	7	SDA	Serial data	Input/output	I^2C data
10	8	10	8	SCL	Serial clock	input	I^2C clock
11~18	9~16	--	--	PWM0~ PWM7	PWM DACs	output	8 channels of 8-bit PWM DAC. Refer to pin assignment in page1 for each PWM DAC's pin assignment.
19	17	11	9	VDD	Digital power	—	+5 V
20	18	12	10	VS	Vertical SYNC	input	Vertical synchronous input signal
21	19	13	11	TEST	TEST	output	Output test only
22	20	14	12	BLANK	Blank	output	Blank signal output

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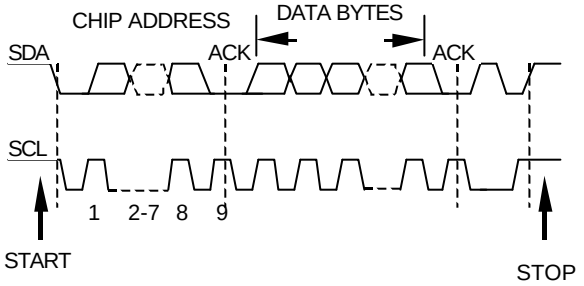
23	21	15	13	B	Blue output	output	Blue signal output
24	22	16	14	G	Green output	output	Green signal output
25	23	17	15	R	Red output	output	Red signal output
26	24	18	16	VSS	Digital Ground		
27	--	19	--	BI	Blue input	input	Video Blue input from Pre-AMP
28	--	20	--	GI	Green input	input	Video Green input from Pre-AMP

MCU INTERFACE



WT6802 uses I^2C to interface with MCU, the Max. data rate is 100 kbps. Default Chip Address byte is as :

A6	A5	A4	A3	A2	A1	A0	Read / Write
0	1	1	1	1	0	1	R= 1 , W= 0

(i.e. 7AH for write, 7BH for read)

The MCU master initiates a transmission by sending a START (SDA goes low first, then SCL goes low), followed by a slave Chip Address byte. Once the address is properly identified, the slave WT6802 will respond with an ACK by pulling SDA to low during the 9th SCL clock. Each data byte which then follows must be 8 bits long with an ACK as the 9th bit. In the case of no ACK or complete of data transmission, the master will send a STOP (SCL goes high first, then SDA goes high).

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DATA TRANSMISSION FORMAT

(1) Data write

To access a specific register in WT6802 , a Row address byte and a Column address byte must be given by MCU to WT6802. There are 3 kinds of data transmission format options to optimize the transmission efficiency, depending on different situations.

(A) R → C → D → R → C → D → ……

(B) R → C → D → C → D → C → ……

(C) R → C → D → D → D → D → ……

R : Row address byte , C : Column address byte , D : Data byte

During a single transmission, it is permissible to change the format from (A) to (B), or from (A) to (C), or from (B) to (A),or from (B) to (C), but not from (C) back to (A) or (B). During a Data bytes updating, it is recommended that format (A) is used for those Data bytes which have different Row and different Column address bytes, format (B) for the same Row but different Column address bytes and format (C) for the same Row address and continuous Column address bytes. Format (C) is the best choice for large area screen pattern updating, these Data bytes will be written with Column address bytes automatically increased for each Data byte updating. During the format (C) transmission, a dummy Data byte should be inserted in Data byte train if Column address reaches one of those undefined registers in WT6802.

To differentiate the Row address byte of Character Display Register from the Row address byte of Character Attribute register, the most significant 3 bits are set to“ 100“ to represent the Character Display Row address byte, and“ 101” for Character Attribute ROW address byte.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Format
(Character Display, Window Reg) Row address byte	1	0	0	X	AD	AD	AD	AD	A,B,C
(Character/ Row Attribute, Control, Auto-calibration Reg) Row address byte	1	0	1	X	AD	AD	AD	AD	A,B,C
Column address byte	0	0	X	AD	AD	AD	AD	AD	A,B
Column address byte	0	1	X	AD	AD	AD	AD	AD	C

X : Don’t Care AD : Address of register

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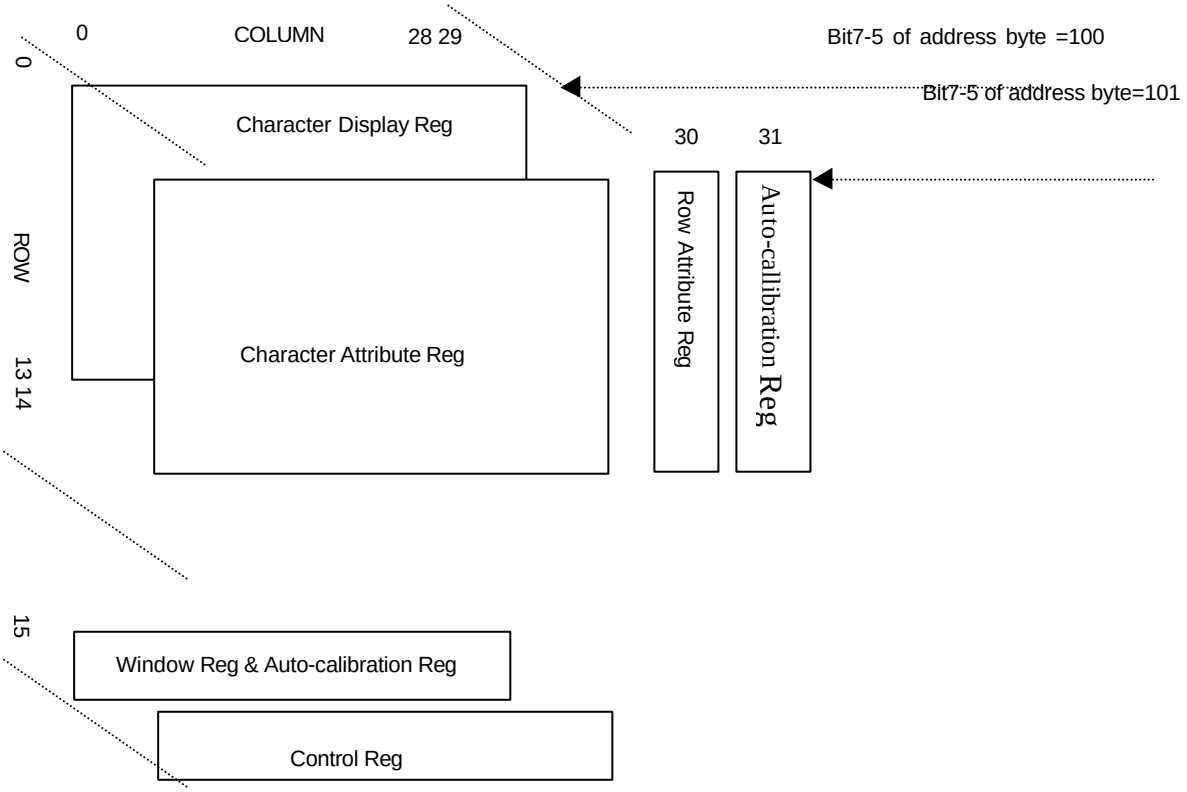
(2) Data read

The data read fomat is written for the right row and column address and then follows the IIC read format.

S	01111010	A	ROW	A	COL	A	S	01111011	A	Data	A	……	P

S: Start A: ACK ROW: Row address COL: column address P: Stop



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REGISTER DESCRIPTION

(1)Character Display Registers ROW m (m=0~14) ; COLN n (n=0~29)

Bit	Symbol	Description
0~7	CRAD0 ~ CRAD7	These 8 bits,CRAD7~CRAD0, select 1 character/symbol to be displayed on OSD screen from the 512 characters/ symbols in the ROM fonts.

Note: For all the Character Display Registers (described in (1) above) and the Window Registers (described in (4) below) and the auto calibration registers (described in (6)), the most significant 3 bits of their Row address bytes must be set to "100" during the data transmission between MCU and WT6802. But for all the other registers (Character Attribute Registers Row Attribute Registers and Control Registers), the Row address bytes must be set to "101".

(2)Character Attribute Registers ROW m (m=0~14) ; COLN n (n=0~29)

Bit	Symbol	Description
0	B	R,G,B defines the foreground color of the corresponding character/ symbol selected by Character Display Register. Refer to Table 1
1	G	
2	R	
3	BLINK	If BLINK=1, the corresponding character/ symbol selected by Character Display Registers will blink. The blinking frequency is the frequency of VS divided by 64 and the duty cycle is 50%.
4	BB	BR, BG, BB defines the background color of the corresponding character selected by the Character Display Registers, but, if BR, BG, BB =(0, 0, 0), there is no background (ie transparent) for this character/ symbol. Refer to Table 1.
5	BG	
6	BR	Not used

R	G	B	Foreground	Background	Window	Border and shadow	Color font(F0H-FFH)
0	0	0	Black	TRANSPARENT	Black	Black	TRANSPARENT
0	0	1	Blue	Blue	Blue	Blue	Blue
0	1	0	Green	Green	Green	Green	Green
0	1	1	Cyan	Cyan	Cyan	Cyan	Cyan
1	0	0	Red	Red	Red	Red	Red
1	0	1	Magenta	Magenta	Magenta	Magenta	Magenta
1	1	0	Yellow	Yellow	Yellow	Yellow	Yellow
1	1	1	White	white	white	white	white

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Table 1 color for character foreground, character background, window, border/shadow and color font

(3)Row Attribute Registers ROW m (m=0~14) ; COLN 30

Bit	Symbol	Description
0	DWm	Double Width control for ROWm (m=0~14). If DWm=1, the widths of the even column characters in ROWm will be doubled and the odd column characters will not be displayed.
1	DHm	Double Height control for ROWm (m=0~14). If DHm=1, the heights of all the characters in ROWm will be doubled.
2 ~ 7		Not used

:

(4) Window Registers

Window1 Registers ROW 15 ; COLN n (n=0~2)
Window2 Registers ROW 15 ; COLN n (n=3~5)
Window3 Registers ROW 15 ; COLN n (n=6~8)
Window4 Registers ROW 15 ; COLN n (n=9~11)
Other window registers ROW 15 ; COLN 12~15

Note: There are 4 windows Max. can be set up, the controls of these windows are similar, take Window1 as an example:

Window1 Registers:

ROW 15 ; COLN 0

Bit	Symbol	Description
0~3	WREND0 ~ WREND3	WREND3~0 defines the row end address of Window1
4~7	WRSTART0~ WRSTART3	WRSTART3~0 defines the row start address of Window1

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ROW 15 ; COLN 1

Bit	Symbol	Description
0	WSHD	If WSHD=1, black-edge shadowing of Window1 will be enabled
1		Not used
2	WENB	If WENB=1, Window1 will be enabled. If WENB=0, Window1 is disabled, and all the characters in this window will not be displayed
3~7	WCSTART0~ WCSTART4	WCSTART4~0 defines the column start address of window1

ROW 15 ; COLN 2

Bit	Symbol	Description
0	WB	WR, WG, WB defines the Window1 color. Refer to Table 1. The Window1 color will offer the background color(if Window1 is enabled) for those characters which background color settings are transparent and are included in the Window1 area.
1	WG	
2	WR	
3 ~ 7	WCEND0 ~ WCEND4	WCEND4~0 defines the column end address of Window1

Note: There are 4 windows can be used. If window over-lapping happens, the higher priority window will cover the lower one. Window1 has the highest priority and Window4 the least.

Other window Registers :

ROW 15 ; COLN 12 (window shadow height setting)

Bit	Symbol	Description
0	WSH10	Defines the window shadow height of Window1. Refer to table 3.
1	WSH11	
2	WSH20	Defines the window shadow height of Window2. Refer to table 3.
3	WSH21	
4	WSH30	Defines the window shadow height of Window3. Refer to table 3.
5	WSH31	
6	WSH40	Defines the window shadow height of Window4. Refer to table 3.
7	WSH41	

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ROW 15 ; COLN 13 (Window shadow width setting)

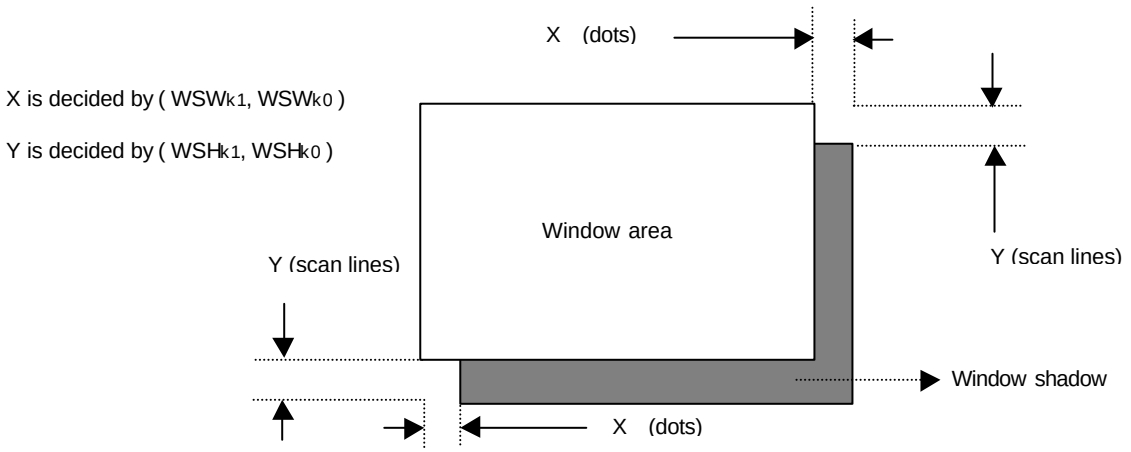
Bit	Symbol	Description
0	WSW10	Defines the window shadow width of Window1. Refer to table 2.
1	WSW11	
2	WSW20	Defines the window shadow width of Wndow2. Refer to table 2.
3	WSW21	
4	WSW30	Defines the window shadow width of Window3. Refer to table 2.
5	WSW31	
6	WSW40	Defines the window shadow width of Wndow4. Refer to table 2.
7	WSW41	

WSWk1	WSWk0	Shadow width(dots)
0	0	2
0	1	4
1	0	6
1	1	8

Table 2 k=1~4 for window1-window4

WSHk1	WSHk0	Shadow height(scan lines)
0	0	2
0	1	4
1	0	6
1	1	8

Table 3 K=1~4 for window1-window4



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ROW 15 ; COLN 14 (window shadowing color setting)

Bit	Symbol	Description
0~2	WSC1(B, G,R)	Defines the window shadowing color of Window1. Refer to Table 1.
3		Not used
4~6	WSC2(B, G,R)	Defines the window shadowing color of Window2. Refer to Table 1.
7		Not used

ROW 15 ; COLN 15 (window shadowing color setting)

Bit	Symbol	Description
0~2	WSC3(B, G,R)	Defines the window shadowing color of Window3. Refer to Table 1.
3		Not used
4~6	WSC4(B, G,R)	Defines the window shadowing color of Window4. Refer to Table 1.
7		Not used

(5) Control Registers

ROW 15 ; COLN 0

Bit	Symbol	Description
0~2	FB1	We divide 512 fonts into 8 font banks. FB1 and FB2 determine font bank.
3~5	FB2	
6	DIV1	DIV1, DIV0 determines the PWM clock. The PWM clock = Dotc / 1 if (DIV0, DIV1) = (0, 0) , where Dotc is the dot frequency from internal PLL Dotc / 2 if (DIV0, DIV1) = (0, 1) Dotc / 4 if (DIV0, DIV1) = (1, 0) Dotc / 8 if (DIV0, DIV1) = (1, 1)
7	DIV0	

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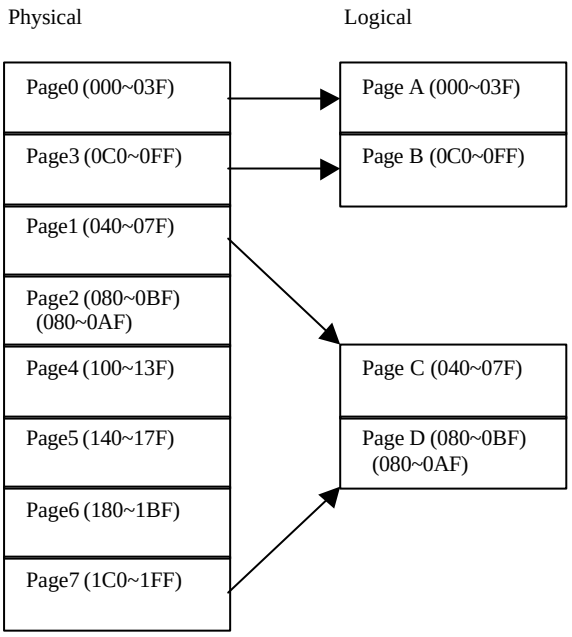

Physical page vs. Logical page

Note:Page C and Page D can be chosed from Page1, Page2, Page4, Page5, Page6, Page7. Use FB1 to decide which page is assigned to Page C,and use FB2 to decide which page is assigned to Page D. For example, if the value of FB1 is ‘ b010 then Page C is assigned to Page2. If the value of FB2 is ‘ b110 then Page D is assigned to Page6.

Table 4. Font bank selector

ROW 15 ; COLN 1 (OSD resolution setting)

Bit	Symbol	Description
0~7	DOTN0~ DOTN7	If DR=0,OSD resolution = DOTN X 4 , if DR =1 ,OSD resolution = DOTN X 8 where DOTN = (DOTN7 ...DOTN0$_2$)

ROW 15 ; COLN 2 (Horizontal start position)

Bit	Symbol	Description
0~7	HP0~H P7	The OSD horizontal start position = HP X 6 dots , counting from the trailing edge of HS pin signal. Where HP = (HP7 .... HP0$_2$) (HP7 .... HP0$_2$) = (00..0) is not allowed.

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ROW 15 ; COLN 3 (Vertical start position setting)

Bit	Symbol	Description
0~7	V0~VP7	The OSD vertical start position = VP X 4 + 1 scan lines , counting from the leading edge of VS pin signal . Where VP = (VP7 .... $VP0_2$) (VP7 .... $VP0_2$) = (00..0) is not allowed.

ROW 15 ; COLN 4 (Character height & Dot frequency range setting)

Bit	Symbol	Description
0~5	CH0~CH5	The character height can be expanded from the 12 X 18 font matrix by setting CH5~CH0. The display character height = CH + ADJ scan lines , (i.e. Character height range is 18 to 69 scan lines) Where CH=(CH5 …$CH0_2$) CH should be 16 (default) at least. ADJ= 2 if 16 ≦ CH < 32 4 if 32 ≦ CH < 48 6 if 48 ≦ CH < 64
6	LF	(HF, LF) determines the frequency range of Dotc, dot frequency from the PLL, (HF, LF) = (1,1) 100 MHz < Dotc ≦ 160MHz (HF, LF) = (1,0) 50 MHz < Dotc ≦ 100 MHz (HF, LF) = (0,0) 25 MHz < Dotc ≦ 50 MHz (HF, LF) = (0,1) 12.5 MHz ≦ Dotc < 25 MHz Note: If Disable CMODE : DR=0, Dotc = DOTN X 4 X (Frequency of HS) , DR =1 , Dotc = DOTN X 8 X (Frequency of HS) If enable CMODE: DR=0, Dotc = (DOTN X 4) X (HTOTAL / HPERIOD) X (Frequency of HS) DR=1, Dotc = (DOTN X 8) X (HTOTAL / HPERIOD) X (Frequency of HS) The default value of (HF, LF) is (0, 0).

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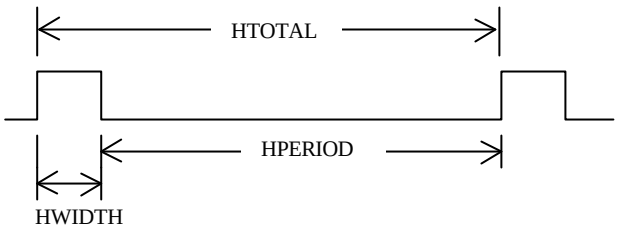
7	HF	

Note: The character height is the result of : multi-scan lines plus repeat lines
(CH5, CH4) determines the multi-scan lines (duplicating the **all** the scan lines originated from the 12 X **18** font matrix) as :

Single-scan lines (18 scan lines) if (CH5, CH4) = 01

Double-scan lines (36 scan lines) if (CH5, CH4) = 10

Triple-scan lines (54 scan lines) if (CH5, CH4) = 11

(CH3 ~ CH0) determines the repeat lines (repeating the scan lines, ranging from 0 to 15 lines, originated from the 12 X **18** font matrix) as :

	REPEAT LINES																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CH0=1	-	-	-	-	-	-	-	-	-	V	-	-	-	-	-	-	-	-
CH1=1	-	-	-	-	-	V	-	-	-	-	-	-	-	V	-	-	-	-
CH2=1	-	-	-	V	-	-	-	V	-	-	-	V	-	-	-	V	-	-
CH3=1	-	-	V	-	V	-	V	-	V	-	V	-	V	-	V	-	V	-

Table 4. Repeat lines

ROW 15 ; COLN 5 (Miscellaneous setting)

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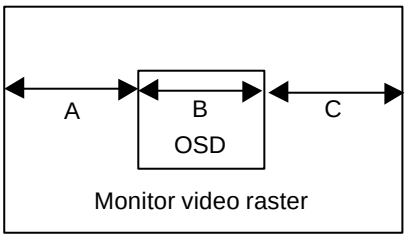
Bit	Symbol	Description
0	BLANKC	If BLANKC=0 , BLANK pin will be high during displaying character foreground and window. If BLANKC=1 , BLANK pin will be high only during displaying character foreground .
1	FAN	If FAN=1 , fan in (/ fan out) effect is enabled while the OSD is turned on (/ off) by setting OSDEN=1 (/ 0)
2	DIV	If DIV=0, the fan in/ fan out speed will be high speed than DIV=1
3	CLR	Setting CLR=1 will clear all the Character Display Registers and Character Attribute Registers
4	CMODE	Setting CMODE=1 will refresh the horizontal synchronous pulse width and keep the ratio of A : B : C (refer to the figure below) same as the last display mode. After this action, CMODE will return to 0 automatically. CMODE setting can (option) be used when a new display mode is coming and want to keep fixed A : B : C ratio.
5	SHDW	If SHDW=1, black-edged shadow is selected when BSEN=1 If SHDW=0, black-edged border is selected when BSEN=1
6	BSEN	If BSEN=1, enable character bordering (or shadowing depending on SHDW)
7	OSDEN	If OSDEN=1 , enable OSD circuit.



ROW 15 ; COLN 6 (Miscellaneous setting)

Bit	Symbol	Description
0	VSPO	If the polarity of VS pin input signal is negative, set VSPO to 0 (default), and set to 1 for positive VS.
1	HSPO	If the polarity of HS pin input signal is negative, set HSPO to 0 (default), and set to 1 for positive HS.
2	TRI	If TRI=1, then R, G, B, BLANK output pins will be Low when OSDEN=0 (OSD disabled) If TRI=0, then R, G, B, BLANK output pins will be in high impedance state when OSDEN=0 (OSD disabled)
3~7	SP0~SP4	SP4~SP0 defines the row to row space in unit of horizontal scan lines.

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Note: After setting TRI bit, R, G, B and BLANK output pins will be change status when you enable OSD.

ROW 15 ; COLN 7

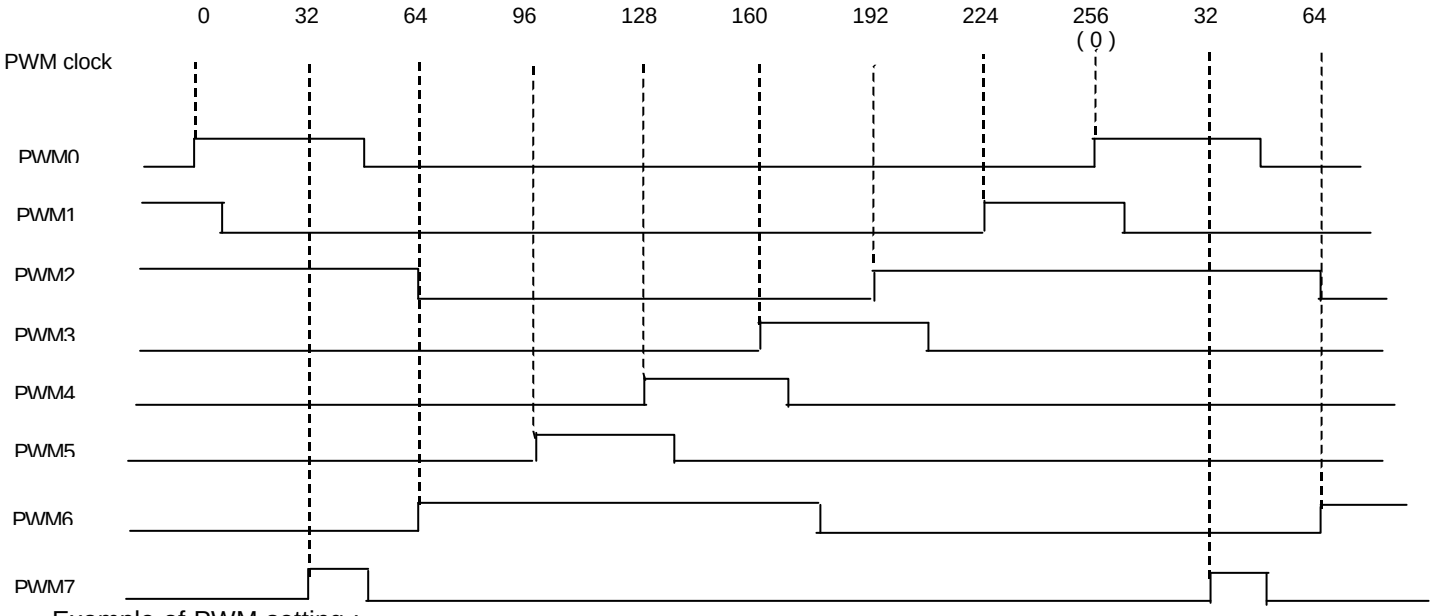
Bit	Symbol	Description
0~2		Must set "0"
3	SREST	Set to 1 for software reset, then set to 0 for normal operation
4~7		Must set "0"

ROW 15 COLN 8~15 (PWM Control Registers; PWMn, n=0~7, output pin control respectively)

Bit	Symbol	Description
0-2	BRM0~BRM2	(BRM2...BRM0) controls the pulse inserted position.
3~7	PW0~PW4	(PW4 ..$PW0_2$) controls the duty cycle of PWMn output pin (n=0~7), refer to the following figure for details.

Example of PWM0~PWM7 setting :

The figure below shows the waveforms when PWM Register setting of PWM0 ~PWM7 is 30H, 28H, 80H, 30H, 28H, 28H, 70H, 10H respectively.



Example of PWM setting :

The figure below shows the waveforms when 5-bit PWM Register is setting to ' b01100 and 3-bit BRM is setting to ' b011. The pulse insertion algorithm is also show in the figure.

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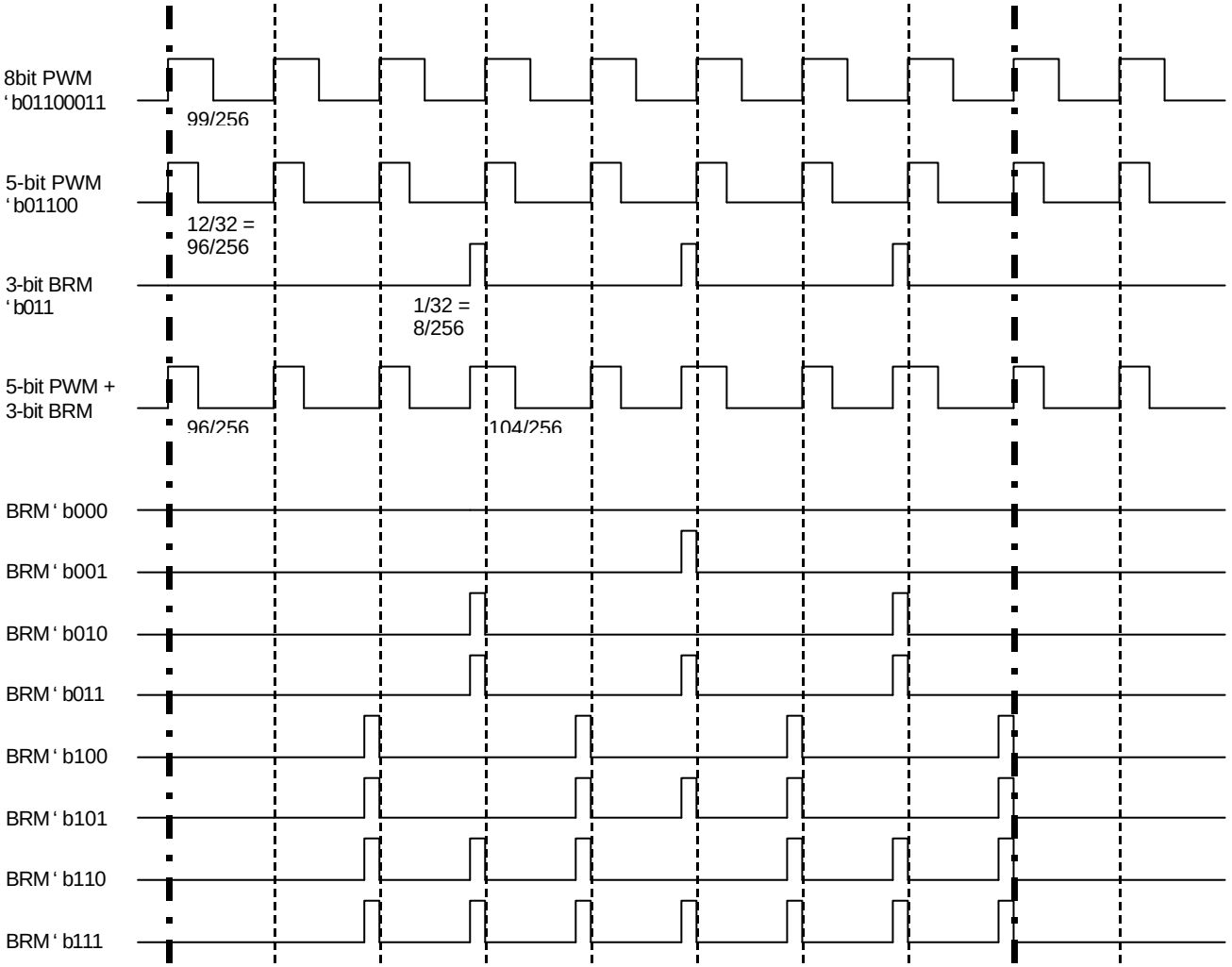

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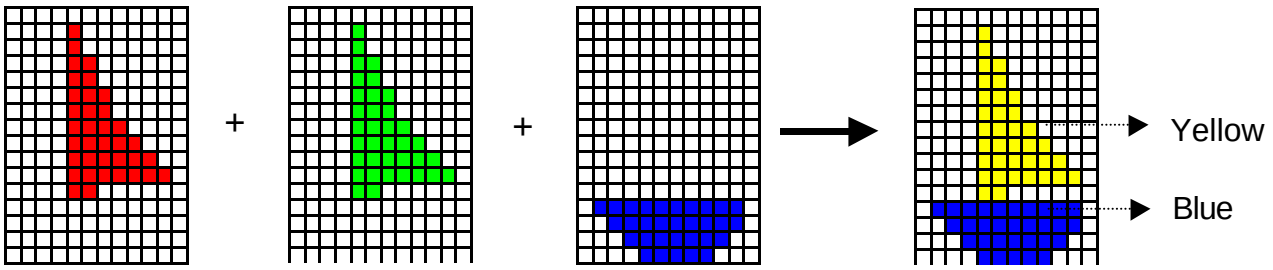
ROW 15 ; COLN 16 (Miscellaneous setting)

Bit	Symbol	Description
0	BSB	BSR, BSG, BSB defines the border and shadow color. Refer to Table 1.
1	BSG	
2	BSR	
3		Not used
4	CFONT	Color font selected at address F0H to FFH if CFONT=1, otherwise mono-color selected at address F0H to FFH
5		Not used
6	CMODE EN	Set to 0 for enable CMODE function, set to 1 for disable CMODE function
7	DR	Double OSD resolution enabled if DR=1

COLOR FONT

There are total 512 fonts can be used in WT6802, address 00H should be left blank –and white,Font address from F0 to FFH are used for color fonts, each color font is made up of 3 different R, G, B fonts which should be defined during the font design stage. Refer to table 1 for the relation between color font and R, G, B fonts



(6) Auto-calibration Registers

Auto-calibration registers are read-only registers except Refresh register. MCU can read the data in these registers through I²C bus (ID : 7BH) to do the horizontal / vertical size, center auto-calibration by S/W algorithm. The RESET bit in Refresh register is used to refresh these Auto-calibration registers in order that the MCU can do the Auto-calibration according to the new coming display mode. The clock used by auto-calibration circuit is synchronous with Dotc, dot frequency from the internal PLL. This Auto-calibration clock will be started only after the RESET bit is set to 1. And in order to get the stable and refreshed data, it is recommended that MCU should wait for at least 2 vertical synchronous signal time after RESET bit set to 1 before it reads these Auto-

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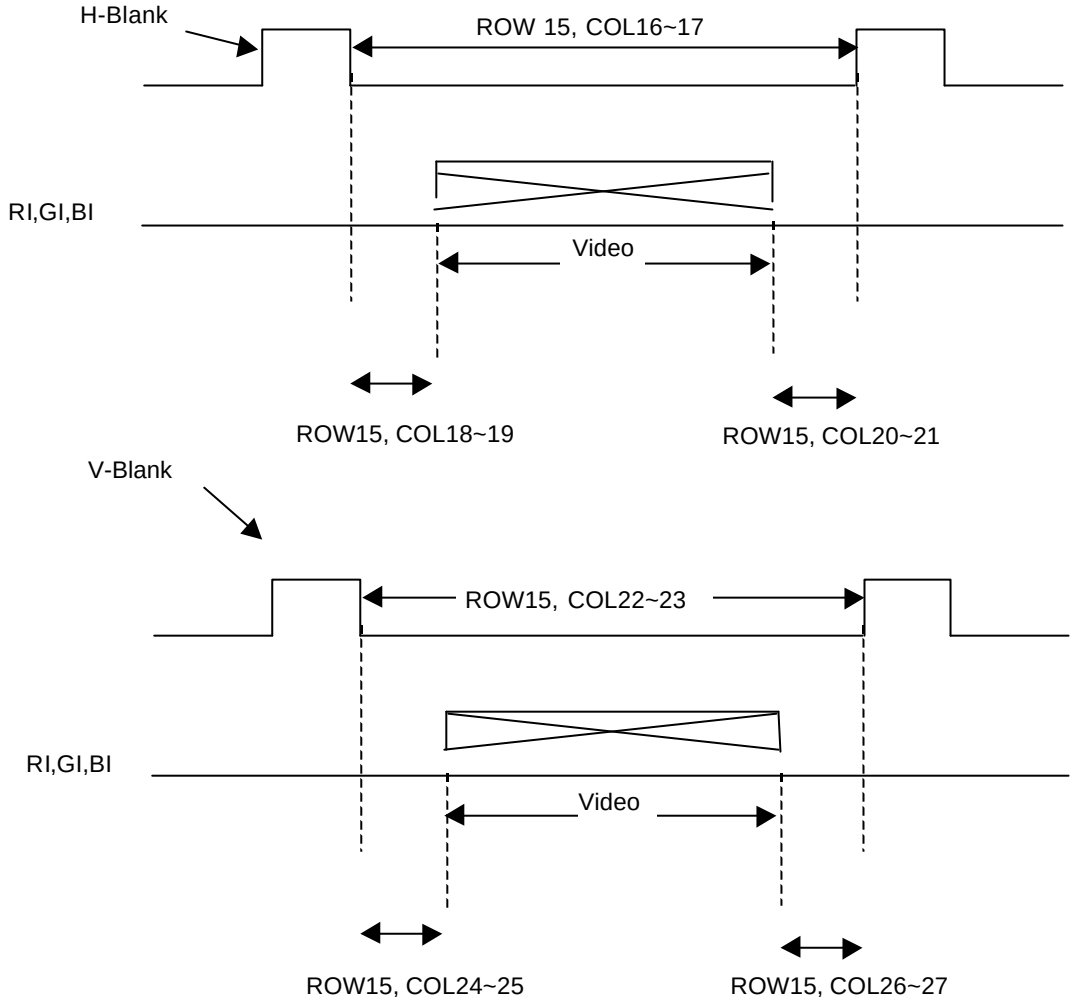
calibration registers.



ROW 15 ; COLN 16

Bit	R/W	Description
0~7	R	Horizontal Active low byte

ROW 15 ; COLN 17)

Bit	R/W	Description
0~2	R	Horizontal Active high byte
3~7		Not used

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ROW 15 ; COLN 18

Bit	R/W	Description
0~7	R	Horizontal Back Porch low byte

ROW 15 : COLN 19

Bit	R/W	Description
0~2	R	Horizontal Back Porch high byte
3~7		Not used

ROW 15 ; COLN 20

Bit	R/W	Description
0~7	R	Horizontal Front porch low byte

ROW 15 ; COLN 21

Bit	R/W	Description
0~2	R	Horizontal Front porch high byte
3~7		Not used

ROW 15 ; COLN 22

Bit	R/W	Description
0~7	R	Vertical Active low byte

ROW 15 ; COLN 23

Bit	R/W	Description
0~2	R	Vertical Active high byte
3~7		Not used

ROW 15 ; COLN 24

Bit	R/W	Description
0~7	R	Vertical Back Porch low byte

ROW 15 ; COLN 25

Bit	R/W	Description
0~2	R	Vertical Back Porch high byte
3~7		Not used

ROW 15 ; COLN 26

Bit	R/W	Description
0~7	R	Vertical Front Porch low byte

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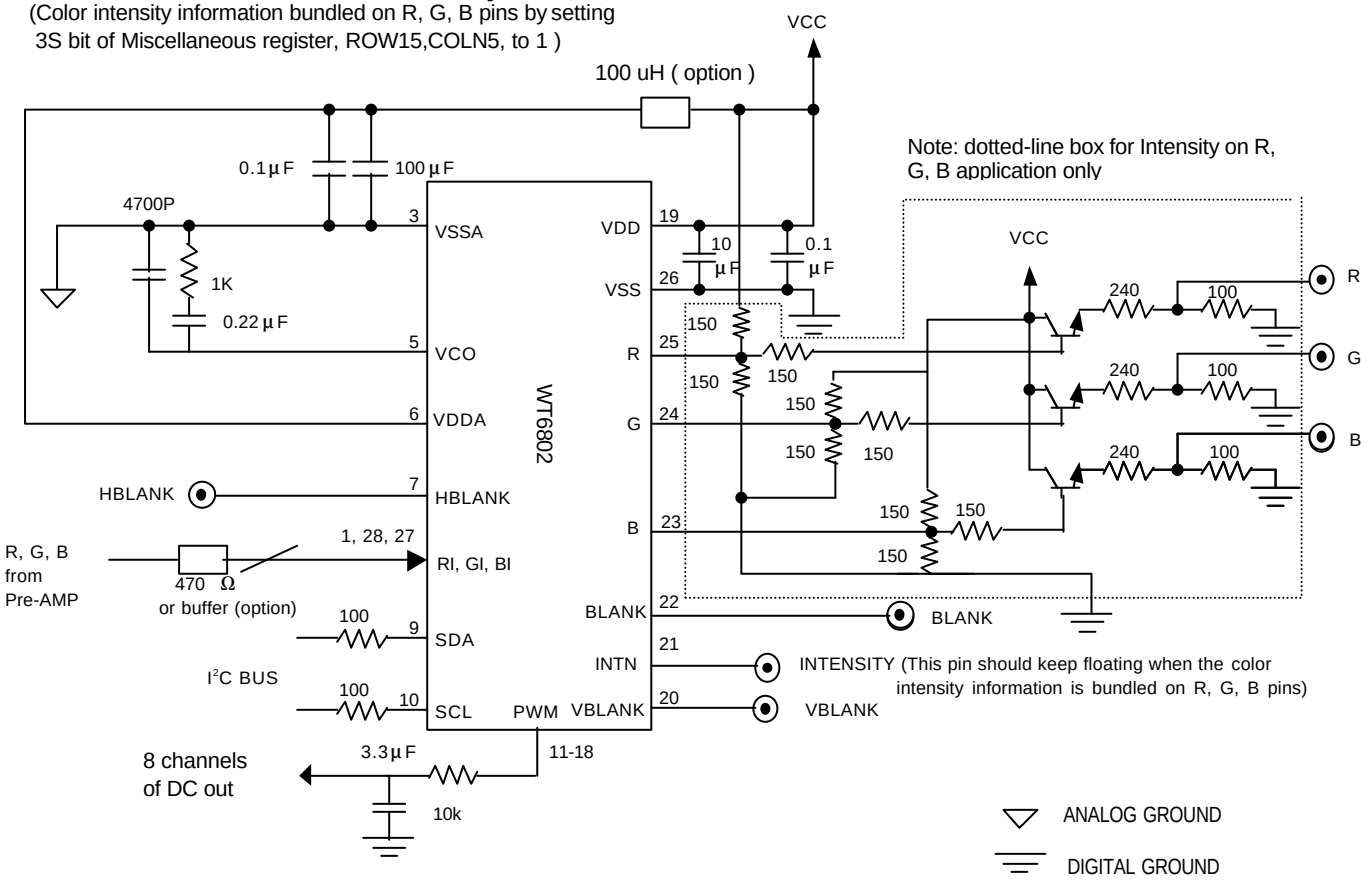
ROW 15 ; COLN 27

Bit	R/W	Description
0~2	R	Vertical Front Porch high byte
3~7		Not used

ROW 15 ; COLN 28 (Refresh register)

Bit	Symbol	Description
0	RESET	Setting RESET to 1 will put the default values to all the Auto-calibration registers (RESET bit is also cleared to 0) and then refresh all the these registers according to the coming display mode.
1~7		Not used

APPLICATION DIAGRAM for Intensity on R, G, B
(Color intensity information bundled on R, G, B pins by setting 3S bit of Miscellaneous register, ROW15,COLN5, to 1)



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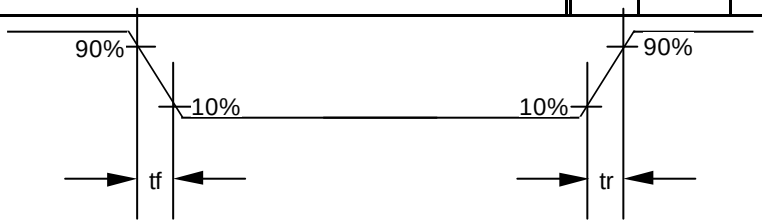
ABSOLUTE MAXIMUM RATINGS (Voltage Referenced to VSS)

Symbol	Characteristic	Value	Unit
VDD	Supply Voltage	-0.3 to + 7.0	V
V_{in}	Input Voltage	VSS - 0.3 to VDD + 0.3	V
Id	Current Drain per Pin Excluding VDD and VSS	25	mA
Ta	Operating Temperature Range	0 to 70	℃
V_{stg}	Storage Temperature Range	-40 to +125	℃

AC ELECTRICAL CHARACTERISTICS (VDD , VDDA = 5.0 V, VSS , VSSA = 0 V, T_A = 25C , Voltage Referenced to VSS)

Symbol	Characteristic	Min	Typ	Max	Unit
t_r t_f	Output Signal (R, G, B, BLANK and INTN), C_{load} = 30 pF Rise Time, Fall Time	— —	— —	6 6	ns ns
t_r t_f	Output Signal (PWM0 – PWM7), C_{load} = 30 pF Rise Time, Fall Time	— —	— —	20 20	ns ns
F_{HS}	HS Input Frequency	15K	—	130K	Hz



Switching Characteristics

DC CHARACTERISTICS (VDD , VDDA = 5.0 V±10%, VSS , VSSA = 0 V, T_A = 25℃, Voltage Referenced to V_{SS})

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage I_{out} = -5mA	V_{DD} –0.8	—	—	V
V_{OL}	Low Level Output Voltage I_{out} = 5mA	—	—	V_{SS} +0.4	V
	Digital Input Voltage (Not Including SDA and SCL)				
V_{IL}	Logic Low	—	—	0.3 V_{DD}	V
V_{IH}	Logic High	0.7 V_{DD}	—	—	V
	Input Voltage of Pin SDA and SCL				
V_{IL}	Logic Low	—	—	0.3 V_{DD}	V
V_{IH}	Logic High	0.7 V_{DD}	—	—	V
I_{II}	High-Z Leakage Current (R, G, B and BLANK)	-10	—	+10	µA
I_{II}	Input Current (Not Including VCO, R, G, B, BLANK and INTN)	-10	—	+10	µA
I_{DD}	Supply Current (NO Load on Any Output) at VDD = 5.0V	—	—	+26	mA