Low Noise/Low Power
Advanced Information

X9428

XDCP™ Digitally Controlled Potentiometer

FEATURES

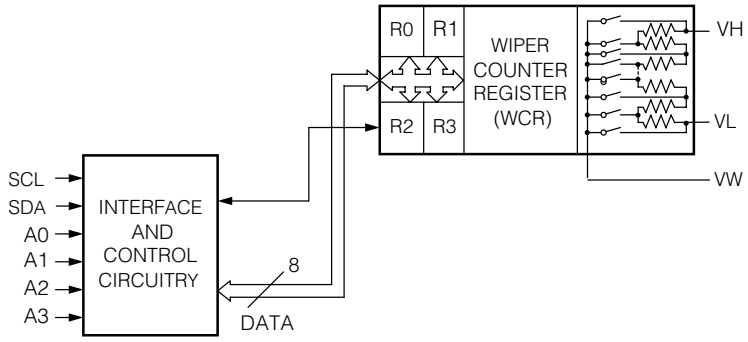
- **Two-Wire Serial Interface**
- **Hardware Write Protection, $\overline{WP}$**
- **Register Oriented Format**
  - **—Directly Read/Write Wiper Position**
  - **—Store as Many as Four Positions**
- **Power Supplies**
  - **—VCC = 2.7V to 5.5V**
  - **—V+ = 2.7V to 5.5V**
  - **—V– = –2.7V to –5.5V**
- **Direct Write Cell**
  - **—Endurance - 100,000 Data Changes per Register**
  - **—Register Data Retention - 100 years**
- **16 Bytes of E^2PROM memory**
- **3 Resistor Array Values**
  - **—2K Ohms to 50K Ohms Mask Programmable**
- **Resolution: 64 Taps each Pot**
- **24-Pin Plastic DIP, 24-Lead TSSOP and 24-Lead SOIC Packages**
- **Low Power CMOS**
  - **—Standby Current < 1µA**

DESCRIPTION

The X9428 nonvolatile XDCP, digitally controlled potentiometer contains a resistor array, composed of 63 resistive elements. Between each element and at either end are tap points accessible to the wiper elements. The position of the wiper element on the array is controlled by the user through the two wire serial bus interface.

The resistor array has associated with it a nonvolatile control latch and four 6 bit data registers that can be directly written and read by the user. The contents of the control latch controls the position of the resistor array/wiper.

FUNCTIONAL DIAGRAM



PIN DESCRIPTIONS

Host Interface Pins

Serial Clock (SCL)

The SCL input is used to clock data into and out of the X9428.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the guidelines for calculating typical values on the bus pull-up resistors graph.

Device Address (A_0–A_3)

The Address inputs are used to set the least significant 4 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the Address input in order to initiate communication with the X9428. A maximum of 16 devices may occupy the 2-wire serial bus.

Potentiometer Pins

V_H (V_{H0} – V_{H1}), V_L (V_{L0} – V_{L1})

The VH and VL inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

V_W (V_{W0} – V_{W1})

The wiper outputs are equivalent to the wiper output of a mechanical potentiometer and the non-inverting input of the voltage follower.

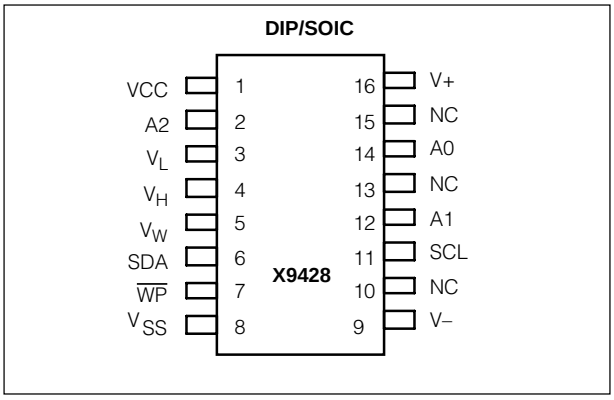
Hardware Write Protect Input $\overline{WP}$

The $\overline{WP}$ pin when low prevents nonvolatile writes to the wiper and voltage follower control latchs.

Analog Supply V+, V-

The Analog Supply V+, V- are the supply voltages for the XDCP analog section.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
SCL	Serial Clock
SDA	Serial Data
A0-A2	Device Address
V_H, V_L	Potentiometers (terminal equivalent)
V_W	Potentiometers (Wiper equivalent)
$\overline{WP}$	Hardware Write Protection
V+,V-	Analog and Voltage Follower Supplys
VCC	System Supply Voltage
Vss	System Ground
NC	No Connection

PRINCIPLES OF OPERATION

The X9428 is a highly integrated microcircuit incorporating a resistor array and associated registers and counters and the serial interface logic providing direct communication between the host and XDCP.

Serial Interface

The X9428 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9428 will be considered a slave device in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW periods (t_{LOW}). SDA state changes during SCL HIGH are reserved for indicating start and stop conditions.

Start Condition

All commands to the X9428 are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH (t_{HIGH}). The X9428 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met.

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA while SCL is HIGH.

Acknowledge

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting eight bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the eight bits of data.

The X9428 will respond with an acknowledge after recognition of a start condition and its slave address and once again after successful receipt of the command byte. If the command is followed by a data byte the X9428 will respond with a final acknowledge.

Array Description

The X9428 is comprised a resistor array containing 63 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (V_H and V_L inputs).

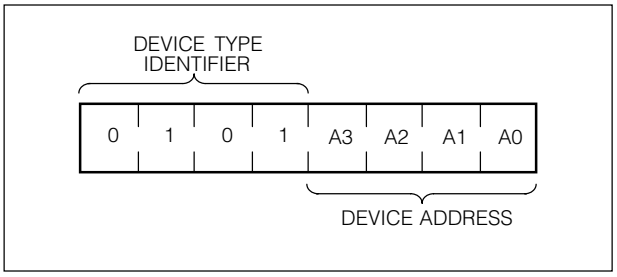
At both ends of the array and between each resistor segment is a CMOS switch connected to the wiper (V_W) output. Within the array only one switch may be turned on at a time. These switches are controlled by a nonvolatile control latch (NCL). The six bits of the NCL are decoded to select, and enable, one of sixty-four switches.

The NCL may be written directly, or it can be changed by transferring the contents of one of four associated data registers into the NCL. These data registers and the NCL can be read and written by the host system.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (refer to Figure 1 below). For the X9428 this is fixed as 0101[B].

Figure 1. Slave Address

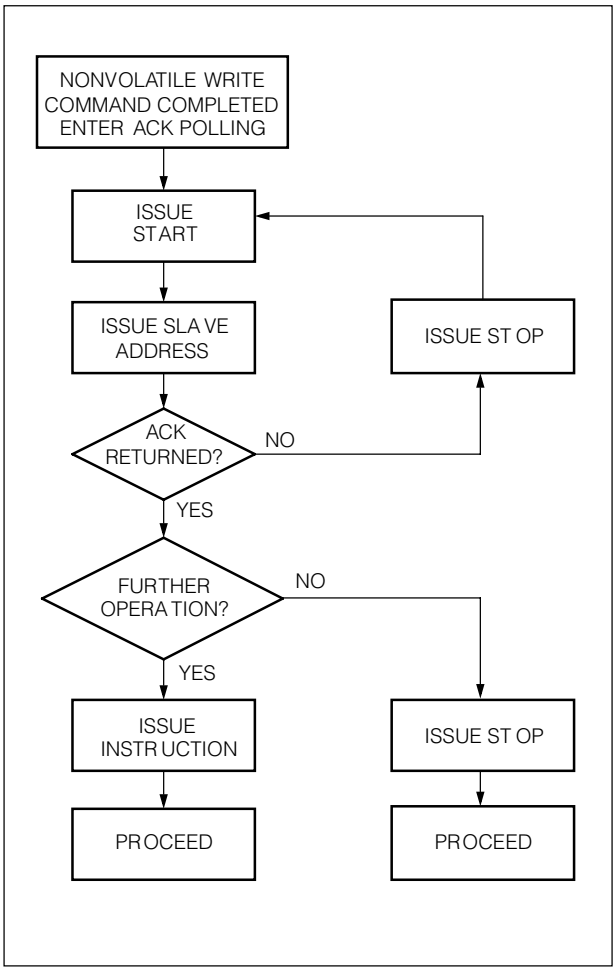


The next four bits of the slave address are the device address. The physical device address is defined by the state of the A0-A2 inputs. The X9428 compares the serial data stream with the address input state; a successful compare of all four address bits is required for the X9428 to respond with an acknowledge. The A_0–A_2 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}.

Acknowledge Polling

The disabling of the inputs, during the internal non-volatile write operation, can be used to take advantage of the typical 5ms E^2PROM write cycle time. Once the stop condition is issued to indicate the end of the nonvolatile write command the X9428 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the device slave address. If the X9428 is still busy with the write operation no ACK will be returned. If the X9428 has completed the write operation an ACK will be returned and the master can then proceed with the next operation.

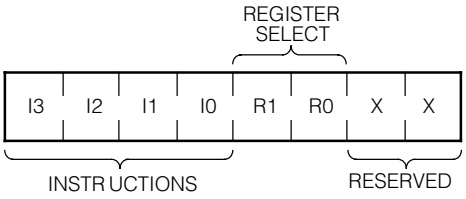
Flow 1. ACK Polling Sequence



Instruction Structure

The next byte sent to the X9428 contains the instruction and register pointer information as shown in Figure 2.

Figure 2. Instruction Byte Format

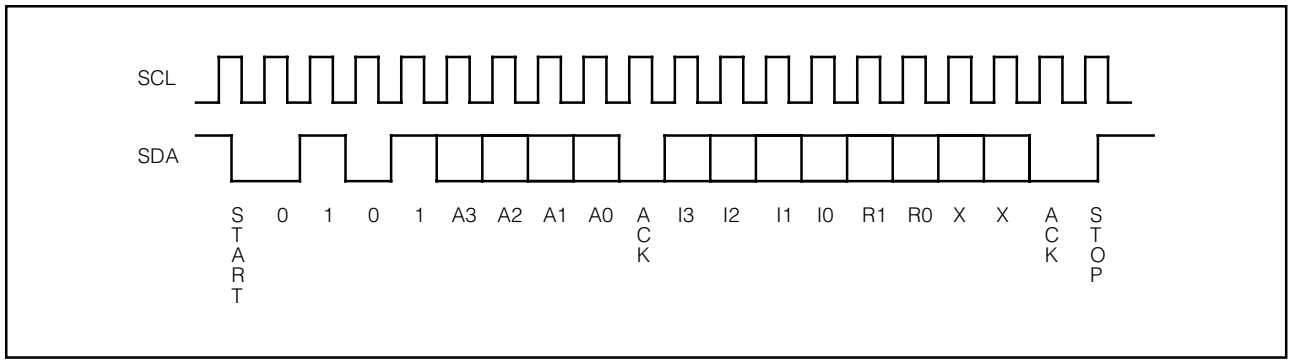


The four high order bits define the instruction. The next two bits (R1 and R0) select one of the four registers that is to be acted upon when a register oriented instruction is issued. The last two bits are reserved and not used.

Four of the nine instructions end with the transmission of the instruction byte. The basic sequence is illustrated in Figure 3. These two-byte instructions exchange data between the Control Latch and one of the data registers. A transfer from a data register to a Control Latch is essentially a write to a static RAM. The response of the wiper to this action will be delayed t_{STPWV}. A transfer from Control Latch current wiper position, to a data register is a write to nonvolatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between the potentiometer and its associated registers.

Four instructions require a three-byte sequence to complete. These instructions transfer data between the host and the X9428; either between the host and one of the data registers or directly between the host and the Control Latch. These instructions are: Read Control Latch, read the current wiper position of the pot Write Control Latch, change current wiper position of the pot Read Data Register, read the contents of the selected nonvolatile register; Write Data Register, write a new value to the selected data register. The sequence of operations is shown in Figure 4.

Figure 3. Two-Byte Command Sequence



The Increment/Decrement command is different from the other commands. Once the command is issued and the X9428 has responded with an acknowledge, the master can clock the wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host. For each SCL clock pulse (t_{HIGH}) while SDA is HIGH, the wiper will move one resistor segment towards the V_H terminal. Similarly, for each SCL clock pulse while SDA is LOW, the wiper will move one resistor segment towards the V_L terminal. A detailed illustration of the sequence and timing for this operation are shown in Figures 5 and 6 respectively.

Table 1. Instruction Set

Instruction	Instruction Set								Operation
	I_3	I_2	I_1	I_0	R_1	R_0	X	X	
Read Control Latch	1	0	0	1	N/A	N/A	N/A	N/A	Read the contents of the Control Latch pointed to by P_1–P_0
Write Control Latch	1	0	1	0	N/A	N/A	N/A	N/A	Write new value to the Control Latch pointed to by P_1–P_0
Read Data Register	1	0	1	1	1/0	1/0	N/A	N/A	Read the contents of the Register pointed to by P_1–P_0 and R_1–R_0
Write Data Register	1	1	0	0	1/0	1/0	N/A	N/A	Write new value to the Register pointed to by P_1–P_0 and R_1–R_0
XFR Data Register to Control Latch	1	1	0	1	1/0	1/0	N/A	N/A	Transfer the contents of the Register pointed to by P_1–P_0 and R_1–R_0 to its associated Control Latch
XFR Control Latch to Data Register	1	1	1	0	1/0	1/0	N/A	N/A	Transfer the contents of the Control Latch pointed to by P_1–P_0 to the Register pointed to by R_1–R_0
Global XFR Data Register to Control Latch	0	0	0	1	1/0	1/0	N/A	N/A	Transfer the contents of all four Data Registers pointed to by R_1–R_0 to their respective Control Latch
Global XFR Control Latch to Data Register	1	0	0	0	1/0	1/0	N/A	N/A	Transfer the contents of all Control Latchs to their respective data Registers pointed to by R_1–R_0
Increment/Decrement Wiper	0	0	1	0	N/A	N/A	N/A	N/A	Enable Increment/decrement of the Control Latch pointed to by P_1–P_0

Notes: (7) 1/0 = data is one or zero
(8) N/A = Not applicable or don't care; that is, a data register is not involved in the operation and need not be addressed (typical)

Figure 4. Three-Byte Command Sequence

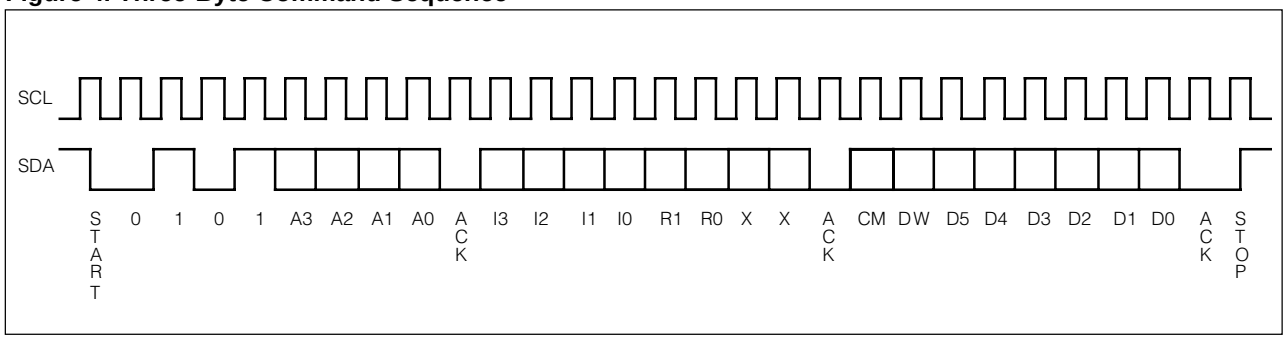


Figure 5. Increment/Decrement Command Squence

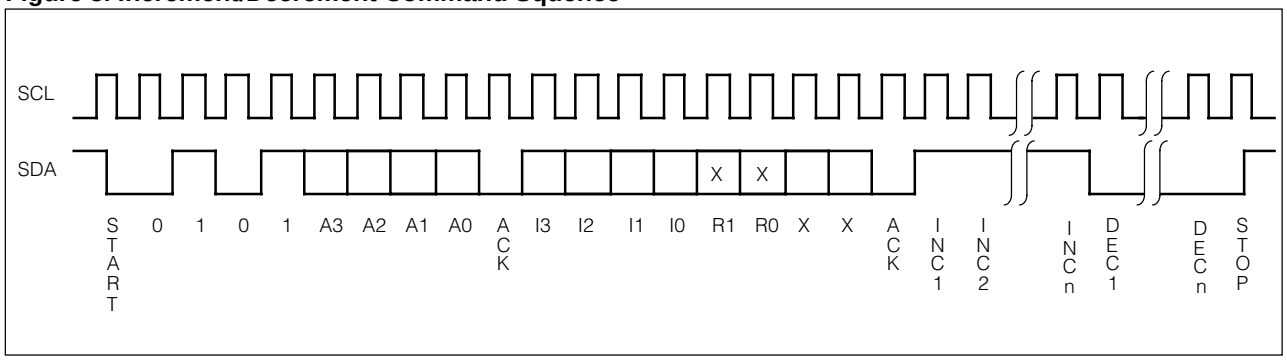


Figure 6. Increment/Decrement Timing Limits

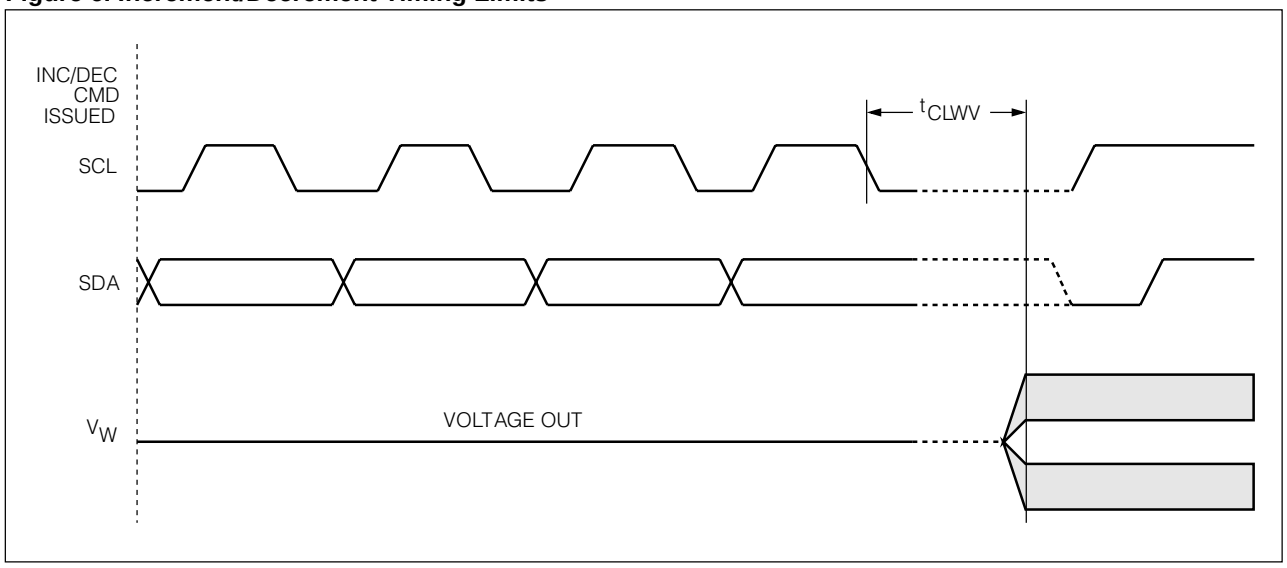


Figure 7. Acknowledge Response from Receiver

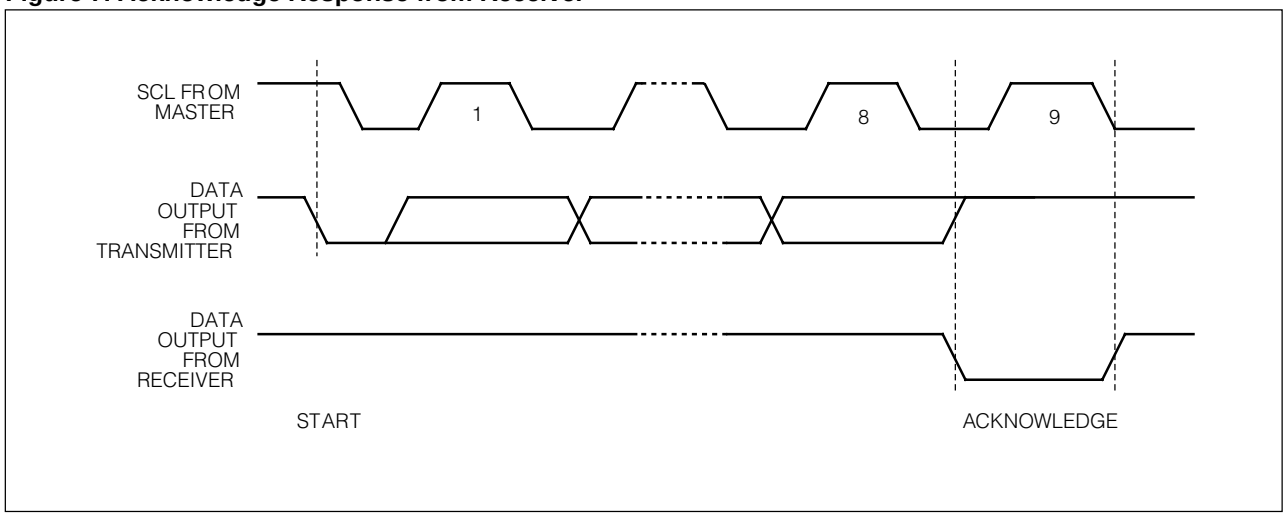
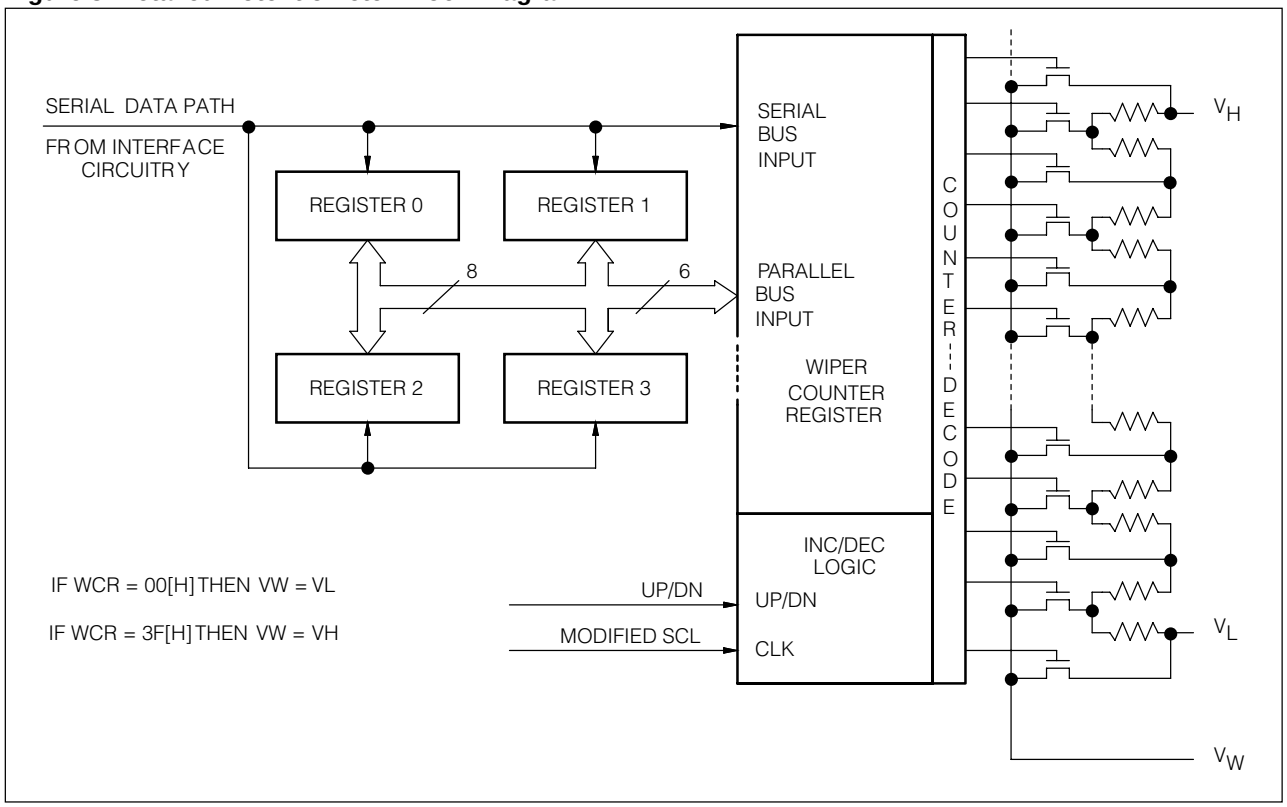


Figure 8. Detailed Potentiometer Block Diagram



DETAILED OPERATION

The XDCP is controlled by the serial interface and is associated with a Control Latch and four data registers. A detailed discussion of the register organization and array operation follows.

Control Latch

The X9428 Control Latch for the XDCP can be envisioned as a 6-bit parallel and serial load counter with its outputs decoded to select one of sixty-four switches along its resistor array. The contents of the Control Latch can be altered in four ways: it may be written directly by the host via the Write Control Latch instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the Increment/ Decrement instruction and it is loaded with the contents of its data register zero (R0) upon power-up.

The Control Latch is a volatile register; that is, its contents are lost when the X9428 is powered-down. Although the register is automatically loaded with the value in R0 upon power-up, it should be noted this may be different from the value present at power-down.

Data Registers

The potentiometer has four nonvolatile data registers. These can be read or written directly by the host and data can be transferred between any of the four data registers and the control latch. It should be noted all operations changing data in one of these registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, these registers can be used as regular memory locations that could possibly store system parameters or user preference data.

Register Descriptions

Wiper Register, WR (6-bit), non-volatile:

WP5	WP4	WP3	WP2	WP1	WP0
NV	NV	NV	NV	NV	NV
(MSB)					(LSB)

- {WP5~WP0}: This is used to store one of the 64 wiper position (0 ~ 63).

Instruction Format

Notes: (1) "MACK"/"SACK": stands for the acknowledge sent by the master/slave.
Notes: (2) "DA3 ~ DA0": stands for the device addresses sent by the master.
Notes: (3) "X": indicates that it is a "0" for testing purpose but physically it is a "don't care" condition.
Notes: (4) "I": stands for the increment operation, SDA held high during active SCL phase (high).
Notes: (5) "D": stands for the decrement operation, SDA held low during active SCL phase (high).
Notes: (6) In dual XDCP devices, "P1" is a "0" for testing purpose but physically it is a "don't care" condition.

Read Wiper Control Latch (RW)

START	device type identifier				device addresses				SACK	instruction opcode				wiper addresses				SACK	wiper position (sent by slave on SDA)								MACK	STOP
	0	1	0	1	DA3	DA2	DA1	DA0		1	0	0	1	X	X	X	X		0	0	WP5	WP4	WP3	WP2	WP1	WP0		

Load Wiper Control Latch (LW)

START	device type identifier				device addresses				SACK	instruction opcode				wiper addresses				SACK	wiper position (sent by master on SDA)								SACK	STOP
	0	1	0	1	DA3	DA2	DA1	DA0		1	0	1	0	X	X	X	X		X	X	WP5	WP4	WP3	WP2	WP1	WP0		

Read Wiper Register (RR)

START	device type identifier				device addresses				SACK	instruction opcode				wiper addresses				SACK	wiper position (sent by slave on SDA)								MACK	STOP
	0	1	0	1	DA3	DA2	DA1	DA0		1	0	1	1	R1	R0	X	X		0	0	WP5	WP4	WP3	WP2	WP1	WP0		

Store Wiper Register (SR)

START	device type identifier				device addresses				SACK	instruction opcode				wiper addresses				SACK	wiper position (sent by master on SDA)								SACK	STOP	
	0	1	0	1	DA3	DA2	DA1	DA0		1	1	0	0	R1	R0	X	X		X	X	WP5	WP4	WP3	WP2	WP1	WP0			HIGH-VOLTAGE WRITE CYCLE

Load Wiper Register to Wiper Latch (LRW)

START	device type identifier				device addresses				SACK	instruction opcode				wiper addresses				SACK	STOP
	0	1	0	1	DA3	DA2	DA1	DA0		1	1	0	1	R1	R0	X	X		

Store Wiper Latch to Wiper Register (SWR)

START	device type identifier				device addresses				SACK	instruction opcode				wiper addresses				SACK	STOP	
	0	1	0	1	DA3	DA2	DA1	DA0		1	1	1	0	R1	R0	X	X			HIGH-VOLTAGE WRITE CYCLE

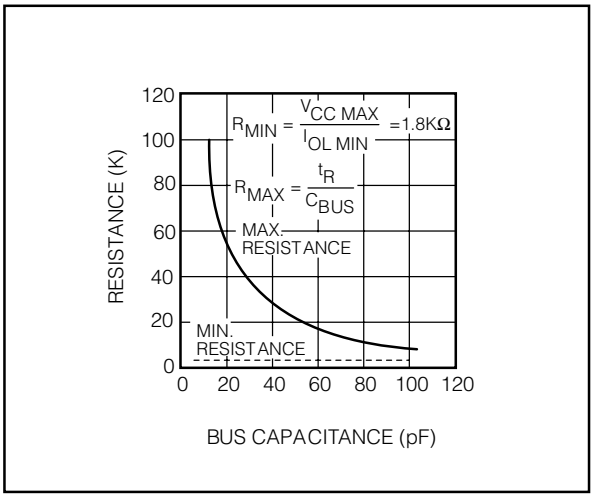
Increment/Decrement Wiper Latch (INCDEC)

START	device type identifier				device addresses				SACK	instruction opcode				wiper addresses				SACK	increment/decrement (sent by master on SDA)						STOP
	0	1	0	1	DA3	DA2	DA1	DA0		0	0	1	0	X	X	X	X		I/D	I/D	.	.	.	I/D	I/D	

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Figure 9. Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias–65°C to +135°C
Storage Temperature–65°C to +150°C
Voltage on SCK, SCL or any Address Input
with Respect to V_{SS}–1V to +7V
Voltage on any V_H or V_L Referenced to V_{SS} ±8V
$\Delta V = |V_H - V_L|$16V
V+, V- ±6V
Lead Temperature (Soldering, 10 seconds)300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C

Supply Voltage	Limits
X9428	5V ±10%
X9428-2.7	2.7V to 5.5V

ANALOG CHARACTERISTICS (Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Units	
R_{TOTAL}	End to End Resistance	–20		+20	%	
	Power Rating			50	mW	25°C, each pot
I_W	Wiper Current	–3		+3	mA	
R_W	Wiper Resistance		150	250	Ω	Wiper Current = ± 1mA
Vv+	Voltage on V+ Pin	2.7		+5.5	V	
Vv-	Voltage on V- Pin	-5.5		-2.7	V	
V_{TERM}	Voltage on any V_H or V_L Pin	V-		V+	V	
	Noise		<-120		dB/$\sqrt{Hz}$	Ref: 1V
	Resolution (4)		1.6		%	
	Absolute Linearity (1)	–1		+1	MI(3)	$V_{w(n)(actual)} - V_{w(n)(expected)}$
	Relative Linearity (2)	–0.2		+0.2	MI(3)	$V_{w(n+1)} - [V_{w(n)} + MI]$
	Temperature Coefficient		±300		ppm/°C	

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Units	
I_{CC}	V_{CC} Supply Current (Active)		3		mA	f_{SCL} = 100KHz, SDA = Open, Other Inputs = V_{SS}
I_{SB}	V_{CC} Current (Standby)		1		µA	SCL = SDA = V_{CC}, Addr. = V_{SS}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IH}	Input HIGH Voltage	V_{CC} x 0.7		V_{CC} x 0.5	V	
V_{IL}	Input LOW Voltage	–0.5		V_{CC} x 0.1	V	
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3mA

Notes: (1) Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
(2) Relative Linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
(3) MI = RTOT/63 or (V_H – V_L)/63, single pot
(4) Max. = all four arrays cascaded together, Typical = individual array resolutions.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Minimum Endurance	100,000	Data Changes per Register
Data Retention	100	Years

CAPACITANCE

Symbol	Test	Max.	Units	Test Conditions
$C_{I/O}$(5)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(5)	Input Capacitance (A0, A1, A2, A3, and SCL)	6	pF	V_{IN} = 0V

POWER-UP TIMING

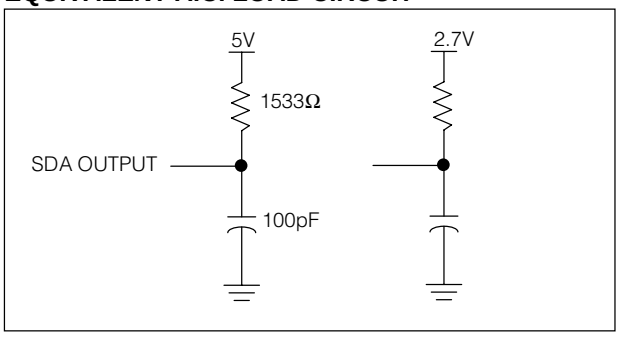
Symbol	Parameter	Max.	Units
t_{PUR}(6)	Power-up to Initiation of Read Operation	1	ms
t_{PUW}(6)	Power-up to Initiation of Write Operation	5	ms

A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

Notes: (5) This parameter is periodically sampled and not 100% tested
(6) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.
These parameters are periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



AC TIMING

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	I^2C Clock Frequency		400	KHz
t_{CYC}	I^2C Clock Cycle Time	2500		nS
t_{HIGH}	I^2C Clock High Time	600		nS
t_{LOW}	I^2C Clock Low Time	1300		nS
$t_{SU:STA}$	Start Setup Time	600		nS
$t_{HD:STA}$	Start Hold Time	600		nS
$t_{SU:STO}$	Stop Setup Time	600		nS
$t_{SU:DAT}$	SDA Data Input Setup Time	100		nS
$t_{HD:DAT\ (4)}$	SDA Data Input Hold Time	0		nS
$t_{R\ (3)}$	SCL and SDA Rise Time		300	nS
$t_{F\ (3)}$	SCL and SDA Fall Time		300	nS
t_{AA}	SCL Low to SDA Data Output Valid Time	100	900	nS
t_{DH}	SDA Data Output Hold Time	50		nS
T_I	I^2C Noise Suppression Time Constant at SCL and SDA inputs	50		nS
t_{BUF}	Bus Free Time (Prior to Any Transmission)	1300		nS
$t_{SU:WPA}$	$\overline{WP}$, A0, A1, A2 Setup Time	0		nS
$t_{HD:WPA}$	$\overline{WP}$, A0, A1, A2 Hold Time	0		nS

HIGH-VOLTAGE WRITE CYCLE TIMING

Symbol	Parameter	Typ.	Max.	Units
t_{WR}	High-voltage Write Cycle Time (Store Instructions)	5	10	mS

EEPOT TIMING

Symbol	Parameter	Min.	Max.	Units
$t_{WRPO\ (2)}$	Wiper Response Time After The Third (Last) Power Supply Is Stable		10	uS
t_{WRL}	Wiper Response Time After Instruction Issued (All Load Instructions)		10	uS
t_{WRID}	Wiper Response Time From An Active SCL/SCK Edge (Increment/Decrement Instruction)		10	uS

Notes: (7) t_{POR} and t_{POW} are the delays required from the time the third (last) power supply (Vcc, V+ or V-) is stable until the specific instruction can be issued. These parameters are periodically sampled and not 100% tested.

(8) The bias order of power supply (Vcc, V+ and V-) don't care.

(9) A device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

TIMING DIAGRAMS

I²C Timing

Figure 10. START and STOP Timing

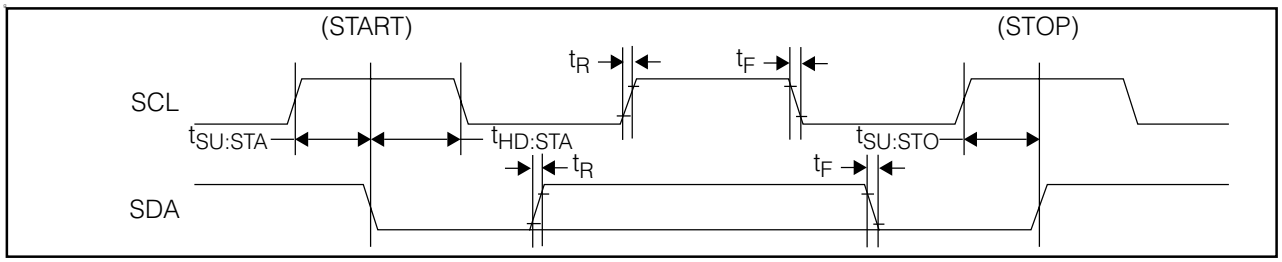


Figure 11. Input Timing

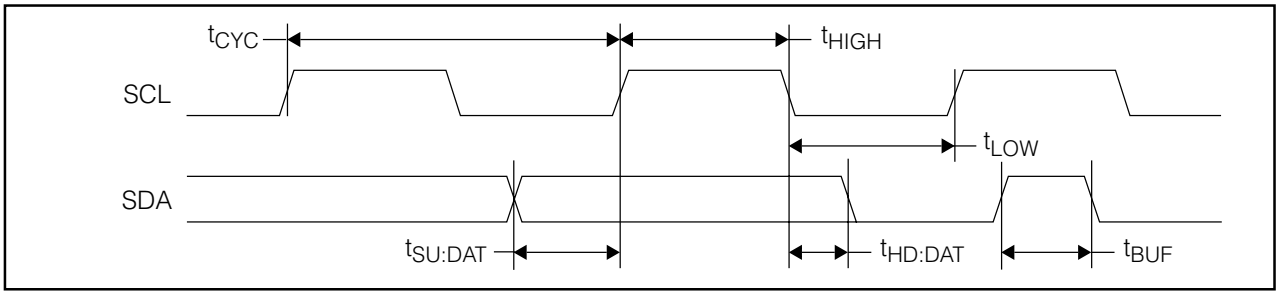


Figure 12. Output Timing

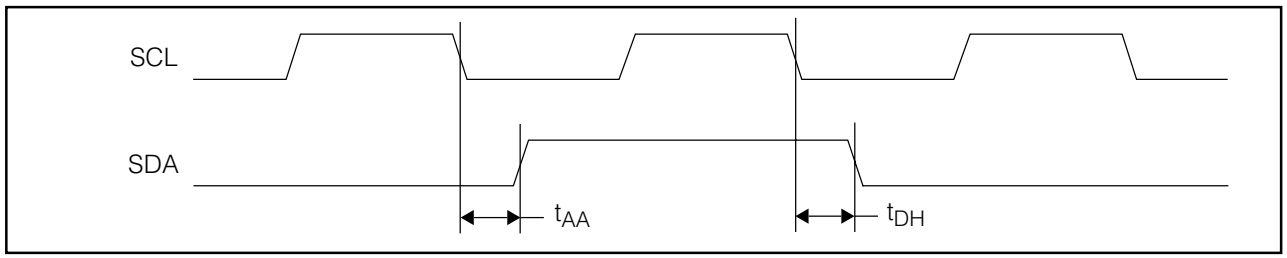


Figure 13. XDCP Timing (for All Load Instructions)

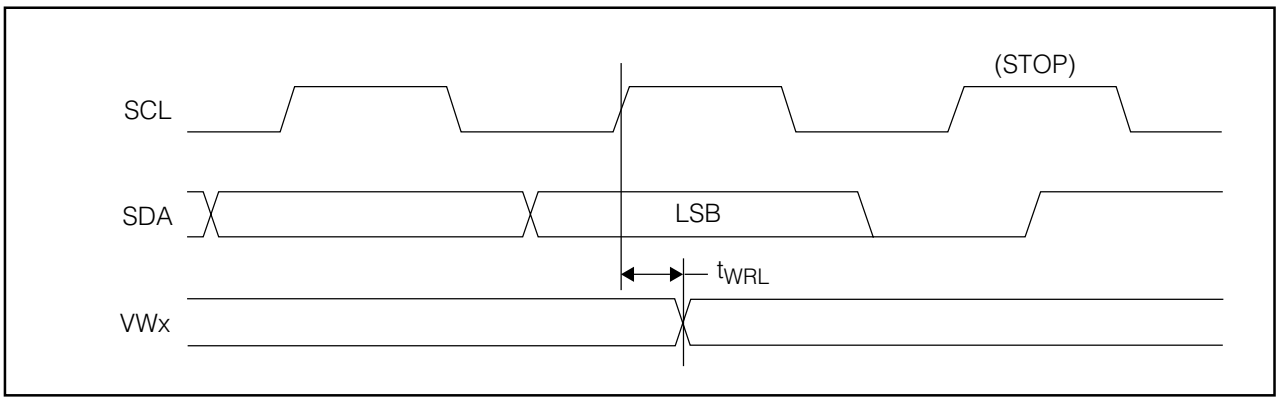


Figure 14. XDCP Timing (for Increment/Decrement Instruction)

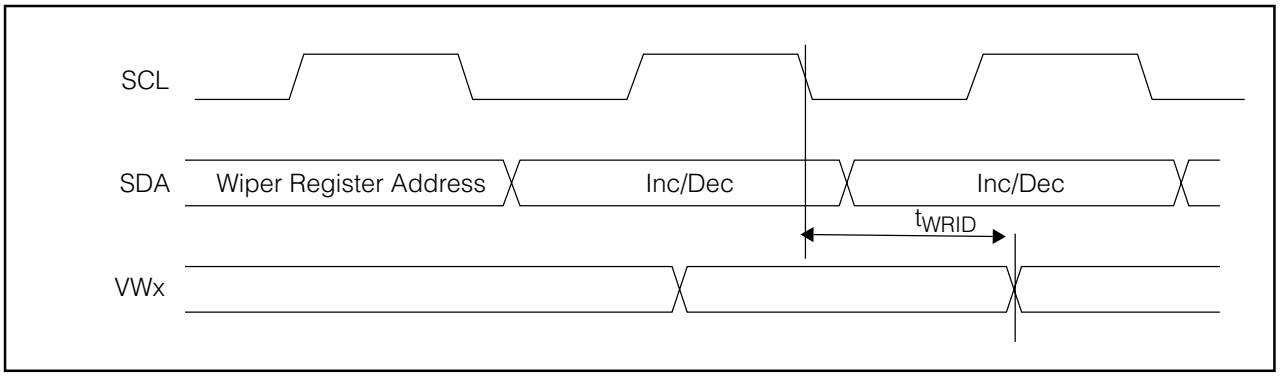
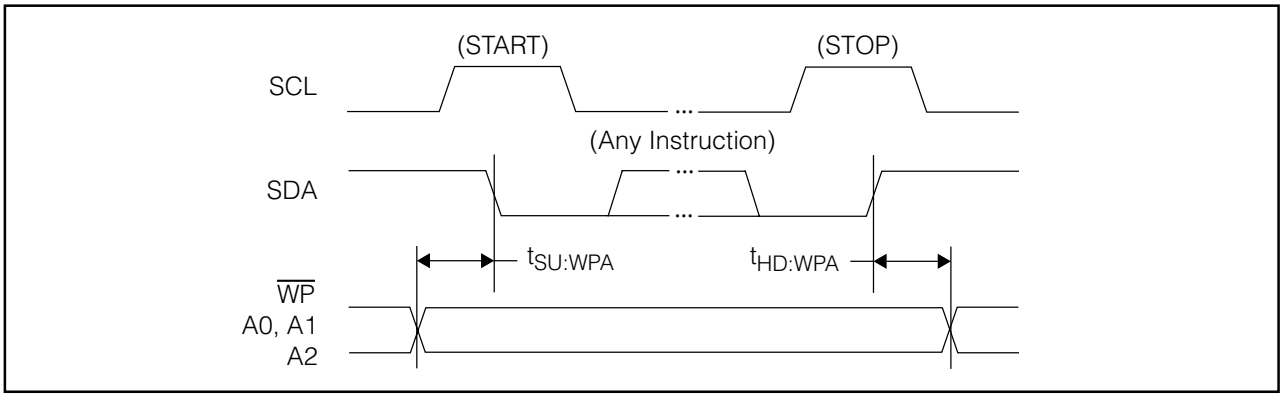


Figure 15. Write Protect and Device Address Pins Timing



ORDERING INFORMATION