

## 14-CHANNEL T1/E1/J1 LONG-HAUL/SHORT-HAUL LINE INTERFACE UNIT

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REV. P1.0.1

## GENERAL DESCRIPTION

The XRT83L314 is a fully integrated 14-channel long-haul and short-haul line interface unit (LIU) that operates from a single 3.3V power supply. Using internal termination, the LIU provides one bill of materials to operate in T1, E1, or J1 mode independently on a per channel basis with minimum external components. The LIU features are programmed through a standard microprocessor interface. EXAR's LIU has patented high impedance circuits that allow the transmitter outputs and receiver inputs to be high impedance when experiencing a power failure or when the LIU is powered off. Key design features within the LIU optimize 1:1 or 1+1 redundancy and non-intrusive monitoring applications to ensure reliability without using relays.

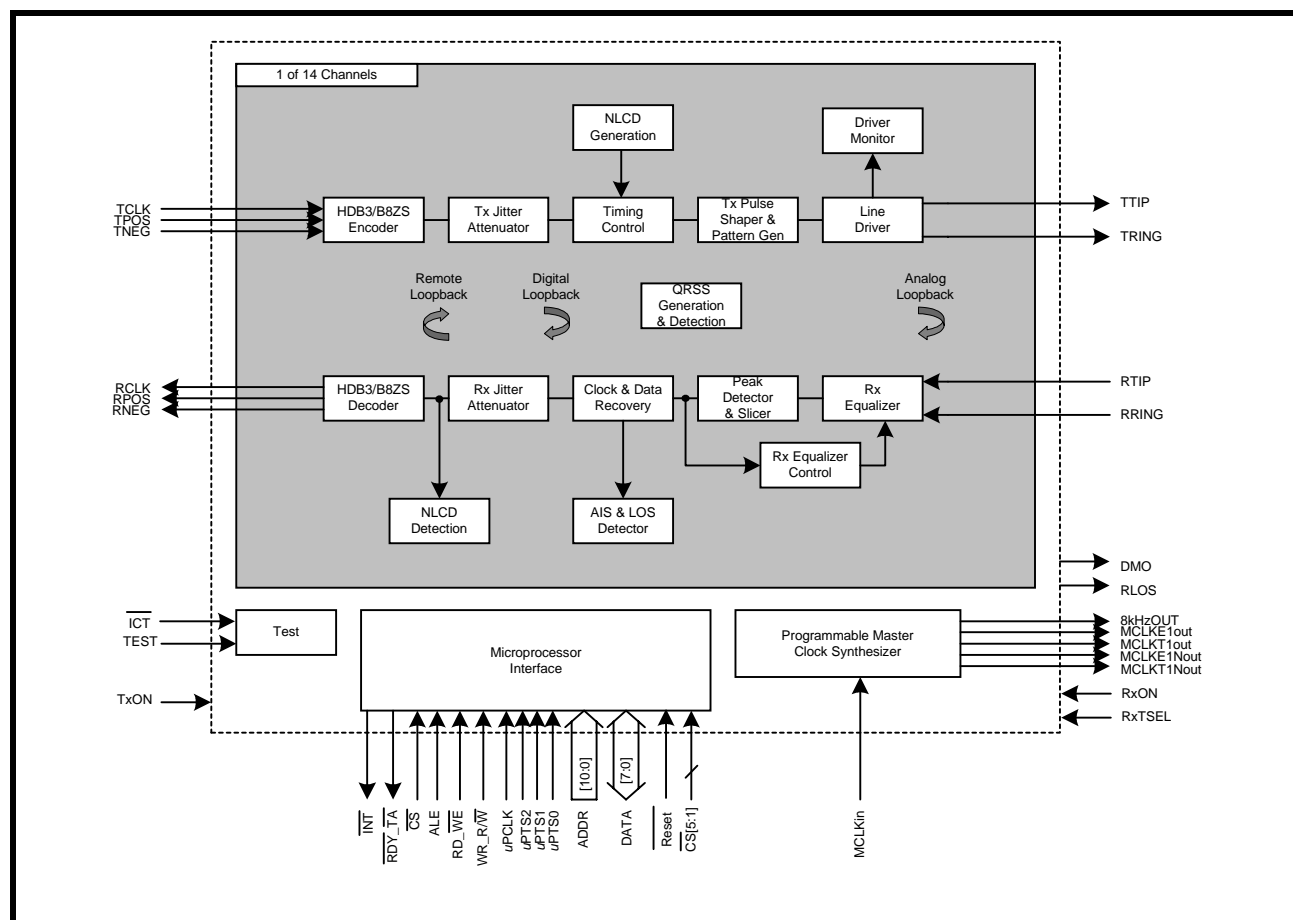
The on-chip clock synthesizer generates T1/E1/J1 clock rates from a selectable external clock frequency and has five output clock references that can be used for external timing (8kHz, 1.544Mhz, 2.048Mhz, nxT1/J1, nxE1).

Additional features include RLOS, a 16-bit LCV counter for each channel, AIS, QRSS generation/detection, Network Loop Code generation/detection, TAOS, DMO, and diagnostic loopback modes.

## APPLICATIONS

- T1 Digital Cross Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public Switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks
- Integrated Multi-Service Access Platforms (IMAPs)
- Integrated Access Devices (IADs)
- Inverse Multiplexing for ATM (IMA)
- Wireless Base Stations

FIGURE 1. BLOCK DIAGRAM OF THE XRT83L314



**FEATURES**

- Fully integrated 14-Channel short haul and long haul transceivers for T1/J1 (1.544MHz) and E1 (2.048MHz) applications.
- T1/E1/J1 short haul, long haul, and clock rate are per port selectable through software without changing components.
- Internal Impedance matching on both receive and transmit for 75Ω (E1), 100Ω (T1), 110Ω (J1), and 120Ω (E1) applications are per port selectable through software without changing components.
- Power down on a per channel basis with independent receive and transmit selection.
- Five pre-programmed transmit pulse settings for T1 short haul applications, as well as an arbitrary programmable waveform generator for custom transmit pulse shaping per channel.
- Arbitrary pulse generator for T1 short haul and T1 long haul modes per channel.
- Transmit line build outs (LBO) for T1 long haul applications from 0dB to -22.5dB in three -7.5dB steps on a per channel basis.
- On-Chip transmit short-circuit protection and limiting protects line drivers from damage on a per channel basis.
- Independent Crystal-Less digital jitter attenuators (JA) with 32-Bit or 64-Bit FIFO for the receive and transmit paths
- On-Chip frequency multiplier generates T1 or E1 master clocks from a variety of external clock sources (8, 16, 56, 64, 128, 256kHz and 1X, 2X, 4X, 8X T1 or E1)
- Driver failure monitor output (DMO) alerts of possible system or external component problems.
- Transmit outputs and receive inputs may be "High" impedance for protection or redundancy applications on a per channel basis.
- Support for automatic protection switching.
- 1:1 and 1+1 protection without relays.
- Selectable receiver sensitivity from 0 to 36dB cable loss in T1 @ 772kHz, and 0 to 43dB cable loss in E1 @ 1,024kHz.
- Receive monitor mode handles 0 to 29dB resistive attenuation (flat loss) along with 0 to 6dB cable loss for both T1 and E1.
- Receiver line attenuation indication output in 1dB steps.
- Loss of signal (RLOS) according to ITU-T G.775/ ETS300233 (E1) and ANSI T1.403 (T1/J1).
- Programmable receive slicer threshold (45%, 50%, 55%, or 68%) for improved receiver interference immunity.
- Programmable data stream muting upon RLOS detection.
- On-Chip HDB3/B8ZS encoder/decoder with an internal 16-bit LCV counter for each channel.
- On-Chip digital clock recovery circuit for high input jitter tolerance.
- QRSS pattern generator and detection for testing and monitoring.
- Error and bipolar violation insertion and detection.
- Transmit all ones (TAOS) and in-band network loop up and loop down code generation.
- Automatic loop code detection for remote loopback activation.
- Supports local analog, remote, digital, and dual loopback modes.
- Low Power dissipation: 170mW per channel (50% density).
- 250mW per channel maximum power dissipation (100% density).
- Single 3.3V supply operation (3V to 5V I/O tolerant).
- 304-Pin TBGA package
- -40°C to +85°C Temperature Range
- Supports gapped clocks for mapper/multiplexer applications.

**PRODUCT ORDERING INFORMATION**

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT83L314IB	304 Lead TBGA	-40°C to +85°C

## PIN OUT OF THE XRT83L314

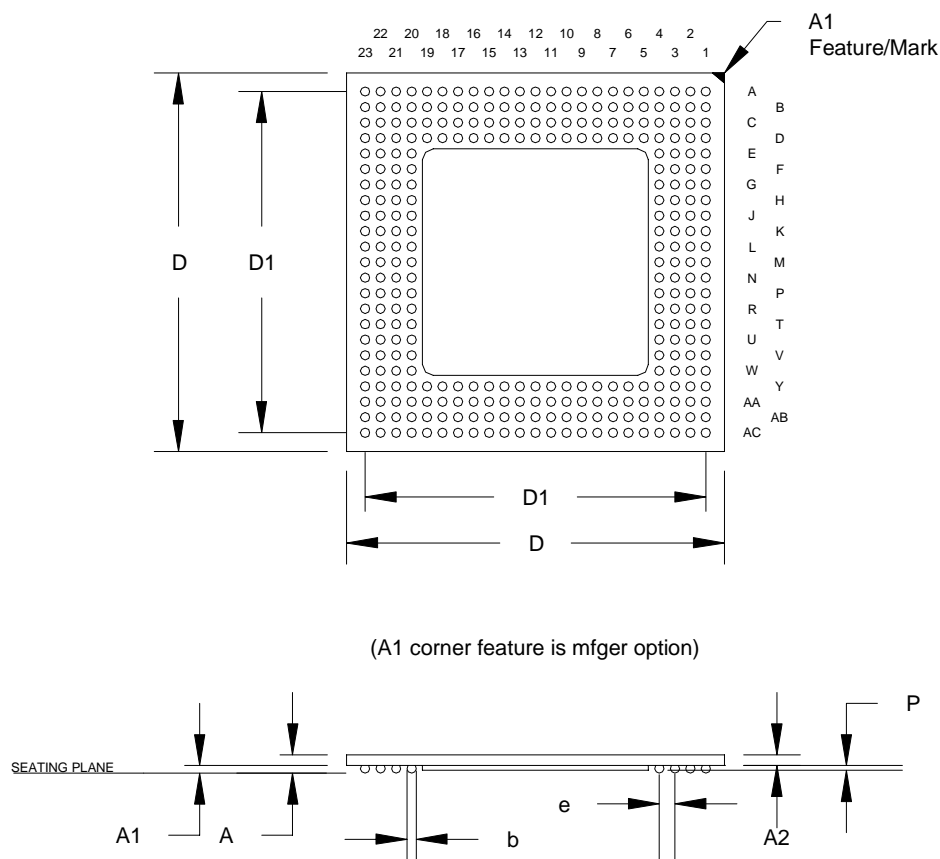
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A[10]	CSB	CSB4	CSB5	TCLK_8	TPOS_10	TPOS_7	DGND_DRV	RVDD_7	RTIP_7	RRING_7	RGND_7	RGND_6	RRING_6	RTIP_6	RVDD_6	ICLKOUT_1	ICLKOUT_0	ICLKOUT_1	ICLKOUT_0	TCLK_5	ICLTB	ICLTB	ICLTB
unnamed.2	RESETB	CSB1	CSB5	TPOS_8	TNEG_9	TNEG_10	TCLK_7	VDDPLL_21	RCLK_7	TVDD_7	TRING_7	TRING_6	TVDD_6	RCLK_6	ICLKOUT_1	TPOS_6	TCLK_3	TCLK_4	TPOS_4	INTB	DGND_DRV	unnamed.1	unnamed.1
RGND_8	A[8]	DVDD_DRV	CSB3	ALE_AS	TNEG_8	TCLK_9	TNEG_7	VDDPLL_22	RNEG_7	TTIP_7	DGND_6	TTIP_6	RNEG_6	GNDPLL_21	TNEG_6	TNEG_6	TNEG_3	TNEG_4	TPOS_5	DVDD_PRE	TRING_5	RGND_5	RGND_5
RRING_8	TRING_8	unnamed.7	DVDD_PRE	CSB2	RDB_DSB	TPOS_9	TCLK_10	DGND_PRE	RPOS_7	TGND_7	DVDD_6	TGND_6	RPOS_6	DVDD_DRV	EIGHT_KVZ	TCLK_6	TPOS_3	TNEG_5	TEST	unnamed.13	TVDD_5	RRING_5	RRING_5
RTIP_8	RVDD_8	TVDD_8	A[9]																unnamed.11	TTIP_5	RVDD_5	RTIP_5	RTIP_5
RVDD_9	RCLK_8	TTIP_8	TGND_8																TGND_5	RNEG_5	RCLK_5	RVDD_4	RVDD_4
RTIP_9	RCLK_9	RNEG_8	RPOS_8																RPOS_5	RNEG_4	RCLK_4	RTIP_4	RTIP_4
RRING_9	TVDD_9	RNEG_9	RPOS_9																RPOS_4	TTIP_4	TRING_4	RRING_4	RRING_4
RGND_9	TRING_9	TTIP_9	TGND_9																TGND_4	TVDD_4	DVDD_3_4_5	RGND_4	RGND_4
DVDD_8_9_10	unnamed.1	unnamed.3	unnamed.4																AVDD_BIAS	DVDD_DRV	unnamed.14	unnamed.16	unnamed.16
DGND_8_9_10	unnamed.6	DGND_DRV	DGND_PRE																DGND_PRE	AGND_BIAS	DGND_3_4_5	unnamed.10	unnamed.10
RGND_10	TRING_10	TTIP_10	TGND_10																TGND_3	TTIP_3	TRING_3	RGND_3	RGND_3
RRING_10	TVDD_10	RNEG_10	RPOS_10																RPOS_3	RNEG_3	TVDD_3	RRING_3	RRING_3
RTIP_10	RCLK_10	RNEG_11	RPOS_11																RPOS_2	RNEG_2	RCLK_3	RTIP_3	RTIP_3
RVDD_10	RCLK_11	TTIP_11	TGND_11																TGND_2	TTIP_2	RCLK_2	RVDD_3	RVDD_3
RTIP_11	RVDD_11	TVDD_11	TRING_11																DGND_1_2	TVDD_2	RVDD_2	RTIP_2	RTIP_2
RRING_11	DVDD_DRV	DVDD_11_12	DGND_11_12																TVDD_1	DGND_DRV	TRING_2	RRING_2	RRING_2
RGND_11	TRING_12	TVDD_12	TGND_12																TGND_1	TRING_1	DVDD_1_2	RGND_2	RGND_2
RRING_12	RGND_12	TTIP_12	RPOS_12																RPOS_1	TTIP_1	RGND_1	RRING_1	RRING_1
RTIP_12	RCLK_12	RNEG_12	DVDD_PRE	A[1]	A[7]	TCLK_12	TCLK_13	RXTSEL	RPOS_13	TGND_13	DGND_13	TGND_13	RPOS_13	GNDPLL_12	TPOS_0	TNEG_1	D[3]	DVDD_PRE	D[0]	RNEG_1	RVDD_1	RTIP_1	RTIP_1
RVDD_12	unnamed.5	UPTS0	A[2]	A[6]	TPOS_12	TNEG_11	DVDD_DRV	DVDD_UP	RNEG_13	TTIP_13	DVDD_13_0	TTIP_0	RNEG_0	RCLK_0	DGND_DRV	TNEG_2	TPOS_1	D[4]	D[7]	RDY_DTBK	RCLK_1	unnamed.9	unnamed.9
DGND_DRV	UPTS1	A[3]	A[5]	RXOFF	TPOS_11	TPOS_13	DVDDPLL_12	DGND_UP	RCLK_13	TVDD_13	TRING_13	TRING_13	TVDD_0	RVDD_0	DGND_PRE	TNEG_0	TPOS_2	D[0]	D[2]	D[6]	UPCLK	RLOS	RLOS
UPTS2	A[0]	A[4]	TXOFF	TNEG_12	TCLK_11	TNEG_13	DVDDPLL_11	RVDD_13	RTIP_13	RRING_13	RGND_13	RGND_13	RRING_0	RTIP_0	GNDPLL_11	TCLK_0	TCLK_2	TCLK_1	D[1]	D[5]	DVDD_DRV	unnamed.0	unnamed.0

Bottom View

## ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83L314IB	304 LEAD TBGA	-40 <sup>0</sup> C to +85 <sup>0</sup> C

## PACKAGE DIMENSIONS (DIE DOWN)



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.051	0.067	1.30	1.70
A1	0.018	0.028	0.45	0.70
A2	0.031	0.071	0.80	1.80
P	0.004	0.012	0.10	0.30
D	1.213	1.228	30.80	31.20
D1	1.100 BSC		27.94 BSC	
b	0.024	0.035	0.60	0.90
e	0.050 BSC		1.27 BSC	

**REVISION HISTORY**

REVISION #	DATE	DESCRIPTION
P1.0.0	02/14/03	First release of the 14-Channel LIU Preliminary Datasheet
P1.0.1	03/27/03	Added the 16-bit LCV Counter Details for Revision B Silicon

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