Advance Data Sheet
September 1996

microelectronics group

Lucent Technologies
Bell Labs Innovations

Z80
8-Bit Microprocessor

Features

- CMOS performance:
  — Z84C0020—dc to 20 MHz
- 6 MHz version can be operated at 6.144 MHz clock
- Z80 microprocessors and associated family of peripherals can be linked by a vectored interrupt system; system can be daisy-chained to allow implementation of a priority interrupt scheme
- Duplicate set of both general-purpose and flag registers
- Two 16-bit index registers
- Three modes of maskable interrupts:
  — Mode 0—8080A similar
  — Mode 1—Non-Z80 environment, location 38H
  — Mode 2—Z80 family peripherals, vectored interrupts
- On-chip dynamic memory refresh counter
- Samples available for system evaluation:
  — 40-pin DIP
  — 44-pin MQFP
  — 44-pin PLCC

Description

The CPUs are fourth-generation enhanced microprocessors with outstanding computational power. As opposed to comparable second- and third-generation microprocessors, these CPUs have a higher overall system and more efficient memory utilization. The programmer can access 208 bits of read/write memory from the internal registers. These internal registers include two sets of six general-purpose registers, which may be used individually as either 8-bit registers or as 16-bit register pairs. There are, additionally, two sets of accumulator and flag registers. A group of "exchange" instructions makes their set of main or alternate registers accessible to the programmer. The alternate set allows operation in foreground-background mode, or it may be reserved for very fast interrupt response.

The CPU also contains a stack pointer, program counter, two index registers, a refresh register (counter), and an interrupt register. Since it requires only a single +5 V power source, the CPU is easy to incorporate into a system. All output signals are fully decoded and timed to control standard memory or peripheral circuits; the CPU is supported by an extensive family of peripheral controllers. The block diagram (Figure 1) shows the primary functions of the processors.

Description (continued)

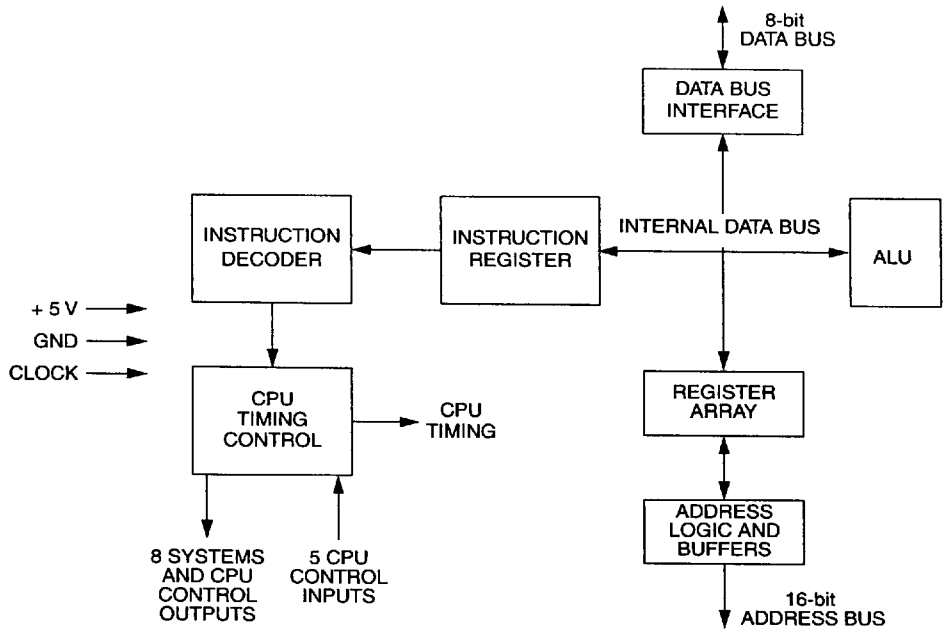

Figure 1. Block Diagram

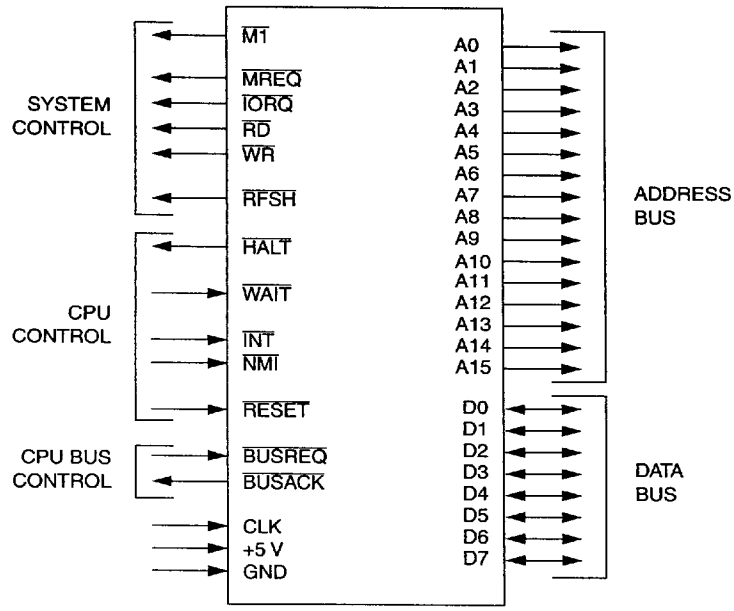

Figure 2. Pin Functions

Description (continued)

Pin Diagrams

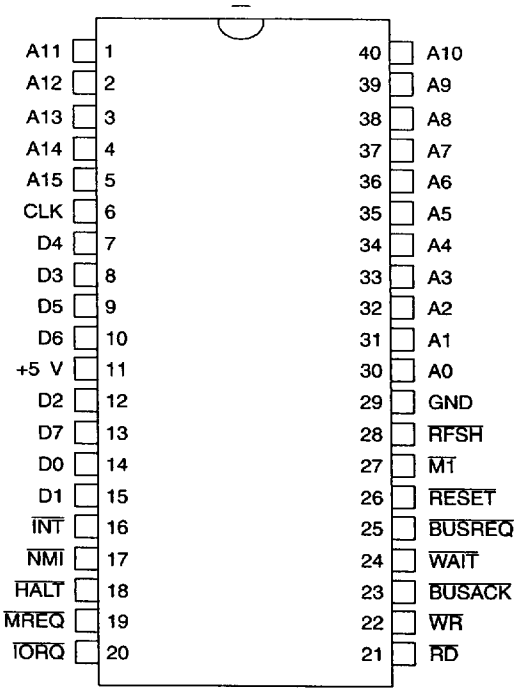

Figure 3. 40-Pin Dual-In-Line (DIP), Pin Assignments

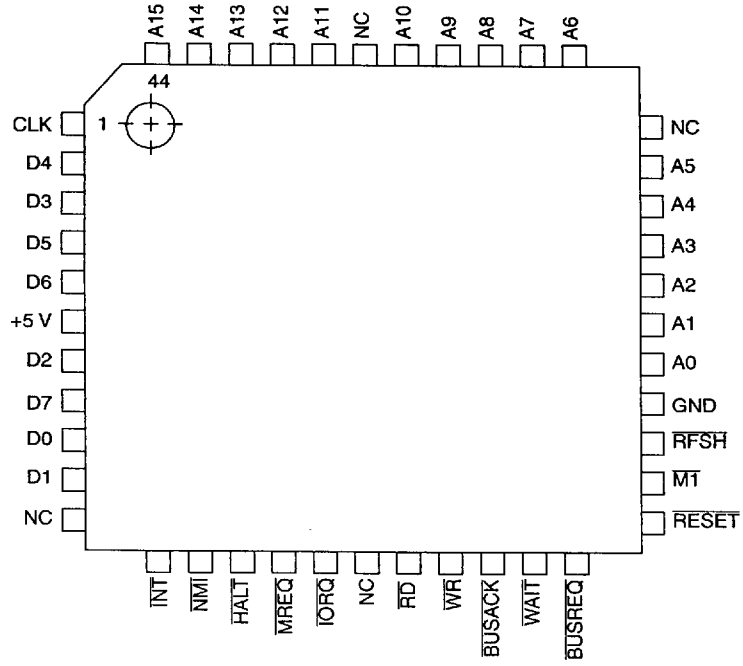

Figure 4. 44-Pin Metric Quad Flat Pack (MQFP)/Plastic Leaded Chip Carrier (PLCC), Pin Assignments

Signal Information

Table 1. Signal Descriptions

Symbol	Type	Name/Function
$\overline{\text{BUSREQ}}$	I	**Bus Request (Active-Low).** Bus request has a higher priority than $\overline{\text{NMI}}$ and is always recognized at the end of the current machine cycle. $\overline{\text{BUSREQ}}$ forces the CPU address bus, the data bus, and the control signals $\overline{\text{MREQ}}$, $\overline{\text{IORQ}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ to go to a high-impedance state so that other devices can control these lines. $\overline{\text{BUSREQ}}$ is normally wired OR and requires an external pull-up for these applications. Extended $\overline{\text{BUSREQ}}$ periods due to extensive DMA operations can prevent the CPU from properly refreshing dynamic RAMs.
$\overline{\text{INT}}$	I	**Interrupt Request (Active-Low).** Interrupt request is generated by I/O devices. The CPU honors a request at the end of the current instruction if the internal software-controlled interrupt enable flip-flop (IFF) is enabled. $\overline{\text{INT}}$ is normally wired OR and requires an external pull-up for these applications.
$\overline{\text{NMI}}$	I	**Nonmaskable Interrupt (Negative Edge Triggered).** $\overline{\text{NMI}}$ has a higher priority than $\overline{\text{INT}}$. $\overline{\text{NMI}}$ is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop, and automatically forces the CPU to restart at location 0066H.
$\overline{\text{RESET}}$	I	**Reset (Active-Low).** $\overline{\text{RESET}}$ initializes the CPU as follows: it resets the interrupt enable flip-flop, clears the PC and registers I and R, and sets the interrupt status to mode 0. During reset time, the address and data bus go to a high-impedance state, and all control output signals go to the inactive state. Note that $\overline{\text{RESET}}$ must be active for a minimum of three full clock cycles before the reset operation is complete.
$\overline{\text{WAIT}}$	I	**Wait (Active-Low).** $\overline{\text{WAIT}}$ indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter a wait-state as long as this signal is active. Extended $\overline{\text{WAIT}}$ periods can prevent the CPU from properly refreshing dynamic memory.
A0—A15	O	**Address Bus (Active-High, Tristate).** A0—A15 form a 16-bit address bus. The address bus provides the memory data bus exchanges (up to 64 Kbytes) and for I/O device exchanges.
$\overline{\text{BUSACK}}$	O	**Bus Acknowledge (Active-Low).** Bus acknowledge indicates to the requesting device that the CPU address bus, data bus, and the control signals $\overline{\text{MREQ}}$, $\overline{\text{IORQ}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ have entered their high-impedance states. The external circuitry can now control these lines.
HALT	O	**Halt State (Active-Low).** $\overline{\text{HALT}}$ indicates that the CPU has executed a halt instruction and is awaiting either a nonmaskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOPs to maintain memory refresh.
$\overline{\text{IORQ}}$	O	**Input/Output Request (Active-Low, Tristate).** $\overline{\text{IORQ}}$ indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. $\overline{\text{IORQ}}$ is also generated concurrently with $\overline{\text{M1}}$ during an interrupt acknowledge cycle to indicate that an interrupt response vector can be placed on the data bus.
$\overline{\text{M1}}$	O	**Machine Cycle One (Active-Low).** $\overline{\text{M1}}$, together with $\overline{\text{MREQ}}$, indicates that the current machine cycle is the opcode fetch cycle of an instruction execution. $\overline{\text{M1}}$, together with $\overline{\text{IORQ}}$, indicates an interrupt acknowledge cycle.
$\overline{\text{MREQ}}$	O	**Memory Request (Active-Low, Tristate).** $\overline{\text{MREQ}}$ indicates that the address bus holds a valid address for a memory read or memory write operation.
$\overline{\text{RD}}$	O	**Read (Active-Low, Tristate).** $\overline{\text{RD}}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
$\overline{\text{RFSH}}$	O	**Refresh (Active-Low).** $\overline{\text{RFSH}}$, together with $\overline{\text{MREQ}}$, indicates that the lower 7 bits of the system's address bus can be used as a refresh address to the system's dynamic memories.
$\overline{\text{WR}}$	O	**Write (Active-Low, Tristate).** $\overline{\text{WR}}$ indicates that the CPU data bus holds valid data to be stored at the addressed memory or I/O location.
D0–D7	I/O	**Data Bus (Active-High, Tristate).** D0—D7 constitute an 8-bit bidirectional data bus, used for data exchanges with memory and I/O.

Signal Information (continued)

Netlist Order

Inputs: $\overline{\text{BUSREQ}}$, $\overline{\text{INT}}$, $\overline{\text{NMI}}$, $\overline{\text{RESET}}$, $\overline{\text{WAIT}}$

Outputs: A0–A15, $\overline{\text{BUSACK}}$, $\overline{\text{HALT}}$, $\overline{\text{IORQ}}$, $\overline{\text{M1}}$, $\overline{\text{MREQ}}$, $\overline{\text{RD}}$, $\overline{\text{RFSH}}$, $\overline{\text{WR}}$

IOputs: D0—D7

Instruction Set

Of any 8-bit microprocessor, this microprocessor has one of the most powerful and versatile instruction sets available. It includes such unique operations as a block move for fast, efficient data transfers within memory, or between memory and I/O. It also allows operations on any bit in any location in memory.

More detailed information for programming use can be found in the Zilog's *Z8400/Z84C00 NMOS/CMOS Z80 CPU Central Processing Unit Product Specification*, *Z80 CPU Technical Manual*, the *Programmer's Reference Guide*, and *Assembly Language Programming Manual*.

The instructions are divided into the following categories

- 8-bit loads
- 16-bit loads
- Exchanges, block transfers, and searches
- 8-bit arithmetic and logic operations
- General-purpose arithmetic and CPU control
- 16-bit arithmetic operations
- Rotates and shifts
- Bit set, reset, and test operations
- Jumps
- Calls, returns, and restarts
- Input and output operations

A variety of addressing modes are implemented to permit efficient and fast data transfer between various registers, memory locations, and input/output devices. These addressing modes include:

- Immediate
- Immediate extended
- Modified page zero
- Relative
- Extended
- Indexed
- Register
- Register indirect
- Implied
- Bit