ACS573MS

Radiation Hardened Octal Three-State Transparent Latch

January 1996

Features

- Devices QML Qualified in Accordance with MIL-PRF-38535
- Detailed Electrical and Screening Requirements are Contained in SMD# 5962-96724 and Intersil's QM Plan
- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose . . . . . >300K RAD (Si)
- Single Event Upset (SEU) Immunity: <1 x 10^{-10} Errors/Bit/Day (Typ)
- SEU LET Threshold . . . . . >100 MEV-cm^2/mg
- Dose Rate Upset . . . . . >10^{11} RAD (Si)/s, 20ns Pulse
- Dose Rate Survivability . . . . . >10^{12} RAD (Si)/s, 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range . . . . . -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range . . . . . 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current ≤ 1μA at VOL, VOH
- Fast Propagation Delay . . . . . 17ns (Max), 12ns (Typ)

Description

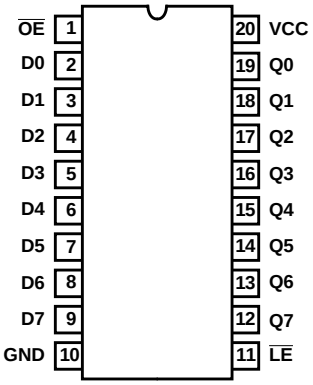
The Intersil ACS573MS is a Radiation Hardened Octal Transparent Latch with an active low output enable. The outputs are transparent to the inputs when the latch enable ($\overline{LE}$) is High. When the latch goes low the data is latched. The output enable controls the three-state outputs. When the output enable pins ($\overline{OE}$) are high the output is in a high impedance state. The latch operation is independent of the state of output enable.

The ACS573MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of a radiation hardened, high-speed, CMOS/SOS Logic family.

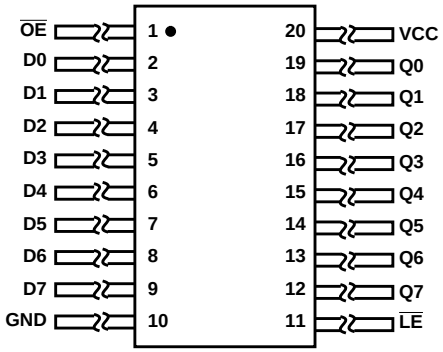
The ACS573MS is supplied in a 20 lead Ceramic Flatpack (K suffix) or a

Pinouts

20 LEAD CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR,
CDIP2-T20, LEAD FINISH C
TOP VIEW



20 LEAD CERAMIC FLATPACK
MIL-STD-1835 DESIGNATOR,
CDFP4-F20, LEAD FINISH C
TOP VIEW



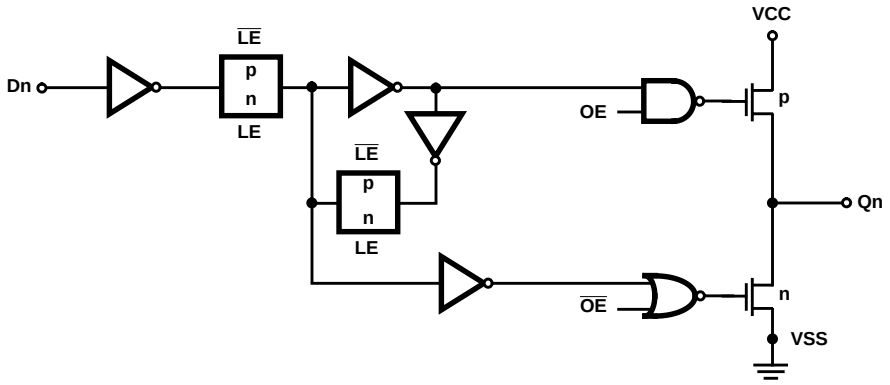
Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962F9672401VRC	-55°C to +125°C	MIL-PRF-38535 Class V	20 Lead SBDIP
5962F9672401VXC	-55°C to +125°C	MIL-PRF-38535 Class V	20 Lead Ceramic Flatpack
ACS573D/Sample	25°C	Sample	20 Lead SBDIP
ACS573K/Sample	25°C	Sample	20 Lead Ceramic Flatpack
ACS573HMSR	25°C	Die	Die

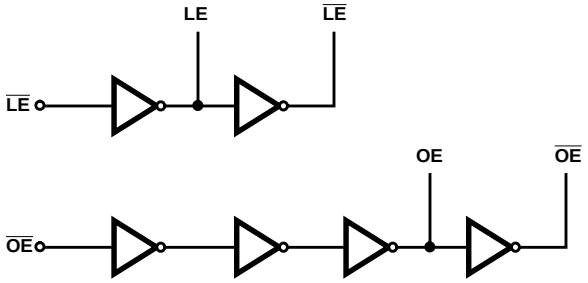
Spec Number **518893**
File Number **4093**

Functional Diagram

1 OF 8 IDENTICAL CIRCUITS



COMMON CONTROLS



TRUTH TABLE

$\overline{OE}$	$\overline{LE}$	DATA	OUTPUT
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

NOTE: L = Low Logic Level, H = High Logic Level, X = Don't Care, Z = High Impedance, l = Low Voltage Level Prior to High-to-Low Latch Enable Transition, h = High Voltage Level Prior to High-to-Low Latch Enable Transition.

Die Characteristics

DIE DIMENSIONS:

102 mils x 102 mils
2,600mm x 2,600mm

METALLIZATION:

Type: AlSi
Metal 1 Thickness: 7.125kÅ ±1.125kÅ
Metal 2 Thickness: 9kÅ ±1kÅ

GLASSIVATION:

Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

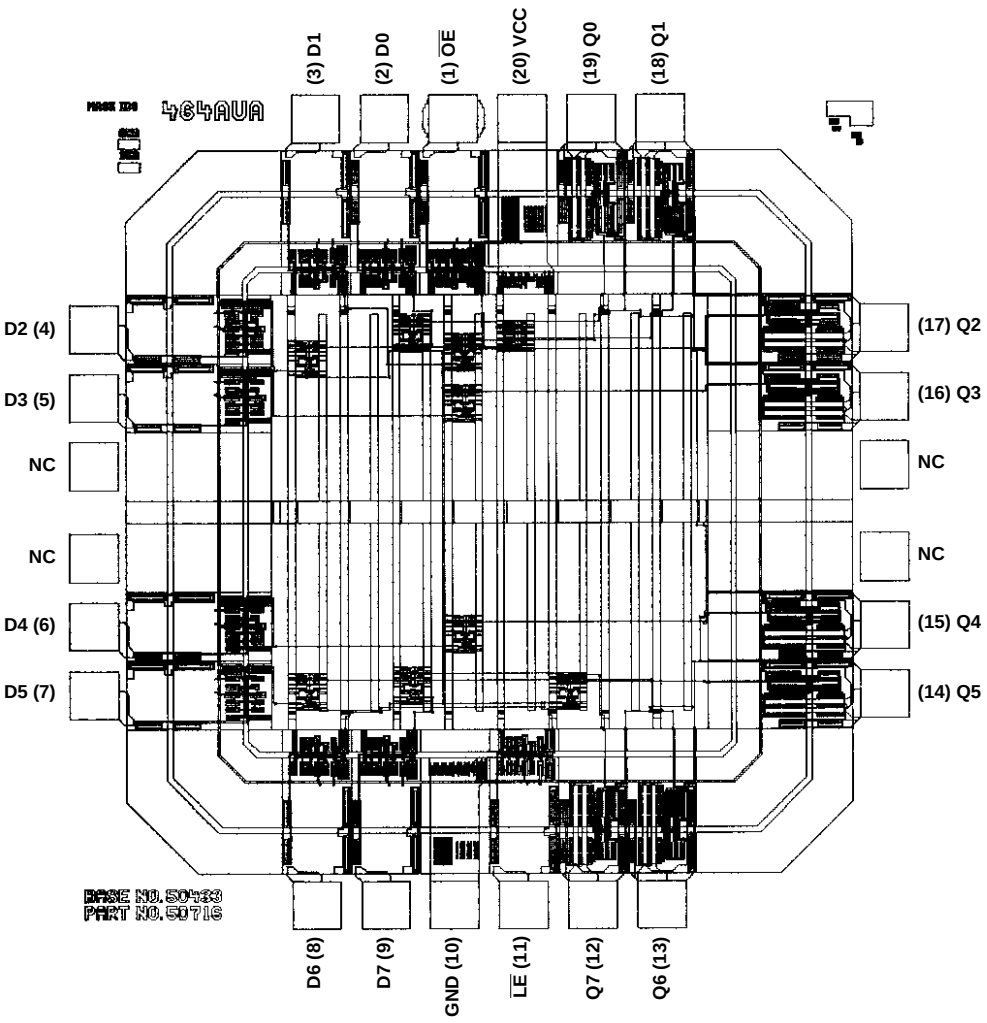
$<2.0 \times 10^5$ A/cm^2

BOND PAD SIZE:

> 4.3 mils x 4.3 mils
> 110µm x 110µm

Metallization Mask Layout

ACS573MS



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