Data Sheet
March 1992

AT&T Microelectronics

ATT20C478A/477A/475A CMOS RAMDACs

Features

- 110/100/80/66/50 MHz operation
- Powerdown to ≤3 mA typical (ATT20C477A/475A)
- Low power dissipation (0.5 W typical)
- On-chip output comparators for monitor detection (ATT20C477A/475A)
- Internal V_{REF} accuracy better than ±3%
- Automatic external V_{REF} disable during powerdown (ATT20C477A/475A)
- External V_{REF} option
- Antisparkle circuitry
- 6- or 8-bit DAC (ATT20C478A/477A)
- 256 x 24 (18) palette
- 15 x 24 (18) overlay palette
- Programmable blank pedestal
- Synchronization on all three channels
- RS-343A, RS-170, and *PS/2** compatible
- 471 RAMDAC (internal or external voltage reference only) operating mode
- Epitaxial layer over substrate for reduced noise feedthrough
- Latch-up immunity >250 mA
- Industry-compatible footprints
- Monolithic 0.9 µm CMOS

* *PS/2* is a registered trademark of International Business Machines Corporation.

Applications

- Desktop, laptop, and notebook PCs
- Screen resolutions (noninterlaced)
  — 1280 x 1024, 60 Hz
  — 1024 x 1024, 76 Hz
- True-color using three devices

Description

The ATT20C478A/477A/475A RAMDACs are designed to increase speed and reduce power in the digital-to-analog conversion of frame buffer images. The ATT20C477A/475A power down to ≤3 mA total current while retaining palette data and read/write capability. On-chip output comparators detect connection to a monitor on the ATT20C477A/475A. All parts contain antisparkle circuitry.

The ATT20C478A/477A/475A have a 256 x 24 (18) look-up table (LUT) displaying 256 colors out of 16.8 M (262K) possible.

The ATT20C478A/477A/475A are designed in AT&T's 0.9 µm CMOS process, adding performance and speed (110 MHz) to industry-standard capabilities. CMOS design and unique RAM cell structure contribute to one of the lowest power dissipations in the industry. Internal voltage reference with better than ±3% accuracy helps to ensure that your product meets PC graphics requirements, and eliminates the need for external references.

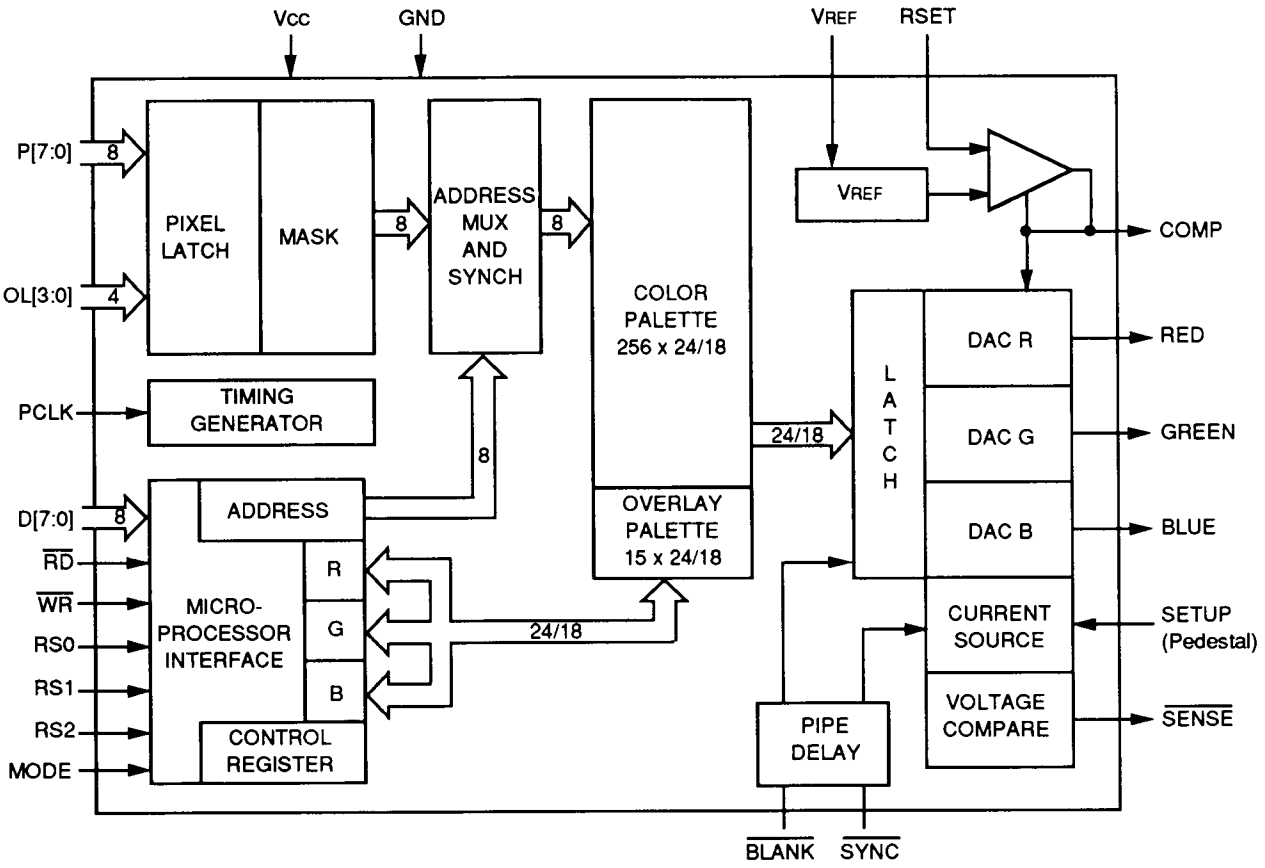
All parts are offered in industry-standard 44-pin PLCC packages and compatible footprints. These parts are meant to work with a voltage reference only (internal or external).

Table of Contents

Contents Page

Features 1
Applications 1
Description 1
Pin Information 4
Functional Description 6
Internal Registers 7
MPU Interface 8
Writing the RAMDAC 8
Reading the RAMDAC 8
Writing the Overlay Registers 8
Reading the Overlay Registers 9
Additional Information 9
471 RAMDAC Compatible Operation 9
6-/8-bit Color Resolution 10
Pixel and Overlay Pins 10
Powerdown 10
$\overline{\text{SENSE}}$ Output 10
DAC Gain 11
Application Information 15
Board Layout 15
Power Distribution 15
Decoupling Capacitors 15
Digital Signals 15
Analog Signals 16
DAC Outputs 16
Multiple RAMDACs 19
Absolute Maximum Ratings 19
Recommended Operating Conditions 19
Electrical Characteristics 20
Timing Characteristics 25
Outline Diagram 26
44-Pin PLCC Package 26
Ordering Information 27
Revision History 27

Description (continued)



Note: Control register on ATT20C477A/475A only.

Figure 1. Block Diagram

Table 1. ATT20C478A/477A/475A Features

Part Number	Anti-Sparkle	Internal V_{REF}	110/100/80/66/50 MHz	Output Compare	Power-down	6-/8-bit Switchable
478A	Yes	Yes	Yes	No	No	Yes
477A	Yes	Yes	Yes	Yes	Yes	Yes
475A	Yes	Yes	Yes	Yes	Yes	No

Pin Information

Top View.

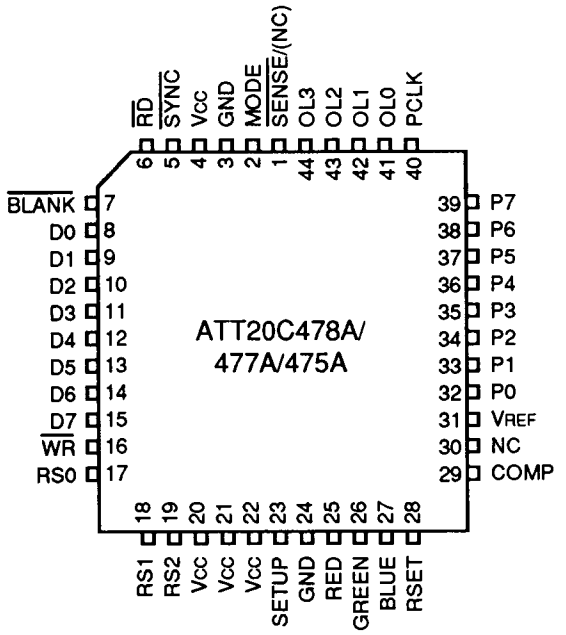


Figure 2. Pin Diagram ATT20C478A/477A/475A

Table 2. Functionality for Pins 1 and 2

Part	Mode (Pin 2)	$\overline{\text{SENSE}}$ (Pin 1)
478A	478A/ $\overline{471}$	No internal connection
477A	477A/ $\overline{471}$	$\overline{\text{SENSE}}$
475A	475A/ $\overline{471}$	$\overline{\text{SENSE}}$

Notes:
471 functionality = 478A fixed at 6 bits per pixel with an internal or external voltage reference only.

For 471 function, use the ATT20C478A/477A/475A with pin 2 tied to TTL low or left unconnected.

When using the ATT20C477A/475A as an 471, do not tie pin 1 ($\overline{\text{SENSE}}$) to power or ground.

Table 3. Pin Descriptions

ATT20C 478/477/475 Pin #	Symbol	Type	Name/Function
1	$\overline{\text{SENSE}}$ /NC	O	**$\overline{\text{SENSE}}$ (Active-Low).** TTL compatible. ATT20C477A/475A only. Monitor detection signal. $\overline{\text{SENSE}}$ is a logic 0 if one or more of the red, green, or blue outputs have exceeded the internal voltage reference level of 340 mV. $\overline{\text{SENSE}}$ may not be stable while SYNC is toggling. This pin has no internal connection on the ATT20C478A.
2	MODE	I	**MODE.** TTL compatible. Device function select. If MODE is a high value, the device operates as a ATT20C478A, 477A, or 475A. If MODE is low or unconnected, all devices operate as a 471 RAMDAC. In 471 mode, the command register is disabled (ATT20C477A/475A) and 6-bit color operation is selected. The ATT20C478A has hardware selectable, 8-bit color capability. The ATT20C477A has software or hardware selectable, 6-/8-bit color operation. The ATT20C477A/475A offer extra software-controlled capabilities such as powerdown, separate color sync, and SETUP control. See Table 4.
3, 24	GND	—	**Analog Ground.**
4, 20—22	Vcc	—	**Analog Power.**

Pin Information (continued)

Table 3. Pin Descriptions (continued)

ATT20C 478/477/475 Pin #	Symbol	Type	Name/Function
5	$\overline{\text{SYNC}}$	I	**$\overline{\text{SYNC}}$ (Active-Low).** TTL compatible. Latched on the rising edge of PCLK. For ATT20C478A/471 operation, SYNC removes a 7.62 mA (RS-343A) current source from each RGB output. For ATT20C477A/475A operation, each RGB output is controlled separately depending on the logic value of the color sync enable bits in the control register. For SYNC to operate properly, it should be asserted only during blanking. For systems having a sync signal separate from the RAMDAC, SYNC should be tied low to turn off the sync current source.
6	$\overline{\text{RD}}$	I	**Read (Active-Low).** TTL compatible. When $\overline{\text{RD}}$ is low, a data transfer from the selected internal register to the data bus takes place. The rising edge of the $\overline{\text{RD}}$ signal indicates the end of a read cycle.
7	$\overline{\text{BLANK}}$	I	**$\overline{\text{BLANK}}$ (Active-Low).** TTL compatible. $\overline{\text{BLANK}}$ is latched on the rising edge of PCLK. When $\overline{\text{BLANK}}$ is low, the 1.44 mA current source on the analog outputs will be turned off. The DACs ignore digital input from memory. The RAMDAC and overlay memory can be updated during blanking.
8—15	D[7:0]	I/O	**Data Bus.** TTL compatible. Data is transferred between the data bus and the internal registers under control of the $\overline{\text{RD}}$ / $\overline{\text{WR}}$ signal. In an MPU write operation, D[7:0] is latched on the rising edge of $\overline{\text{WR}}$. To read data D[7:0] from the device, $\overline{\text{RD}}$ must be in an active-low state. The rising edge of the $\overline{\text{RD}}$ signal indicates the end of a read cycle. Following the read cycle, the data bus will go to a high-impedance state. For 6-bit operation, color data is contained in the lower six bits of the data bus. D0 is the LSB and D5 is the MSB. When the MPU writes color data, D6 and D7 are ignored. During MPU read cycles, D6 and D7 are a logic 0.
16	$\overline{\text{WR}}$	I	**Write (Active-Low).** TTL compatible. $\overline{\text{WR}}$ controls the data transfer from the data bus to the selected internal register. D[7:0] data is latched at the rising edge of $\overline{\text{WR}}$, and RS[2:0] data is latched at the falling edge of $\overline{\text{WR}}$.
17—19	RS[2:0]	I	**Register Select.** TTL compatible. These inputs are sampled on the falling edge of the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ to determine which one of the internal registers is to be accessed.
23	SETUP	I	**SETUP.** TTL compatible. For the ATT20C478A, a low on this pin will shut off the blanking pedestal current. A logical high will cause a blanking pedestal of 1.44 mA on an RS-343A output level. For the ATT20C477A/475A, this pin is disabled while MODE is high. When MODE is low (471 RAMDAC functionality), this pin functions as described above for the ATT20C478A.
25 26 27	Red Green Blue	O	**Color Signals.** These pins are analog outputs. These high-impedance current sources are capable of driving a double-terminated 75 Ω coaxial cable.

Pin Information (continued)

Table 3. Pin Descriptions (continued)

ATT20C 478/477/475 Pin #	Symbol	Type	Name/Function
28	RSET	I	**Reference Resistor.** An external resistor (RSET) is connected between the RSET pin and GND to control the magnitude of the full-scale current. Refer to DAC Gain section under Functional Description.
29	COMP	I	**Compensation Pin.** Bypass this pin with an external 0.1 µF capacitor.
30	NC	—	**No Connect.** No internal connection to the chip.
31	V_{REF}	I	**Voltage Reference.** If an external voltage is used, it must supply this input with a 1.235 V reference.
32—39	P[7:0]	I	**Pixel Address.** TTL compatible. This pin is latched on the rising edge of PCLK. These inputs are masked by the pixel mask register and then used to specify one of the 256 addresses of the color RAM. The pixel address input is ignored when the overlay address bits are all nonzero. Unused inputs should be connected to GND.
40	PCLK	I	**Pixel Clock.** TTL compatible. The duty cycle of the clock should be between 30% and 70%. The rising edge of the pixel clock latches the pixel address, BLANK and SYNC inputs. The pixel clock controls the four-stage video pipelined operation.
41—44	OL[3:0]	I	**Overlay Address.** TTL compatible. These pins are latched on the rising edge of PCLK. These inputs are used to specify one of the 15 addresses of the color overlays. When the overlay address is non-zero, the pixel address inputs are ignored. Unused inputs should be connected to GND.

Functional Description

Table 4. Function Configuration for the ATT20C478A/477A/475A

The ATT20C478A/477A/475A can be configured for compatibility with devices of less functionality and performance.

Part Number	Function Change	Controlled By	Operational Change
ATT20C478A	478A → 471	MODE → Low	6-bit color only
ATT20C477A	477A → 471	MODE → Low	Control register disabled — 6-bit color only — No sleep mode — Blanking pedestal controlled by SETUP pin — Sync on all three (RGB) DACs
	477A → 475A	Control register bit CR1 → 0	6-bit color only
ATT20C475A	475A → 471	MODE → Low	Control register disabled — No sleep mode — Blanking pedestal controlled by SETUP pin — Sync on all three (RGB) DACs

Functional Description (continued)

Internal Registers

Table 5. Control Register

This register is present only in the ATT20C477A/475A. It is operational on powerup only while the MODE pin is a logic 1. It can be written to or read by the MPU at any time and is not initialized.

Bit	Name/Description
CR7	**Reserved.**
CR6	**Reserved.**
CR5	**SETUP Select.** Logic 0: No blanking pedestal current. Logic 1: Blanking pedestal current. This bit is logically ANDed with the MODE pin. When MODE is logic 1 (ATT20C477A/475A functionality), the SETUP pin is disabled and bit CR5 controls the blanking (SETUP) pedestal. When MODE is a logic zero, the SETUP pin controls the blanking pedestal and bit CR5 is disabled (471 mode). For VGA operation, tie the ATT20C477A/475A SETUP pin to logic 0, and write a logic 0 to bit CR5.
CR4 CR3 CR2	**Sync Enable.** Logic 0: Sync disabled. Logic 1: Sync enabled. Bits CR4, CR3, and CR2, respectively specify whether the blue, green, or red outputs will have sync offset current. A logic 1 specifies sync current. The sync currents enabled by CR4, CR3, and CR2 are controlled by the $\overline{\text{SYNC}}$ pin. For noncomposite sync, tie the $\overline{\text{SYNC}}$ pin to logic 0.
CR1	**6-/8-bit Select.** ATT20C477A only. The value of CR1 is ignored in the ATT20C475A. Logic 0: 6 bit. Logic 1: 8 bit. A logic 1 specifies 8-bit color operation. A logic 0 specifies 6-bit color operation.
CR0	**Sleep Enable.** Logic 0: Normal operation. Logic 1: Sleep mode. If this bit is logic 0, the device will be in normal operation. If this bit is logic 1, the DAC is turned off and the palette RAM is powered down. The RAM retains data and will wake up to accept inputs from the MPU port. After accepting MPU data, the RAM returns to the sleep state. After programming the device for normal operation, valid data will appear at the DAC outputs in about one second.

Functional Description (continued)

MPU Interface

The ATT20C478A/477A/475A support a standard MPU interface, allowing the MPU direct access to the RAMDAC RAM, overlay color registers, or control register (see Figure 1).

As outlined in Table 6, the RS[2:0] select inputs indicate whether.the MPU is accessing the address register, RAMDAC RAM, overlay registers, read mask register, or control register. To eliminate the requirement for external address multiplexers, the 8-bit address register is used to address the RAMDAC RAM and overlay registers. ADDR0 corresponds to D0 and is the least significant bit.

Writing the RAMDAC

The MPU writes the address register (RAM write mode) with the address of the RAMDAC RAM location to be modified. Using RS[2:0] to select the RAMDAC RAM, the MPU completes three continuous write cycles (6 or 8 bits each of red, green, and blue). Following the blue write cycle, the 3 bytes of color information are concatenated into an 18- or 24-bit word and written to the location specified by the address register. The address register advances to the next location which the MPU can modify by simply writing another sequence of red, green, and blue data. A block of color values in successive locations can be written to by writing the start address and performing continuous R, G, and B write cycles until the entire block has been written.

Reading the RAMDAC

The MPU loads the address register (RAM read mode) with the address of the RAMDAC RAM location to be read. The contents of the RAMDAC RAM at the specified address are copied into the RGB registers, and the address register advances to the next RAM location. Using RS[2:0] to select the RAMDAC RAM, the MPU completes three continuous read cycles (6 or 8 bits each of red, green, and blue). After the blue read cycle, the contents of the RAMDAC RAM at the address specified by the address register are copied into the RGB registers, and the address register advances to the next address. A block of color values in successive locations can be read by writing the start address and performing continuous R, G, and B read cycles until the entire block has been read.

Writing the Overlay Registers

The MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. Using RS[2:0] to select the overlay registers, the MPU completes three continuous write cycles (6 or 8 bits each of red, green, and blue). Following the blue write cycle, the 3 bytes of color information are concatenated into an 18- or 24-bit word and written to the overlay location specified by the address register. The address register then advances to the next location which the MPU can modify by simply writing another sequence of red, green, and blue data. A block of color values in successive locations can be written to by writing the start address and performing continuous R, G, and B write cycles until the entire block has been written.

Table 6. Control Input Truth Table

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (RAM write mode)
0	1	1	address register (RAM read mode)
0	0	1	RAMDAC RAM
0	1	0	pixel read mask register
1	0	0	address register (overlay write mode)
1	1	1	address register (overlay read mode)
1	0	1	overlay registers
1	1	0	control register (ATT20C477A/475A only)

Functional Description (continued)

Reading the Overlay Registers

The MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers, and the address register advances to the next overlay location. Using RS[2:0] to select the overlay registers, the MPU completes three continuous read cycles (6 or 8 bits each of red, green, and blue). Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers, and the address register advances to the next address. A block of color values in successive locations can be read by writing the start address and performing continuous R, G, and B read cycles until the entire block has been read.

Additional Information

Following a blue read or write cycle to RAM location $FF, the address register resets to $00. The four most significant bits of the address register ADDR[7:4] are ignored while accessing the overlay color registers.

Operation of the MPU interface occurs asynchronously to the pixel clock. Internal logic synchronizes data transfers between the RAMDAC RAM/overlay registers and the R, G, B color subregister. The transfers occur between MPU accesses. As a result, the $\overline{WR}$ and $\overline{RD}$ signals must maintain a logic high for several clock cycles. See the ac timing characteristics under $\overline{RD}$ and $\overline{WR}$ high time for further information. To eliminate sparkling on the CRT screen during MPU access to the RAMDAC RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between look-up table RAMs and the RGB registers occurs.

To monitor the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 7. They are reset to 0 when the MPU writes to the address register, and are not reset to 0 when the MPU reads the address register. The MPU does not have access to these bits.

The other 8 bits of the address register ADDR[7:0], incremented following a blue read or write cycle, are accessible to the MPU and are used to address RAMDAC RAM locations and overlay registers, as outlined in Table 8.

The MPU can read the address register at any time without modifying its contents or the existing read/write mode. Note that the pixel clock must be active for MPU accesses to the RAMDAC RAM.

If the MODE input is a logic 1, the command register is available (ATT20C477A/475A). On the ATT20C477A, the 6- or 8-bit select in the command register can be used to specify whether 6- or 8-bit color data values are being used.

471 RAMDAC Compatible Operation

The ATT20C478A/477A/475A operate as a 471 RAMDAC, without a current reference, if the MODE pin is logic 0 (see Table 2). This active-low signal disables the command register (ATT20C477A/475A) and selects 6-bit operation. Color data is on the lower 6 bits of the data bus, with D0 being the LSB and D5, the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be logic 0. Note that in the 6-bit mode, the ATT20C478A/477A full-scale output current will be about 1.5% lower than when in the 8-bit mode. This is a result of the two LSBs of each 8-bit DAC always being a logic 0 in the 6-bit mode.

When the ATT20C477A/475A are in the 471 RAMDAC mode (MODE pin = 0), the $\overline{SENSE}$ output pin still functions. Therefore, do not tie $\overline{SENSE}$ to power or ground.

Table 7. Modulo Counter Operation

Value	Addressed by MPU
00	red value
01	green value
10	blue value

Table 8. Address Register (ADDR) Operation

RS2	RS1	RS0	Address	Addressed by MPU
0	0	1	$00–$FF	RAMDAC RAM
1	0	1	$X0	reserved
1	0	1	$X1	overlay color 1
:	:	:	:	:
1	0	1	$XF	overlay color 15

Functional Description (continued)

6-/8-bit Color Resolution

Bit D0 is the color data LSB, and bit D7 is the MSB in the 8-bit color mode. While operating in the 6 bits per color mode, the lower 6 bits of the data bus contain the color data, with D0 being the LSB and D5, the MSB. When writing color data, D6 and D7 are ignored, and during color read cycles, D6 and D7 are zero.

Pixel and Overlay Pins

Table 9 outlines how the P[7:0] and OL[3:0] inputs address the RAMDAC RAM and overlay registers. The contents of the pixel read mask register, which can be accessed by the MPU at any time, are bit-wise logically ANDed with the P[7:0] inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 18 bits ATT20C475A or 24 bits ATT20C478A/477A of color information to the three D/A converters.

To maintain synchronization with color data, the rising edge of the clock latches the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs. $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ add appropriately weighted currents to the analog outputs to produce the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ pedestal currents as shown in Figures 3, 4, and 5 and Tables 11, 12, and 13.

The MODE input pin is logically ANDed with the SETUP control bit CR5, and is used to specify whether a 0 IRE or 7.5 IRE blanking pedestal is to be used. When MODE is high, the SETUP pin is disabled. When MODE is low, bit CR5 is disabled.

The analog outputs of the ATT20C478A/477A/475A are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

Powerdown (ATT20C477A/475A only)

The SLEEP command bit controls the powerdown in the ATT20C477A/475A. The device operates normally while the sleep bit is a logic 0. A logic 1 in the command register SLEEP bit turns off power to the RAM and the DACs. The RAM still retains the data and can still be read or written to while sleeping, as long as the pixel clock is running. The RAM automatically powers up during MPU read/write cycles, and shuts down when the MPU access is completed. The ATT20C477A/475A disable all references both internal and external to the device, preventing current from flowing out of the device during powerdown. The internal reference disable circuitry eliminates the need for external disable logic and allows minimum power dissipation during sleep mode, regardless of the referencing scheme used.

$\overline{\text{SENSE}}$ Output (ATT20C477A/475A only)

$\overline{\text{SENSE}}$ is a logic 0 if one or more of the red, green, and blue outputs have exceeded the internal voltage reference level (340 mV). This output is used to determine the presence of a CRT monitor, and, via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The 340 mV reference has a ±40 mV tolerance. Note that $\overline{\text{SYNC}}$ should be a logic 0 for $\overline{\text{SENSE}}$ to be stable.

Table 9. Pixel and Overlay Control Truth Table

(Condition: Pixel Read Mask Register = $FF)

OL[3:0]	P[7:0]	Addressed by Frame Buffer
$0	$00	RAMDAC RAM location $00
$0	$01	RAMDAC RAM location $01
:	:	:
$0	$FF	RAMDAC RAM location $FF
$1	$XX	overlay color 1
:	$XX	:
$F	$XX	overlay color 15

Functional Description (continued)

DAC Gain

The device gain from the voltage reference to the DAC output current is shown below. To set the full-scale white current on the DACs while using an internal or external voltage reference, use the formula below.

V_{REF} is the voltage reference in volts, K is the gain constant from Table 10, and RSET is the resistor connected between the RSET pin and ground. Find the recommended RSET in Table 10.

I_{OUT} (mA) = [V_{REF} (V) * 1,000 * K] / RSET (Ω)

Table 10. I_{OUT} Current

Output Waveform Level	RS-343A	*PS/2*	K Factor
Black to White (6 bit)	17.6 mA	14.25 mA	2.1
Black to White (8 bit)	17.6 mA	14.25 mA	2.125
Black to $\overline{\text{BLANK}}$	1.4 mA	—	0.1667
$\overline{\text{BLANK}}$ to $\overline{\text{SYNC}}$	7.6 mA	6.1 mA	0.9
Recommended RSET	147 Ω	182 Ω	—

In this case, a voltage reference of 1.235 V with RSET = 147 Ω and a K factor of 3.17 results in I_{OUT} = 26.63 mA. A 6-bit DAC with no sync or blank results in a K factor of 2.1 and I_{OUT} = 17.64 mA.

As shown in Table 10, the recommended RSET for RS-343A compatibility applications (doubly terminated 75 Ω) is 147 Ω. The recommended RSET for *PS/2* applications (50 Ω) is 182 Ω.

Functional Description (continued)

NO $\overline{\text{SYNC}}$		$\overline{\text{SYNC}}$	
mA	V	mA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000

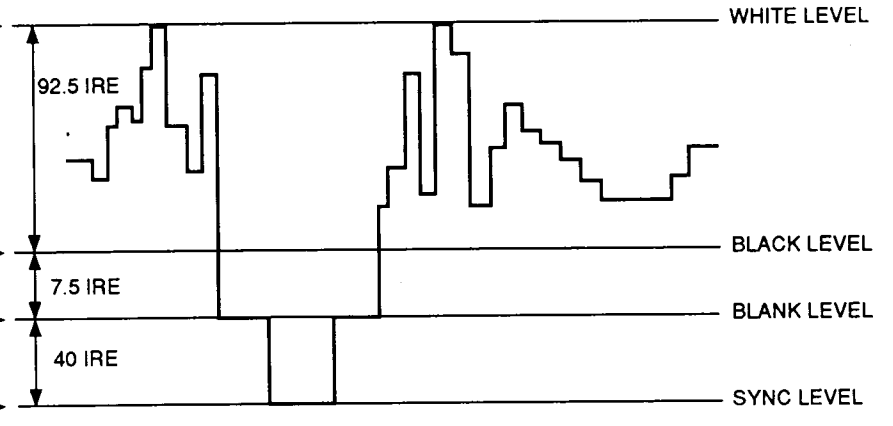


Figure 3. RS-343A Composite Video Output Waveforms

Table 11. RS-343A Video Output Truth Table (Blank offset current to equal 7.5 IRE)

DAC Input Data	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	Output Level	I_{OUT} (mA) $\overline{\text{SYNC}}$ Disabled	I_{OUT} (mA) $\overline{\text{SYNC}}$ Enabled
$FF	1	1	WHITE	19.05	26.67
data	1	1	DATA	data + 1.44	data + 9.05
data	0	1	DATA- $\overline{\text{SYNC}}$	data + 1.44	data + 1.44
$00	1	1	BLACK	1.44	9.05
$00	0	1	BLACK- $\overline{\text{SYNC}}$	1.44	1.44
$XX	1	0	$\overline{\text{BLANK}}$	0	7.62
$XX	0	0	$\overline{\text{SYNC}}$	0	0

Note: 75 Ω doubly terminated load, SETUP = 7.5 IRE. V_{REF} = 1.235 V, RSET = 147 Ω.

Functional Description (continued)

NO $\overline{\text{SYNC}}$		$\overline{\text{SYNC}}$	
mA	V	mA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000

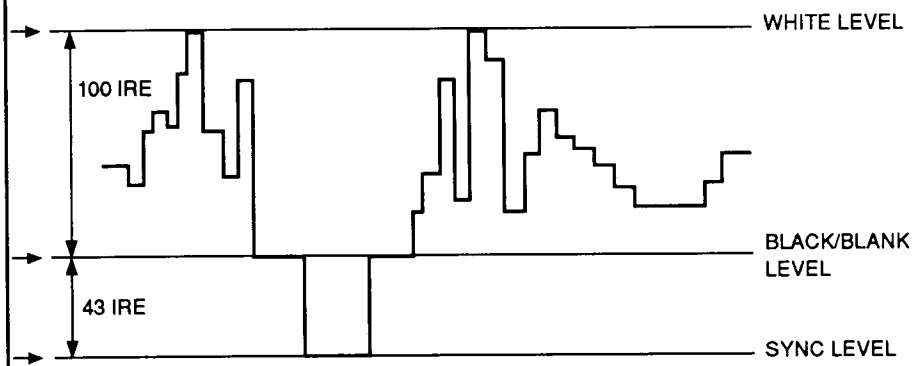


Figure 4. RS-343A Composite Video Output Waveforms

Table 12. RS-343A Video Output Truth Table (No blank offset current)

DAC Input Data	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	Output Level	I_{OUT} (mA) $\overline{\text{SYNC}}$ Disabled	I_{OUT} (mA) $\overline{\text{SYNC}}$ Enabled
$FF	1	1	WHITE	17.62	25.24
data	1	1	DATA	data	data + 7.62
data	0	1	DATA- $\overline{\text{SYNC}}$	data	data
$00	1	1	BLACK	0	7.62
$00	0	1	BLACK- $\overline{\text{SYNC}}$	0	0
$XX	1	0	$\overline{\text{BLANK}}$	0	7.62
$XX	0	0	$\overline{\text{SYNC}}$	0	0

Note: 75 Ω doubly terminated load, SETUP = 0 IRE. V_{REF} = 1.235 V, RSET = 147 Ω.

Functional Description (continued)

NO $\overline{\text{SYNC}}$		$\overline{\text{SYNC}}$	
mA	V	mA	V
14.25	0.713	20.36	1.018
0.00	0.000	6.11	0.305
0.00	0.000	0.00	0.000

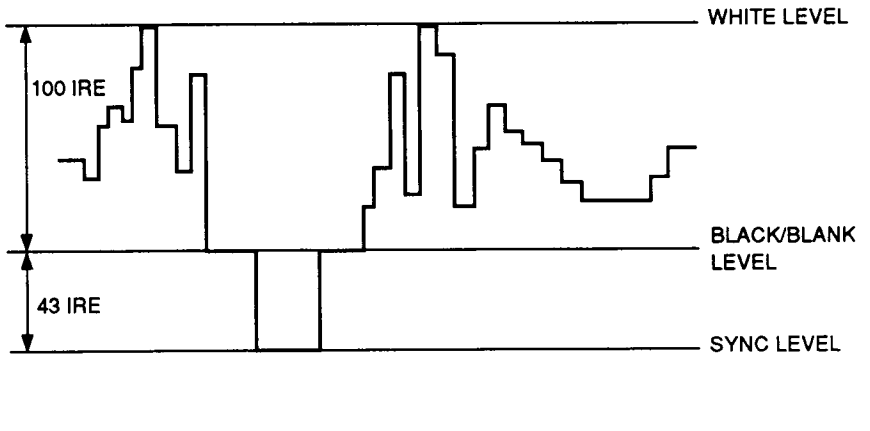


Figure 5. *PS/2* Composite Video Output Waveforms

Table 13. *PS/2* Video Output Truth Table

DAC Input Data	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	Output Level	$\overline{\text{SYNC}}$ Disabled I_{OUT} (mA)	$\overline{\text{SYNC}}$ Enable I_{OUT} (mA)
$FF	1	1	WHITE	14.25	20.36
data	1	1	DATA	data	data + 6.11
data	0	1	DATA- $\overline{\text{SYNC}}$	data	data
$00	1	1	BLACK	0	6.11
$00	0	1	BLACK- $\overline{\text{SYNC}}$	0	0
$XX	1	0	$\overline{\text{BLANK}}$	0	6.11
$XX	0	0	$\overline{\text{SYNC}}$	0	0

Note: 50 Ω load, SETUP = 0 IRE. V_{REF} = 1.235 V, RSET = 182 Ω.

Application Information

Board Layout

Careful configuration and placement of supply planes, components, and signal traces ensure a low-noise board. This helps ensure proper functionality and low signal emissions in restricted frequency bands as mandated by regulatory agencies.

A 4-layer PC board with separate power and ground planes will likely result in a board with quieter signals and supplies as well as less spectral content in emitted frequency bands. The board should have signal layers 1 and 4 (outside layers) and supply layers 2 and 3 (inside layers). Use a solid ground plane for frequencies up to 100 MHz.

The ATT20C478A/477A/475A parts should be placed close to the video output connector and between the video output connector and the edge card connector. This will keep the high-speed DAC output traces short and minimize the amount of circuitry between the RAMDAC and the supply pins on the edge card connector.

Power Distribution

Separate the power plane into digital and analog areas. Place all digital components over the digital plane and all analog components over the analog plane. The analog components include the RAMDAC, reference circuitry, comparators, all mixed signal chips (such as a clock synthesizer), and any passive support components for analog circuits.

The analog and digital power plane should be connected with at least one ferrite bead across the separation as illustrated in Figures 6 and 7. This bead provides resistance to high-frequency currents. Select a ferrite bead with an impedance curve suitable for your design. The ferrite should have a resistance at a higher frequency than the maximum signal frequency on the board, but lower than the second harmonic (2x) of that frequency. The following beads provide resistances of approximately 75 Ω at 100 MHz: Ferroxcube VK20019-4B, Fair-Rite 2743001111, or Philips 431202036690.

Decoupling Capacitors

All decoupling capacitors should be located within 0.25 in. of the device to be decoupled. Chip capacitors are recommended, but radial and axial leads will work. Keep lead lengths as short as possible to reduce inductance and EMI. For leaded capacitors, use devices with a self-resonance above the pixel clock frequency.

For the ATT20C478A/477A/475A RAMDACs, decouple Vcc pins 20, 21, and 22 to ground with C2. Decouple Vcc pin 4 to ground with C3. For higher frequency pixel clocks (>80 MHz), use a 0.001 µF capacitor in parallel with the 0.1 µF capacitor to shunt the higher frequency noise to ground. Power supply noise should be <200 mV for a good design. About 10% of any noise below 1 MHz will be coupled onto the DAC outputs. As illustrated in Figures 6 and 7, the COMP pin should also be decoupled with a 0.1 µF capacitor. For designs showing ghosting or smearing, add a parallel COMP capacitance of 2.2 µF.

Digital Signals

The digital inputs should not travel over the analog power plane if possible. The RAMDAC should be located over the analog plane close to the digital/analog supply separation. The RAMDAC may also be placed over the supply separation so the digital pixel inputs are over the digital supply plane. The digital inputs, especially the P[7:0] high-speed inputs, should be isolated from the analog outputs. Placing the digital inputs over the digital supply reduces coupling into the analog supply plane. High-speed signals (both analog and digital) should not be routed under the RAMDAC.

Avoid high slew rate edges, as they can contribute to undershoot, overshoot, ringing, EMI, and noise feedthrough. Wherever possible, use slower edge rate (3 ns—5 ns) logic such as 74LS or 74ALS devices. If this is not possible, edges can be slowed down using series termination (75 Ω to 150 Ω). Edge noise will result if the digital signal propagates from an impedance mismatch while the signal rises. The reflection noise is particularly troublesome in the TTL threshold region. For a 2 ns edge, the trace length must be less than 4 in.

Application Information (continued)

Digital Signals (continued)

The clock signal trace should be as short as possible and should not run parallel to any high-speed signals. To ensure a quality clock signal without high-frequency noise components, decouple the supply pins on the clock driver. If necessary, transmission line techniques should be used on the clock by providing controlled impedance striplines and parallel termination.

Analog Signals

The load resistor should be as close as possible to the DAC outputs. The resistor should equal the destination termination which is usually a 75 Ω monitor. Unused analog outputs should be connected to ground. The DAC output traces should be as short as possible to minimize any impedance mismatch in the trace or video connector. Series ferrite beads can be added to the analog video signal to reduce high-frequency signals coupled onto the DAC outputs or reflected from the monitor.

To reduce the interaction of the analog video return current with board components, a separate video ground return trace can be added to the ground plane or signal layer. This trace connects directly to the point that ground enters the card.

DAC Outputs

The ATT20C478A/477A/475A analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching ac coupled monitors.

The diode protection circuit shown in Figures 6 and 7 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes.

Application Information (continued)

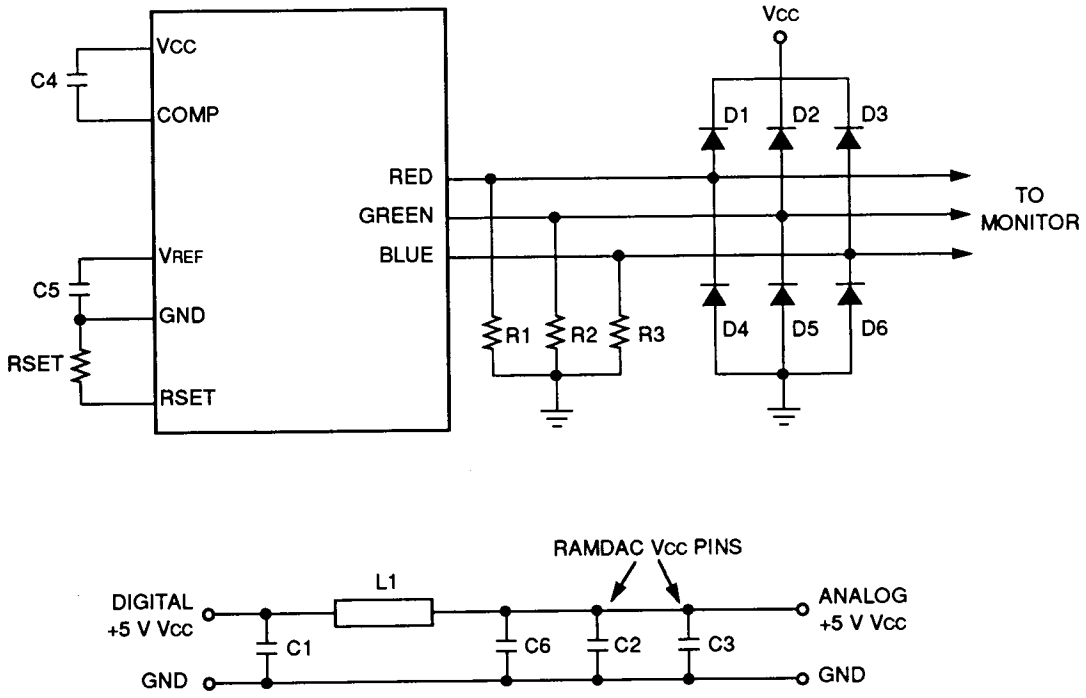


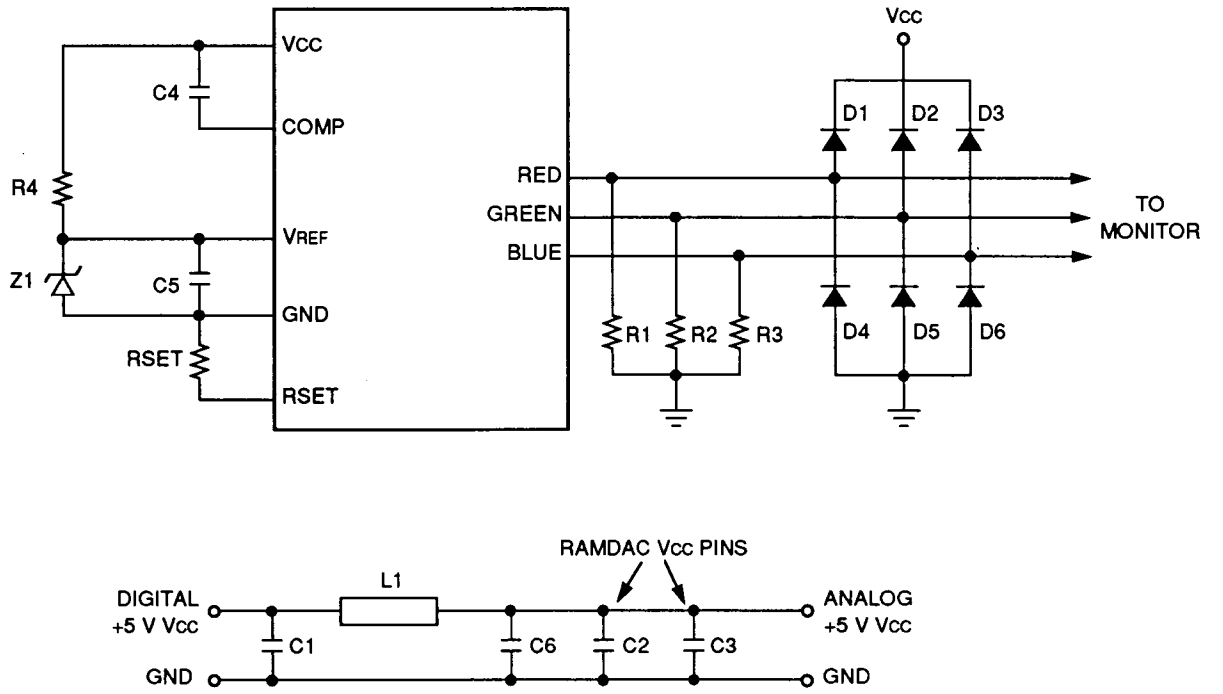
Figure 6. Typical Connection Diagram for Internal Voltage Reference

Table 14. Internal Voltage Reference Parts List

Location	Description	Vendor Part Number
C1—C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	Ferrite bead	Fair-Rite 2743001111
R1—R3	75 Ω, 1% metal film resistor	Dale CMF-55C
RSET	147 Ω, 1% metal film resistor	Dale CMF-55C
D1—D6	Fast-switching diodes	National 1N4148/49

Note: The above vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the ATT20C478A/477A/475A.

Application Information (continued)



* VREF pin internally disabled when ATT20C477A/475A is powered down.

Figure 7. Typical Connection Diagram for External Voltage Reference

Table 15. External Voltage Reference Parts List

Location	Description	Vendor Part Number
C1—C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	Ferrite bead	Fair-Rite 2743001111
R1—R3	75 Ω, 1% metal film resistor	Dale CMF-55C
R4	1 kΩ, 5% resistor	—
RSET	147 Ω, 1% metal film resistor	Dale CMF-55C
Z1	1.2 voltage reference	National Semiconductor LM385BZ-1.2
D1—D6	Fast-switching diodes	National 1N4148/49

Note: The above vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the ATT20C478A/477A/475A.

Application Information (continued)

Multiple RAMDACs

Each device should have its own power plane and ferrite bead when using multiple ATT20C478A/477A/475A devices. Use the internal voltage references rather than a single external reference to achieve less color channel crosstalk and RAMDAC interaction.

Each ATT20C478A/477A/475A device must still have its own individual RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} (measured to GND)	—	—	—	7.0	V
Voltage on any Digital Pin	—	GND – 0.5	—	V_{CC} + 0.5	V
Analog Output Short Circuit: Duration to any Power Supply or Common	ISC	—	indefinite	—	—
Ambient Operating Temperature	T_A	–55	—	125	°C
Storage Temperature	T_{stg}	–65	—	150	°C
Junction Temperature	T_J	—	—	150	°C
Vapor Phase Soldering (60 s)	TV_{SOL}	—	—	220	°C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply (MHz):					
66/80	V_{CC}	4.5	5.0	5.5	V
100/110	V_{CC}	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	0	—	70	°C
Output Load	R_L	—	37.5	—	Ω
Voltage Reference Configuration: Reference Voltage	V_{REF}	1.2	1.235	1.27	V

Electrical Characteristics

Table 16. dc Characteristics

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = 7.5 IRE, MODE pin = logic 1. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

Parameter	Symbol	Min	Typ	Max	Unit
Resolution (each DAC):					
ATT20C475A	—	6	6	6	bits
ATT20C478A/477A	—	6	—	8	bits
Accuracy (each DAC):					
Integral Linearity Error:	IL	—	—	—	—
ATT20C475A	—	—	—	±1/4	LSB
ATT20C478A/477A	—	—	—	±1	LSB
Differential Linearity Error:	DL	—	—	—	—
ATT20C475A	—	—	—	±1/4	LSB
ATT20C478A/477A	—	—	—	±1	LSB
Gray Scale Error	—	—	—	±5	% Gray
Monotonicity	—	—	guaranteed	—	Scale
Coding	—	—	—	—	Binary
Digital Inputs:					
Input Voltage:					
Low	V_{IL}	GND – 0.5	—	0.8	V
High	V_{IH}	2.0	—	Vcc + 0.5	V
Input Current:					
Low (V_{IN} = 0.4 V)	I_{IL}	—	—	–1	µA
High (V_{IN} = 2.4 V)	I_{IH}	—	—	1	µA
Capacitance (f = 1 MHz, V_{IN} = 2.4 V)	C_{IN}	—	—	7	pF
Digital Outputs:					
Output Voltage:					
Low (I_{OL} = 3.2 mA)	V_{OL}	—	—	0.4	V
High (I_{OH} = –400 µA)	V_{OH}	2.4	—	—	V
3-State Current	I_{OZ}	—	—	50	µA
Capacitance	C_{DOUT}	—	—	7	pF

Electrical Characteristics (continued)

Table 16. dc Characteristics (continued)

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = 7.5 IRE, MODE pin = logic 1. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

Parameter	Symbol	Min	Typ	Max	Unit
Analog Outputs:					
Gray Scale Current Range	—	—	—	20	mA
Output Current:					
White Level Relative to Black*	—	16.74	17.62	18.50	mA
Black Level Relative to Blank:					
Setup = 7.5 IRE	—	0.95	1.44	1.90	mA
Setup = 0 IRE	—	0	5	50	µA
Blank Level:					
Sync Enabled	—	6.29	7.62	8.96	mA
Sync Disabled	—	0	5	50	µA
Sync Level	—	0	5	50	µA
LSB Size:					
ATT20C475A	—	—	279.68	—	µA
ATT20C478A/477A	—	—	69.1	—	µA
DAC to DAC Matching	—	—	2	5	%
Output Compliance	V_{OC}	−1.0	—	+1.5	V
Output Impedance	RA_{OUT}	—	10	—	kΩ
Output Capacitance (f = 1 MHz, I_{OUT} = 0 mA)	CA_{OUT}	—	—	30	pF
Internal Reference Output (±3%)	V_{REF}	1.2	1.235	1.27	V
Power Supply Rejection Ratio (COMP = 0.1 F, f = 1 kHz)	PSRR	—	—	0.5	%/% ΔVcc
	—	—	—	−6	dB

* Since the ATT20C475A has 6-bit DACs (and the ATT20C477A in the 6-bit mode), the output levels are approximately 1.5% lower than these values.

Electrical Characteristics (continued)

Table 17. ac Characteristics

Test conditions (unless otherwise specified): Recommended operating conditions using external voltage reference with RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = 7.5 IRE, MODE (47X/ $\overline{471}$) pin = logic 1. TTL level input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF, $\overline{SENSE}$, D[7:0] output load ≤50 pF. The parameters are applicable over the full voltage and temperature range as shown in the Recommended Operating Conditions table.

		110 MHz Devices			100 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Clock Rate	fmax	—	—	110	—	—	100	MHz
RS[2:0] Setup Time	1	10	—	—	10	—	—	ns
RS[2:0] Hold Time	2	10	—	—	10	—	—	ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5	—	—	5	—	—	ns
$\overline{RD}$ Asserted to Data Valid	4	—	—	30	—	—	30	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5	—	—	20	—	—	20	ns
Read Data Hold Time	6	5	—	—	5	—	—	ns
Write Data Setup Time	7	10	—	—	10	—	—	ns
Write Data Hold Time	8	10	—	—	10	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	4	—	—	4	—	—	PCLK
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10, 11	6	—	—	6	—	—	PCLK
Pixel and Control Setup Time	12	2	—	—	2	—	—	ns
Pixel and Control Hold Time	13	2	—	—	2	—	—	ns
Clock Cycle Time	14	9.1	—	—	10	—	—	ns
Clock Pulse Width High Time	15	3	—	—	3	—	—	ns
Clock Pulse Width Low Time	16	3	—	—	3	—	—	ns
Analog Output Delay	17	—	—	30	—	—	30	ns
Analog Output Rise/Fall Time	—	—	3	—	—	3	—	ns
Analog Output Settling Time*	—	—	10	—	—	10	—	ns
Clock and Data Feedthrough*	—	—	-30	—	—	-30	—	dB
Glitch Impulse*	—	—	75	—	—	75	—	pV-s
DAC to DAC Crosstalk	—	—	-23	—	—	-23	—	dB
Analog Output Skew	18	—	—	2	—	—	2	ns
$\overline{SENSE}$ Output Delay	—	—	1	—	—	1	—	µs
Pipeline Delay	—	4	4	4	4	4	4	Clocks
V_{CC} Supply Current†: Normal Operation	I_{CC}	—	115	175	—	110	175	mA
Sleep Mode‡ (ATT20C477A/475A)	ISLP	—	3	5	—	3	5	mA

* Clock and data feedthrough are functions of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74 HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough. –3 dB test bandwidth = 2 x clock rate.

† At fmax, I_{CC} (typ) at V_{CC} = 5.0 V I_{CC} (max) at V_{CC} (max).

‡ External voltage reference automatically disabled during sleep mode. Test conditions: 25 °C to 70 °C. Pixel and data ports at 0.4 V.

Electrical Characteristics (continued)

Table 17. ac Characteristics (continued)

Test conditions (unless otherwise specified): Recommended operating conditions using external voltage reference with RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = 7.5 IRE, MODE (47X/ $\overline{471}$) pin = logic 1. TTL level input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF, $\overline{SENSE}$, D[7:0] output load ≤50 pF. The parameters are applicable over the full voltage and temperature range as shown in the Recommended Operating Conditions table.

		80 MHz Devices			66 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Clock Rate	fmax	—	—	80	—	—	66	MHz
RS[2:0] Setup Time	1	10	—	—	10	—	—	ns
RS[2:0] Hold Time	2	10	—	—	10	—	—	ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5	—	—	5	—		ns
$\overline{RD}$ Asserted to Data Valid	4	—	—	40	—	—	40	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5	—	—	20	—	—	20	ns
Read Data Hold Time	6	5	—	—	5	—	—	ns
Write Data Setup Time	7	10	—	—	10	—	—	ns
Write Data Hold Time	8	10	—	—	10	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	4	—	—	4	—	—	PCLK
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10, 11	6	—	—	6	—	—	PCLK
Pixel and Control Setup Time	12	3	—	—	3	—	—	ns
Pixel and Control Hold Time	13	3	—	—	3	—	—	ns
Clock Cycle Time	14	12.5	—	—	15.15	—	—	ns
Clock Pulse Width High Time	15	4	—	—	5	—	—	ns
Clock Pulse Width Low Time	16	4	—	—	5	—	—	ns
Analog Output Delay	17	—	—	30	—	—	30	ns
Analog Output Rise/Fall Time	—	—	3	—	—	3	—	ns
Analog Output Settling Time*	—	—	13	—	—	13	—	ns
Clock and Data Feedthrough*	—	—	–30	—	—	–30	—	dB
Glitch Impulse*	—	—	75	—	—	75	—	pV-s
DAC to DAC Crosstalk	—	—	–23	—	—	–23	—	dB
Analog Output Skew	18	—	—	2	—	—	2	ns
$\overline{SENSE}$ Output Delay	—	—	1	—	—	1	—	µs
Pipeline Delay	—	4	4	4	4	4	4	Clocks
Vcc Supply Current†: Normal Operation	Icc	—	105	160	—	100	160	mA
Sleep Mode‡ (ATT20C477A/475A)	ISLP	—	3	5	—	3	5	mA

* Clock and data feedthrough are functions of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74 HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough. –3 dB test bandwidth = 2 x clock rate.

† At fmax, Icc (typ) at Vcc = 5.0 V Icc (max) at Vcc (max).

‡ External voltage reference automatically disabled during sleep mode. Test conditions: 25 °C to 70 °C. Pixel and data ports at 0.4 V.

Electrical Characteristics (continued)

Table 17. ac Characteristics (continued)

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operation condition for generating test signals is RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = 7.5 IRE, 8/$\overline{6}$ pin = logic 1. The parameters are applicable over the full voltage and temperature range as shown in the Recommended Operating Conditions table.

		50 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Clock Rate	fmax	—	—	50	MHz
RS[2:0] Setup Time	1	10	—	—	ns
RS[2:0] Hold Time	2	10	—	—	ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5	—	—	ns
$\overline{RD}$ Asserted to Data Valid	4	—	—	40	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5	—	—	20	ns
Read Data Hold Time	6	5	—	—	ns
Write Data Setup Time	7	10	—	—	ns
Write Data Hold Time	8	10	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	4	—	—	PCLK
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10, 11	6	—	—	PCLK
Pixel and Control Setup Time	12	3	—	—	ns
Pixel and Control Hold Time	13	3	—	—	ns
Clock Cycle Time	14	20	—	—	ns
Clock Pulse Width High Time	15	6	—	—	ns
Clock Pulse Width Low Time	16	6	—	—	ns
Analog Output Delay	17	—	—	30	ns
Analog Output Rise/Fall Time	—	—	3	—	ns
Analog Output Settling Time*	—	—	20	—	ns
Clock and Data Feedthrough*	—	—	–30	—	dB
Glitch Impulse*	—	—	75	—	pV-s
DAC to DAC Crosstalk	—	—	–23	—	dB
Analog Output Skew	18	—	—	2	ns
$\overline{SENSE}$ Output Delay	—	—	1	—	µs
Pipeline Delay	—	4	4	4	Clocks
V_{CC} Supply Current†: Normal Operation	I_{CC}	—	100	160	mA
Sleep Mode‡ (ATT20C477A/475A)	ISLP	—	3	5	mA

* Clock and data feedthrough are functions of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74 HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough. –3 dB test bandwidth = 2 x clock rate.

† At fmax, I_{CC} (typ) at V_{CC} = 5.0 V I_{CC} (max) at V_{CC} (max).

‡ External voltage reference automatically disabled during sleep mode. Test conditions: 25 °C to 70 °C. Pixel and data ports at 0.4 V.

Timing Characteristics

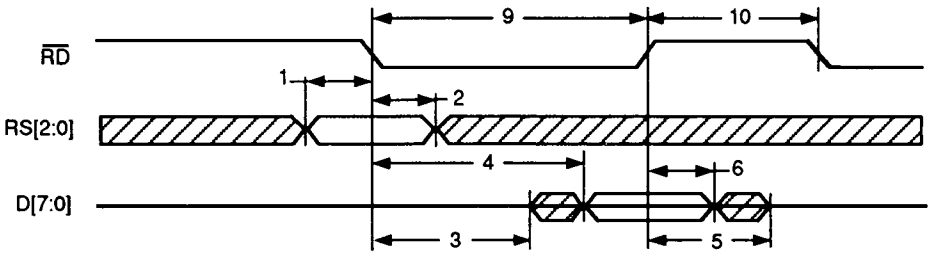


Figure 8. Basic Read-Cycle Timing Diagram

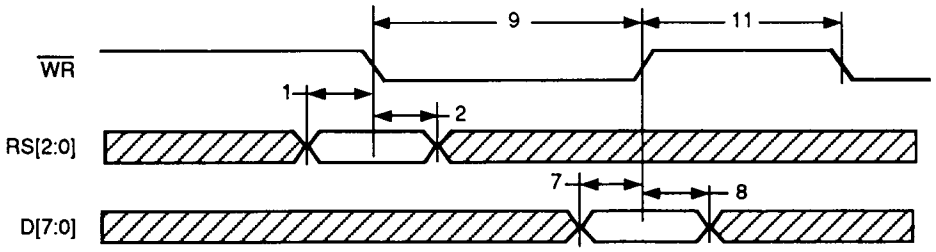


Figure 9. Basic Write-Cycle Timing Diagram

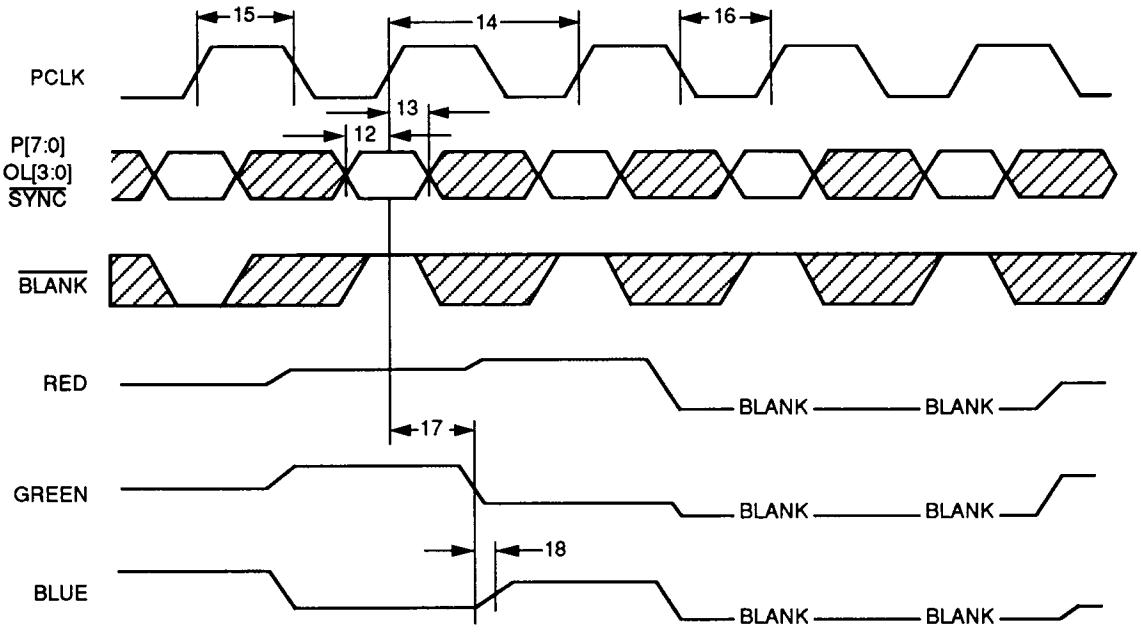


Figure 10. Pixel and Video Control Timing

Timing Characteristics (continued)

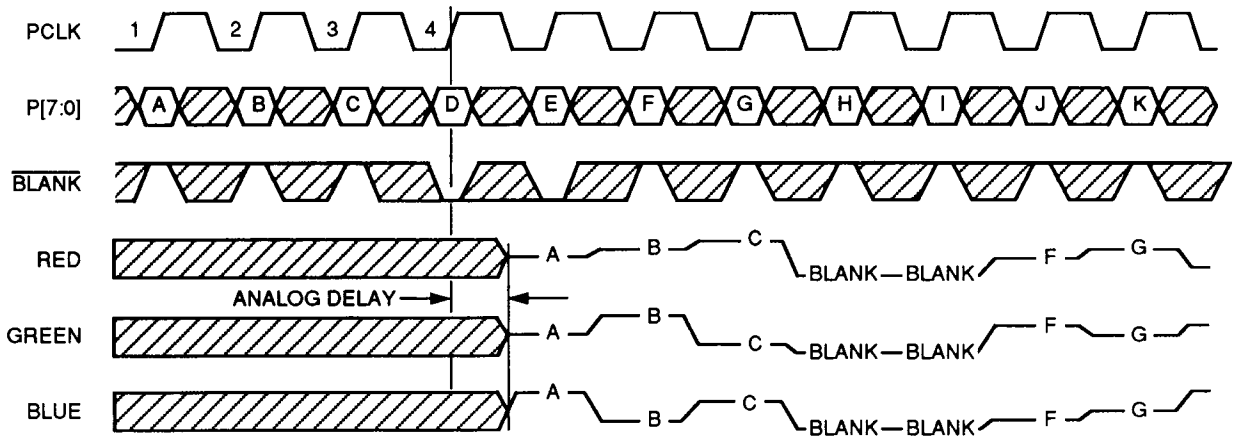


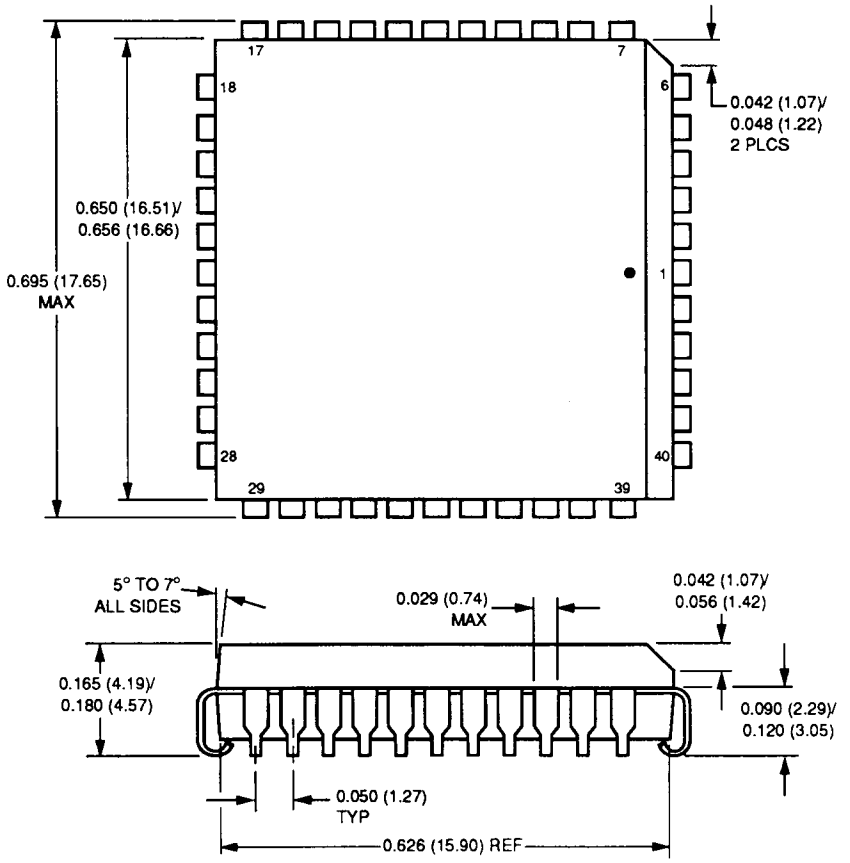
Figure 11. System Timing Diagram: Pixel Pipeline

Outline Diagram

44-Pin PLCC Package

Top View.

Dimensions are in inches and (millimeters).



Ordering Information

Device*	Speed	Package Type
ATT20C478A-XXM44	110/100/80/66/50 MHz	44-Pin PLCC
ATT20C477A-XXM44	110/100/80/66/50 MHz	44-Pin PLCC
ATT20C475A-XXM44	110/100/80/66/50 MHz	44-Pin PLCC

*XX refers to speed grade:
11 = 110 MHz
10 = 100 MHz
80 = 80 MHz
66 = 66 MHz
50 = 50 MHz

Revision History

Table 18. Updates to ATT20C478A/477A/475A Data Sheet

The following table outlines and identifies the updates to the *ATT20C478A/477A/475A CMOS RAMDACs* Data Sheet.

Date	Description	Pages Revised
August 1991	First relaease	—
March 1992	— Added 50 MHz speed grade. — Text updated on page 6 under pixel address. The pixel address input is ignored when the overlay address bits are all **nonzero**. — Revised table references on page 8 for Tables 7 and 8. — Deleted Table 18, Read and Write Pulse Width High Time (see Table 17). — Minor text revisions; not affecting operation or specifications. — Added revision history.	1, 3, 4, 6, 8, 9, 15, 17, 18, 19, 24, and 27

For additional information, contact your AT&T Account Manager or the following:
U.S.A.: AT&T Microelectronics, Dept. AL-520404200, 555 Union Boulevard, Allentown, PA 18103
1-800-372-2447, FAX 215-778-4106 (In CANADA: **1-800-553-2448,** FAX 215-778-4106)
EUROPE: AT&T Microelectronics, AT&T Deutschland GmbH, Bahnhofstr. 27A, D-8043 Unterfoehring, Germany
Tel. (49) 89 95086-0, FAX (49) 89 95086-331
ASIA PACIFIC: AT&T Microelectronics Asia/Pacific, 14 Science Park Drive, #03-02A/04 The Maxwell, Singapore 0511
Tel. (65) 778-8833, FAX (65) 777-7495, Telex RS 42898 ATTM
JAPAN: AT&T Microelectronics, AT&T Japan Ltd., 31-11, Yoyogi 1-chome, Shibuya-ku, Tokyo 151, Japan
Tel. (03) 5371-2700, FAX (03) 5371-3556
SPAIN: AT&T Microelectronica de España, Poligono Industrial de Tres Cantos (Zona Oeste), 28770 Colmenar Viejo, Madrid, Spain
Tel. (34) 1-8071441, FAX (34) 1-8071420

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