

DATA SHEET

BSP106

N-channel enhancement mode
vertical D-MOS transistor

Product specification
File under Discrete Semiconductors, SC13b

April 1995

N-channel enhancement mode vertical D-MOS transistor

BSP106

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line transformer drivers.

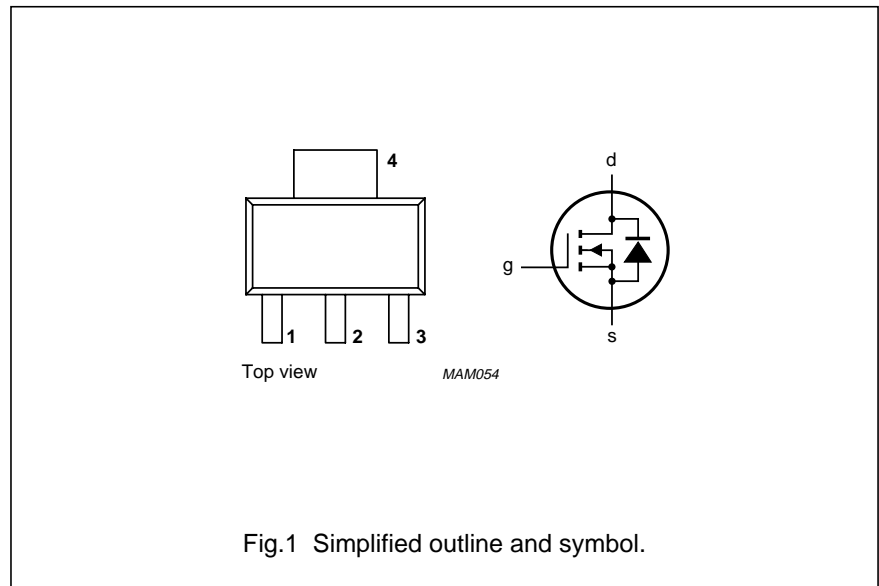
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage	–	60	V
I_D	drain current	DC value	425	mA
$R_{DS(on)}$	drain-source on-resistance	$I_D = 200 \text{ mA}$ $V_{GS} = 10 \text{ V}$	4	Ω
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$ $V_{GS} = V_{DS}$	3	V

PIN CONFIGURATION



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LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
V_{DG}	drain-gate voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage		–	20	V
I_D	drain current	DC value	–	425	mA
I_{DM}	drain current	peak value	–	850	mA
P_{tot}	total power dissipation	up to $T_{amb} = 25\text{ °C}$ (note 1)	–	1.5	W
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm;
mounting pad for the drain lead minimum 6 cm².

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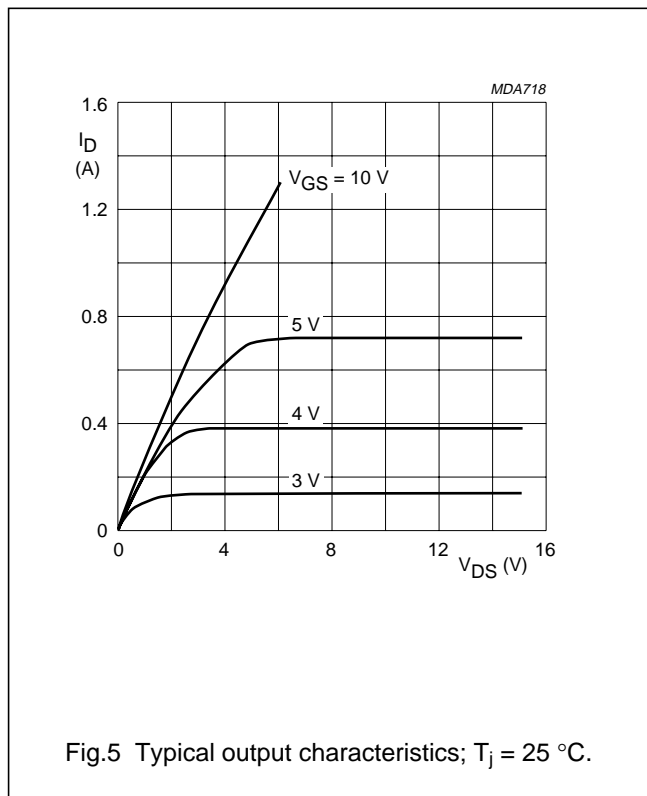
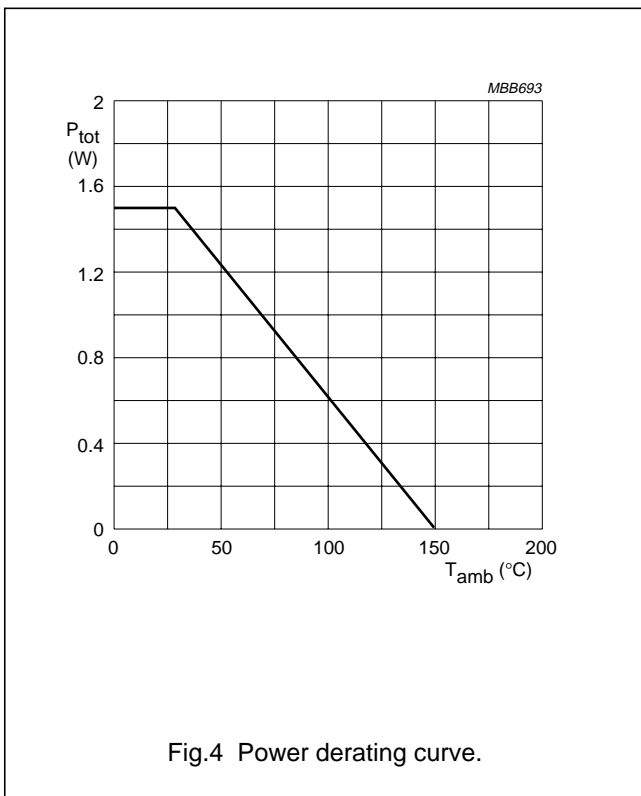
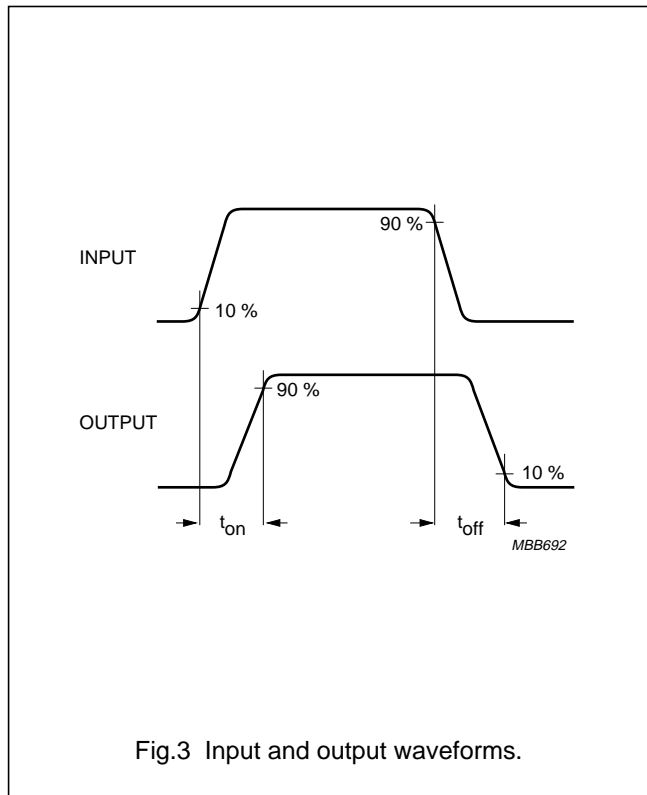
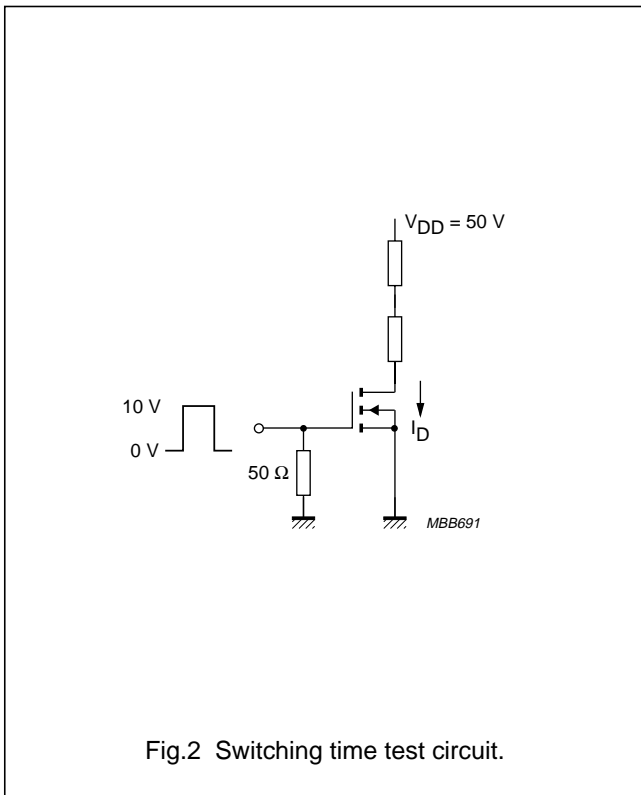
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CHARACTERISTICS $T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\ \mu\text{A}$ $V_{GS} = 0$	60	90	–	V
I_{DSS}	drain-source leakage current	$V_{DS} = 48\ \text{V}$ $V_{GS} = 0$	–	–	1	μA
		$V_{DS} = 25\ \text{V}$ $V_{GS} = 0$	–	–	0.5	μA
$\pm I_{GSS}$	gate-source leakage current	$V_{DS} = 0$ $\pm V_{GS} = 15\ \text{V}$	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$ $V_{GS} = V_{DS}$	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	$I_D = 200\ \text{mA}$ $V_{GS} = 10\ \text{V}$	–	2.5	4	Ω
$ Y_{fs} $	transfer admittance	$I_D = 200\ \text{mA}$ $V_{DS} = 10\ \text{V}$	100	200	–	mS
C_{iss}	input capacitance	$V_{DS} = 10\ \text{V}$ $V_{GS} = 0$ $f = 1\ \text{MHz}$	–	25	40	pF
C_{oss}	output capacitance	$V_{DS} = 10\ \text{V}$ $V_{GS} = 0$ $f = 1\ \text{MHz}$	–	22	30	pF
C_{rss}	feedback capacitance	$V_{DS} = 10\ \text{V}$ $V_{GS} = 0$ $f = 1\ \text{MHz}$	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$I_D = 200\ \text{mA}$ $V_{DD} = 50\ \text{V}$ $V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	2	5	ns
t_{off}	turn-off time	$I_D = 200\ \text{mA}$ $V_{DD} = 50\ \text{V}$ $V_{GS} = 0\ \text{to}\ 10$	–	10	15	ns

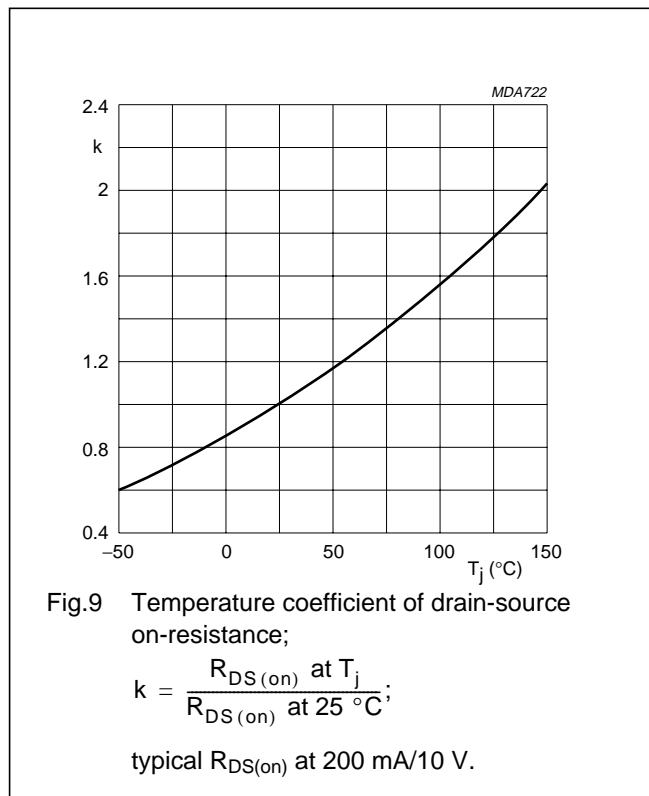
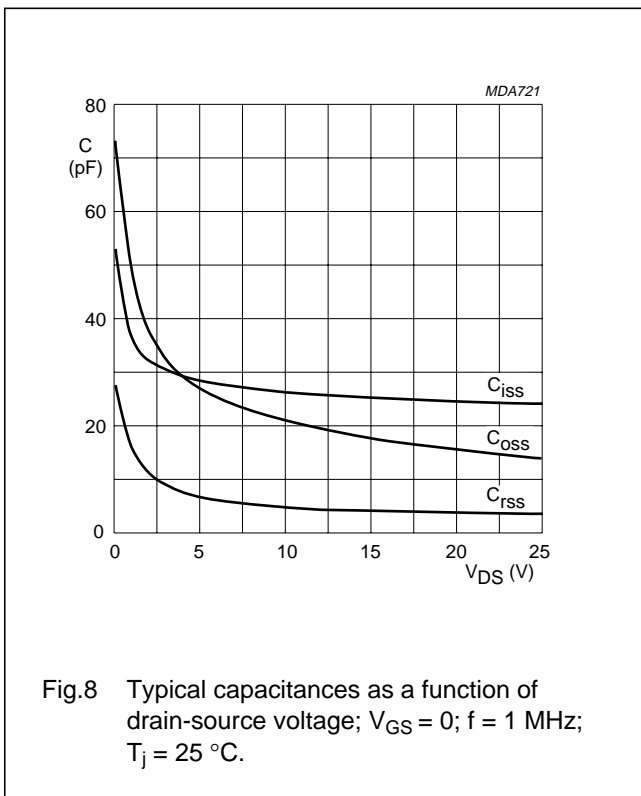
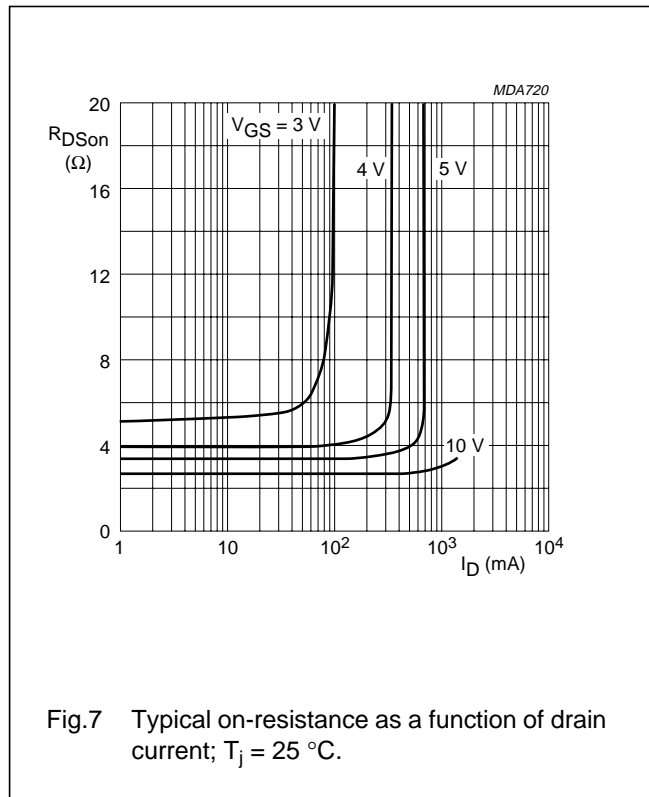
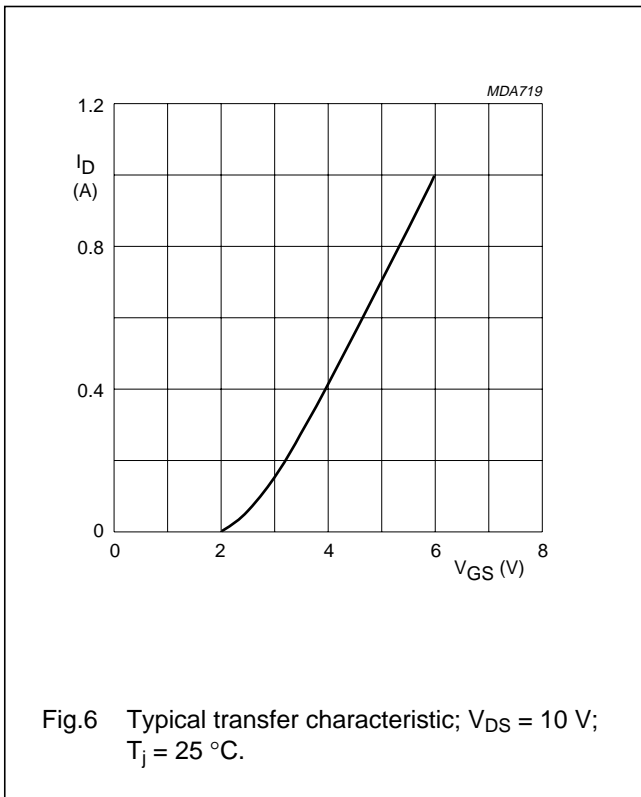
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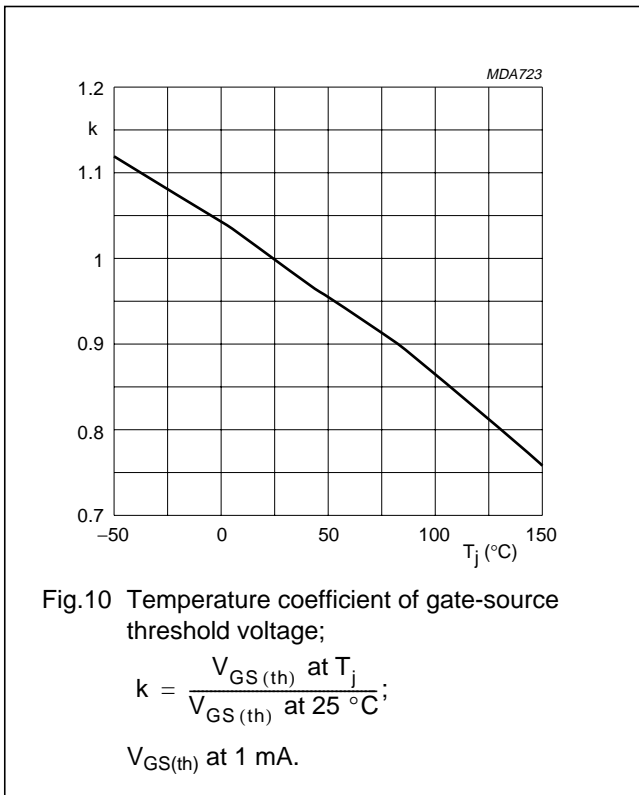
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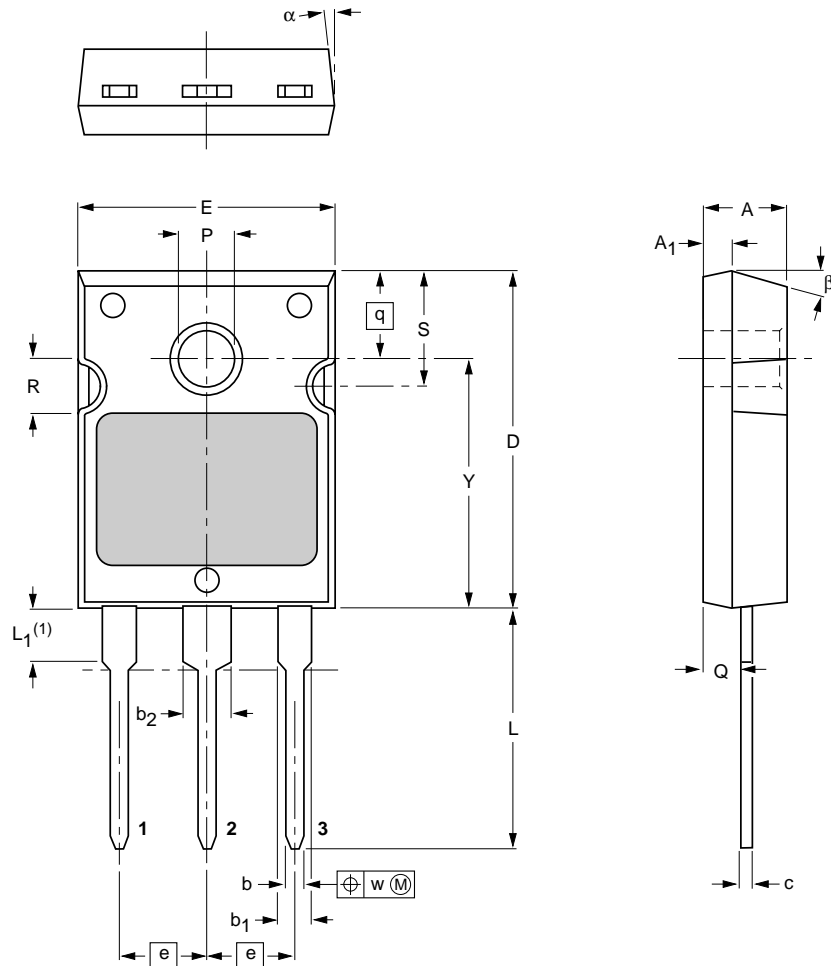
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PACKAGE OUTLINES

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-247

SOT429



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	b ₂	c	D	E	e	L	L ₁ ⁽¹⁾	P	Q	q	R	S	w	Y	α	β
mm	5.3 4.7	1.9 1.7	1.2 0.9	2.2 1.8	3.2 2.8	0.9 0.6	21 20	16 15	5.45	16 15	4.0 3.6	3.7 3.3	2.6 2.4	5.3	3.5 3.3	7.5 7.1	0.4	15.7 15.3	6° 4°	17° 13°

Note

1. Tinning of terminals are uncontrolled within zone L₁.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT429		TO-247				98-03-24

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BSP106**DEFINITIONS**

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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Printed in The Netherlands

137107/00/01/pp12

Date of release: April 1995

Document order number: 9397 750 02466

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