Spread Spectrum Clock Synthesizer for Desktop Pentium II

Features

- Up to 112 MHz operation
- Spread Spectrum Modulation for CPUCLK, and PCICLK
- Two copies of CPU clock with V_{DD} of 2.5V ±5%
- Seven copies of PCI clock, (synchronous with CPU clock) 3.3V
- One copy of Ref. clock @ 14.31818MHz (3.3V_{TTL})
- 48MHz USB Clock, 24MHz Super I/O clock
- I^2C Serial Configuration Interface
- Low cost 14.31818MHz crystal oscillator input
- Power management control
- Isolated core V_{DD}, V_{SS} pins for noise reduction
- 28-pin SSOP (H) and SOIC package (S)

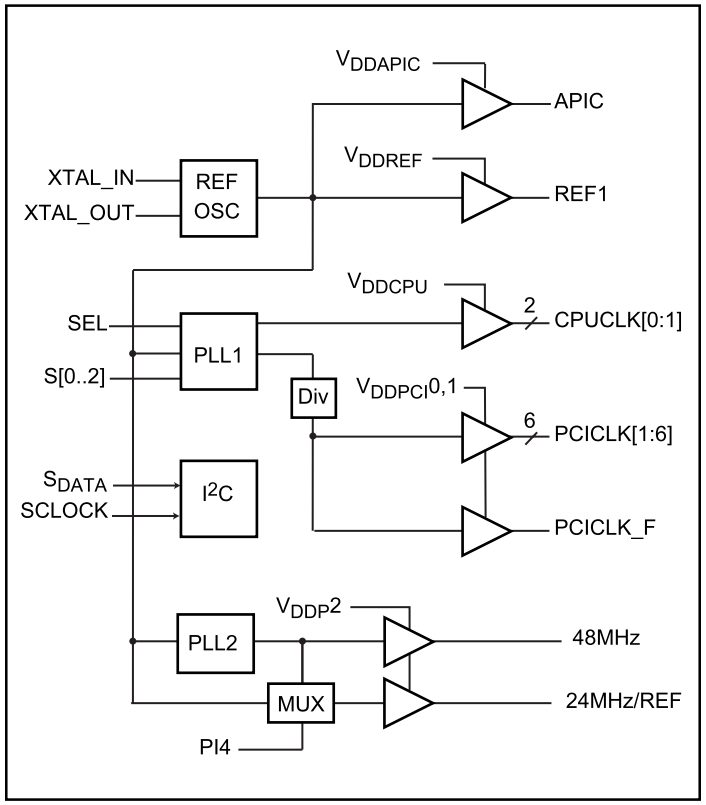
Description

The PI6C104 is a high-speed low-noise clock generator designed to work with the PI6C18X family of clock buffer to meet all clock needs for Desktop Intel Architecture platforms. CPU and chipset clock frequencies from 66.6 MHz to 112 MHz are supported.

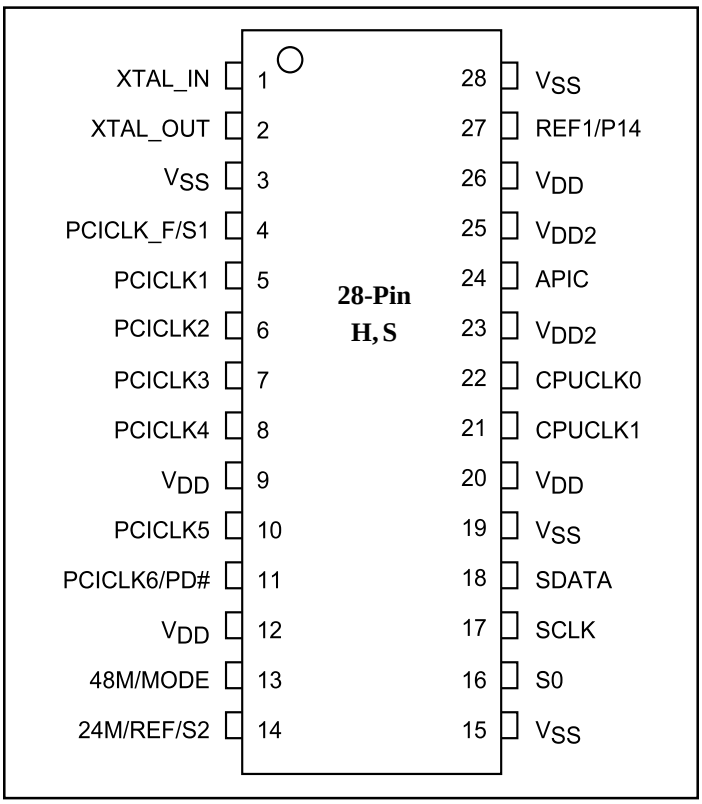
Split supplies of 3.3V and 2.5V are used. The 3.3V power supply powers a portion of the I/O and the core. The 2.5V is used to power the remaining outputs (CPU and APIC). 2.5V signaling follows JEDEC standard 8-X. Power sequencing of the 3.3V and 2.5V supplies is not required.

An asynchronous PD# signal may be used to orderly power down (or up) the system during power on.

Block Diagram



Pin Configuration



Pin Description

Pin	Signal Name	Type	Qty.	Description
1	XTAL_IN	XI	1	14.318 MHz crystal input
2	XTAL_OUT	XO	1	14.318 MHz crystal input
4	PCICLK_F	O	1	Free running PCI clock output.
	S1	I+PU		Frequency Select bit 1
				During power up this pin is S1 input, PCICLK_F output otherwise
5,6,7,8,10	PCICLK[1:5]	O	5	PCI clock outputs.
11	PCICLK6	O	1	PCI clock outputs.
	PD#	I+PU		Active low Power Down input. PCI and CPU clocks are disabled when PD# is low, except for PCICLK_F
				This pin is set by MODE (pin 13). MODE = 0: PD# input, MODE = 1: PCICLK6 output
13	48M	O	1	48 MHz output
	MODE	I+PU		MODE determines the definition of pin 11, 0=PD# input, 1=PCICLK6 output
				This is a an input, sampled during power up. Becomes 48 MHz output after power up
14	24M	O	1	24 MHz output
	REF	O		Buffered Reference output.
	S2	I+PU		Frequency Select bit 2.
				During power up this pin is S2 input, output otherwise. P14 (pin 27) mode selects: 0 = REF, 1 = 24 MHz
16	S0	I+PU	1	Frequency Select bit 0
17	SCLK	I+PU	1	Serial Clock for I^2C interface
18	SDATA	IO+PU	1	Serial Data for I^2C interface
21,22	CPUCLK[0:1]	O	2	CPU clock output
24	APIC	O	1	Buffered Crystal output.
27	REF1	O	1	Buffered Crystal output.
	P14	1	1	Pin 14 mode select, 0 = REF1, 1 = 24 MHz
				During power up this pin is P14 input, REF1 output otherwise.
9,12,20,26	V_{DD}		4	Power supply for PCI, Core, REF, PLL. 3.3V
23,25	V_{DD2}		2	Power supply for APIC & CPU clocks. 2.5V
3,15,19,28	V_{SS}		4	Grounds

Clock Enable Configuration

PD#	CPUCLK[0:1]	PCICLK[1:5]	PCICLK_F	Other Clocks	Crystal	VCO's
0	low	low	Running	Running	Running	Running
1	Running	Running	Running	Running	Running	Running

PI6C104 I^2C Address Assignment 0D2H

A7	A6	A5	A4	A3	A2	A1	A0
1	1	0	1	0	0	1	0

Frequency Table				
S0	S1	S2	CPU	PCI
0	0	0	75	30
0	0	1	66.8	33.4
0	1	0	66.6	33.3
0	1	1	66.8	33.4
1	0	0	112	37.3
1	0	1	83.3	33.3
1	1	0	100	33.3
1	1	1	100	33.3

2-Wire I^2C Control

The I^2C interface permits individual enable/disable of each clock output and test mode enable.

The PI6C104 is a slave receiver device. It can not be read back. Sub addressing is not supported. All preceding bytes must be sent in order to change one of the control bytes.

Every byte put on the SDATA line must be 8-bits long (MSB first), followed by an acknowledge bit generated by the receiving device. During normal data transfers SDATA changes only when SCLK is LOW. Exceptions: A HIGH to LOW transition on SDATA while SCLK is HIGH indicates a "start" condition. A LOW to HIGH transition on SDATA while SCLK is HIGH is a "stop" condition and indicates the end of a data transfer cycle.

Each data transfer is initiated with a start condition and ended with a stop condition. The first byte after a start condition is always a 7-bit address byte followed by a read/write bit. (HIGH = read from addressed device, LOW = write to addressed device).

If the device's own address is detected, PI6C104 generates an acknowledge by pulling SDATA line LOW during ninth clock pulse, then accepts the following data bytes until another start or stop condition is detected.

Following acknowledgement of the address byte (D2), two more bytes must be sent:

1. "Command Code" byte, and

2. "Byte Count" byte.

Although the data bits on these two bytes are "don't care," they must be sent and acknowledged.

Byte 3 : Frequency, Spread Spectrum

Bit #	Pup	Pin #	Name	Description		
7	0	~	RSVD	Reserved		
6		~	S0	Frequency Select Bit 0		
5		~	S1	Frequency Select Bit 1		
4		~	S2	Frequency Select Bit 2		
3		~	SFS	0 = Hardware Frequency Select 1 = Software Frequency Select (1^2C reg.)		
2		~	RSVD	Reserved		
1		~	MODE1	Mode Bit 1		
0		~	MODE0	Mode Bit 0		
				M1	M0	
				0	0	Spread Spectrum Off
				0	1	Test Mode
				1	0	Spread Spectrum On
				1	1	Hi-Z

Byte 4 : Clock Controls (1 = Enabled, 0 = Disabled)

Bit #	Pup	Pin #	Name	Description
7	0	~	RSVD	Reserved
6		~		
5		~		
4		~		
3		~		
2	1	21	CPU1EN	CPUCLK1 Enable, Default is Enable
1	0	~	RSVD	Reserved
0	1	22	CPU0EN	CPUCLK0 Enable, Default is Enable

Byte 5 : PCI Clock Control (1 = Enabled, 0 = Disabled)

Bit #	Pup	Pin #	Name	Description
7	1	4	PCIFEN	PCI_F Enable, Default is Enable
6	0	11	PCI6EN	PCI6 Enable, Default is Enable
5	1	10	PCI5EN	PCI5 Enable, Default is Enable
4	0	~	~	Reserved
3	1	8	PCI4EN	PCI4 Enable, Default is Enable
2		7	PCI3EN	PCI3 Enable, Default is Enable
1		6	PCI2EN	PCI2 Enable, Default is Enable
0		5	PCI1EN	PCI1 Enable, Default is Enable

Byte 6 : REF Clock Control (1 = Enabled, 0 = Disabled)

Bit #	Pup	Pin #	Name	Description
7	0	~	RSVD	Reserved
6		~	RSVD	Reserved
5		24	APICEN	APIC Enable, Default is Enable
4		~	RSVD	Reserved
2	1	~	RSVD	Reserved
1		26	RFEN1	REF1 High drive Enable 1
0		26	RFEN0	REF1 High drive Enable 0
				RFEN1 RFEN0
				0 0
	Low Drive			0 1
	Normal Drive, Default			1 0
	High Drive			1 1

Note: Outputs are disabled @ low state

Table 1: Byte 3 Frequency and Spread Spectrum Table

Bit3 SFS	Bit1 SSEN	Bit6 S0	Bit5 S1	Bit4 S2	CPU(MHz)	PCI(MHz)	Spread (%)
1	0	0	0	0	75	30	OFF
1	0	0	0	1	66.8	33.4	OFF
1	0	0	1	0	66.6	33.3	OFF
1	0	0	1	1	66.8	33.4	OFF
1	0	1	0	0	112	37.3	OFF
1	0	1	0	1	83.3	33.3	OFF
1	0	1	1	0	100	33.3	OFF
1	0	1	1	1	100	33.3	OFF
1	1	0	0	0	75	30	-0.5~+0.5
1	1	0	0	1	66.8	33.4	-0.9~+0.9
1	1	0	1	0	66.6	37.3	-1.0~+0.0
1	1	0	1	1	66.8	33.4	-0.5~+0.5
1	1	1	0	0	112	37.3	-0.5~+0.5
1	1	1	0	1	83.3	33.3	-0.5~+0.5
1	1	1	1	0	100	33.3	-1~+0.0
1	1	1	1	1	100	33.3	-0.5~+0.0

Notes:
Bit 3 = Enable Software Frequency Select
Bit 1 = Enable Software Frequency Select
Bit 6 = Frequency Select 0
Bit 5 = Frequency Select 1
Bit 4 = Frequency Select 0

Byte 0: Test Mode Table

Bit 1	Bit 0	CPU	PCI	48M	24M	REF/APIC	Mode
0	0	table 1	table 1	48MHz	24 MHz/Ref	14.318MHz	Normal
0	1	Xin/2	Xin/6	Xin/2	Xin/4	Xin	Test
1	0	table 1	table 1	48MHz	24 MHz/Ref	14.318MHz	SSC
1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Tri-state

Power Management Timing

When MODE = 0, the device supports power management and pin 11 is input PD#. When MODE = 1, this function is not available). A particular output is enabled only when both the I^2C serial interface and this pin indicate that it should be enabled. The clocks may be disabled according to the following table in order to reduce the power consumption. All clocks are stopped in the low state.

All clocks maintain a valid high period on transitions from running to stopped. The CPU and PCI clocks transition between running and stopped by waiting for one positive edge on PCI_F followed by a negative edge on the clock of interest, after which high levels of the outputs are either enabled or disabled. See Figure 1 below.

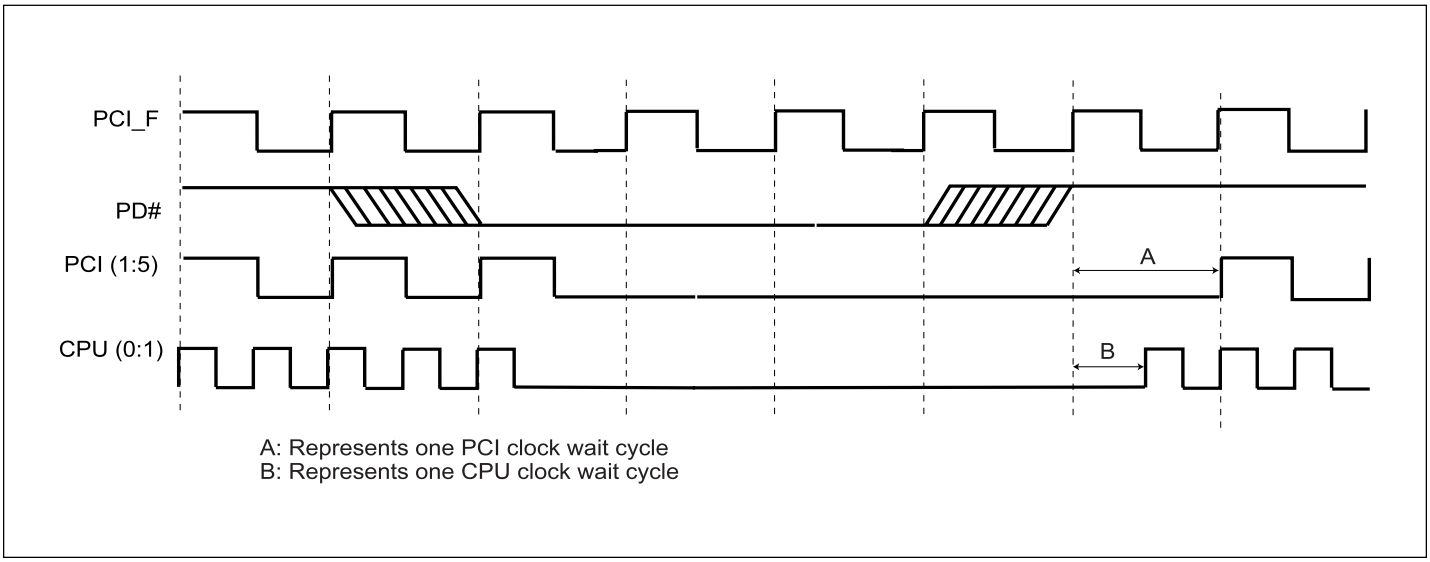


Figure 1. PD# Timing Diagram

Note:

1. Please note that all clocks can also be individually (asynchronously) enabled or stopped via the 2-wire I^2C control interface. In this case all clocks are stopped in the low state.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–0°C to +70°C
3.3V Supply Voltage to Ground Potential	–0.5V to +4.6V
2.5V Supply Voltage to Ground Potential	–0.5V to +3.6V
DC Input Voltage	–0.5V to +4.6V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (V_{DD} = +3.3V ± 5%, V_{DD2} = +2.5V ± 5%, T_A = 0°C to +70°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
I_{DD2}	2.5V Current	V_{DD2} = 2.625V, PD# = 0 CLOAD = Max.			100	µA
I_{DD2}		V_{DD2} = 2.625V @ 66.66MHz CLOAD = Max.			72	mA
I_{DD2}		V_{DD2} = 2.625V @ 100MHz CLOAD = Max.			100	
I_{DD}	3.3V Current	V_{DD} = 3.465V, PD# = 0 CLOAD = Max.			500	µA
I_{DD}		V_{DD} = 3.465V @ 66.66MHz CLOAD = Max.			170	mA
I_{DD}		V_{DD} = 3.465V @ 100MHz CLOAD = Max.			170	

DC Operating Specifications

Symbol	Parameters	Conditions	Min.	Max.	Units
Input Voltage, V_{DD} = 3.3V ± 5%					
V_{IH3}	Input high voltage	V_{DDCORE}	2.0	V_{DDCORE} +0.3	V
V_{IL3}	Input low voltage		V_{SS} -0.3	0.8	
I_{IL}	Input leakage current	$0 < V_{IN} < V_{DDCORE}$	-5	+5	µA
Output Voltage, V_{DD2} = 2.5V ± 5%					
V_{OH}	Output high voltage	I_{OH} = -1mA	2.0		V
V_{OL}	Output low voltage	I_{OL} = 1mA		0.4	
Output Voltage, V_{DD} = 3.3V ± 5%					
V_{OH}	Output high voltage	I_{OH} = -1mA	2.4		V
V_{OL}	Output low voltage	I_{OL} = 1mA		0.4	
Output Voltage, V_{DD} = 3.3V ± 5%					
V_{POH}	PCI Bus output high voltage	I_{OH} = -1mA	2.4		V
V_{POL}	PCI Bus output low voltage	I_{OL} = 1mA		0.55	
C_{IN}	Input pin capacitance			5	pF
C_{XTAL}	Xtal pins capacitance	13.5	18.0	22.5	
C_{OUT}	Output pin capacitance			6	
L_{PIN}	Pin Inductance			7	nH
T_A	Ambient Temperature	No airflow	0	70	°C

Buffer Specifications

V_{DD} Range(V)	Impedance (Ω)	Buffer Type
2.375 -2.625	13.5 - 45	Type 1
3.135 - 3.465	12 - 55	Type 5

Type 1: 2.5V Clock Buffers

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	V_{OUT} = 1.0V	-27			mA
I_{OHMAX}	Pull-up current	V_{OUT} = 2.375V			-27	
I_{OLMIN}	Pull-down current	V_{OUT} = 1.2V	27			
I_{OLMAX}	Pull-down current	V_{OUT} = 0.3V			30	
t_{RH}	2.5V Type 1 output rise edge rate	2.5V ± 5% @ 0.4V-2.0V	1		4	V/ns
t_{FH}	2.5V Type 1 output fall edge rate	2.5V ± 5% @ 2.0V-0.4V	1		4	

Type 5: 3.3V Clock Buffers

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	V_{OUT} = 1.0V	-33			mA
I_{OHMAX}	Pull-up current	V_{OUT} = 3.135V			-33	
I_{OLMIN}	Pull-down current	V_{OUT} = 1.95V	30			
I_{OLMAX}	Pull-down current	V_{OUT} = 0.4V			38	
t_{RH}	3.3V Type 5 output rise edge rate	3.3V ± 5% @ 0.4V-2.4V	1		4	V/ns
t_{FH}	3.3V Type 5 output fall edge rate	3.3V ± 5% @ 2.4V-0.4V	1		4	

AC Timing

Figure 1. Host Clock to PCI CLK Offset	Parameters	66 MHz		100 MHz		Units
		Min.	Max.	Min.	Max.	
t_{HKP} (2.5V)	Host CLK period	15.0	15.5	10.0	10.5	ns
t_{HKH} (2.5V)	Host CLK high time	5.2		3.0		
t_{HKL} (2.5V)	Host CLK low time	5.0		2.8		
t_{HRISE} (2.5V)	Host CLK rise time	0.4	1.6	0.4	1.6	
t_{HFALL} (2.5V)	Host CLK fall time	0.4	1.6	0.4	1.6	
t_{JITTER} (2.5V)	Host CLK Jitter		250		250	ps
Duty Cycle (2.5V)	Measured at 1.25V	45	55	45	55	%
t_{HSKW} (2.5V)	Host Bus CLK Skew		175		175	ps
t_{PZL}, t_{PZH}	Output enable delay	1.0	8.0	1.0	8.0	ns
t_{PLZ}, t_{PHZ}	Output disable delay	1.0	8.0	1.0	8.0	
t_{HSTB}	Host CLK Stabilization from power-up		3		3	ms
t_{PKP}	PCI CLK period	30.0	∝	30.0	∝	ns
t_{PKPS}	PCI CLK period stability		500		500	ps
t_{PKH}	PCI CLK high time	12.0		12.0		ns
t_{PKL}	PCI CLK low time	12.0		12.0		
t_{PSKW}	PCI Bus CLK Skew		500		500	ps
$t_{HPOFFSET}$	Host to PCI Clock Offset	1.5	4.0	1.5	4.0	ns
t_{PSTB}	PCI CLK Stabilization from power-up		3		3	ms

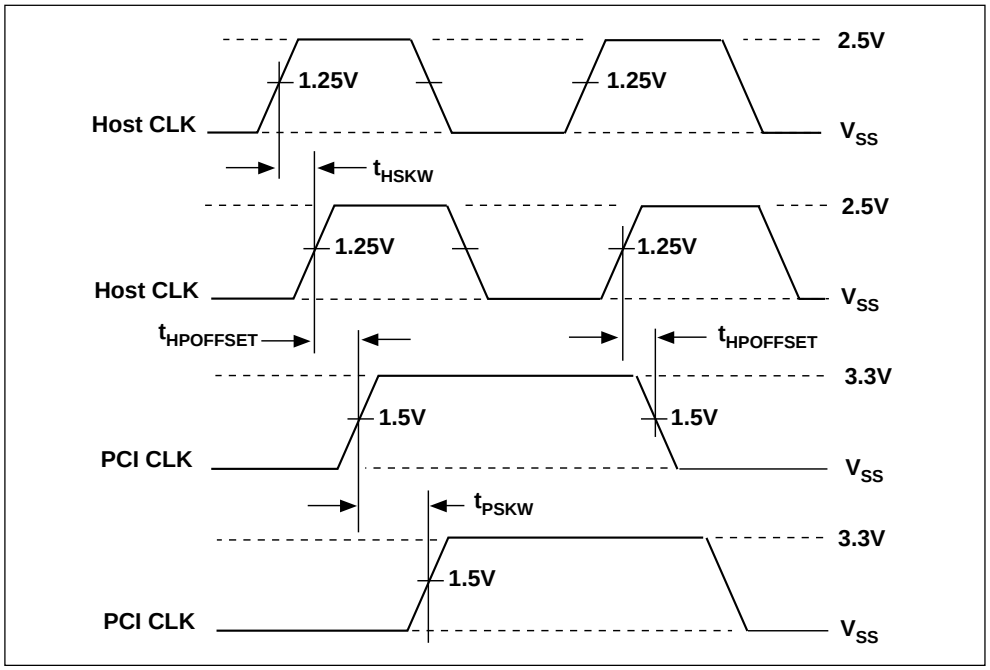


Figure 1. Host Clock and PCI CLK Timing

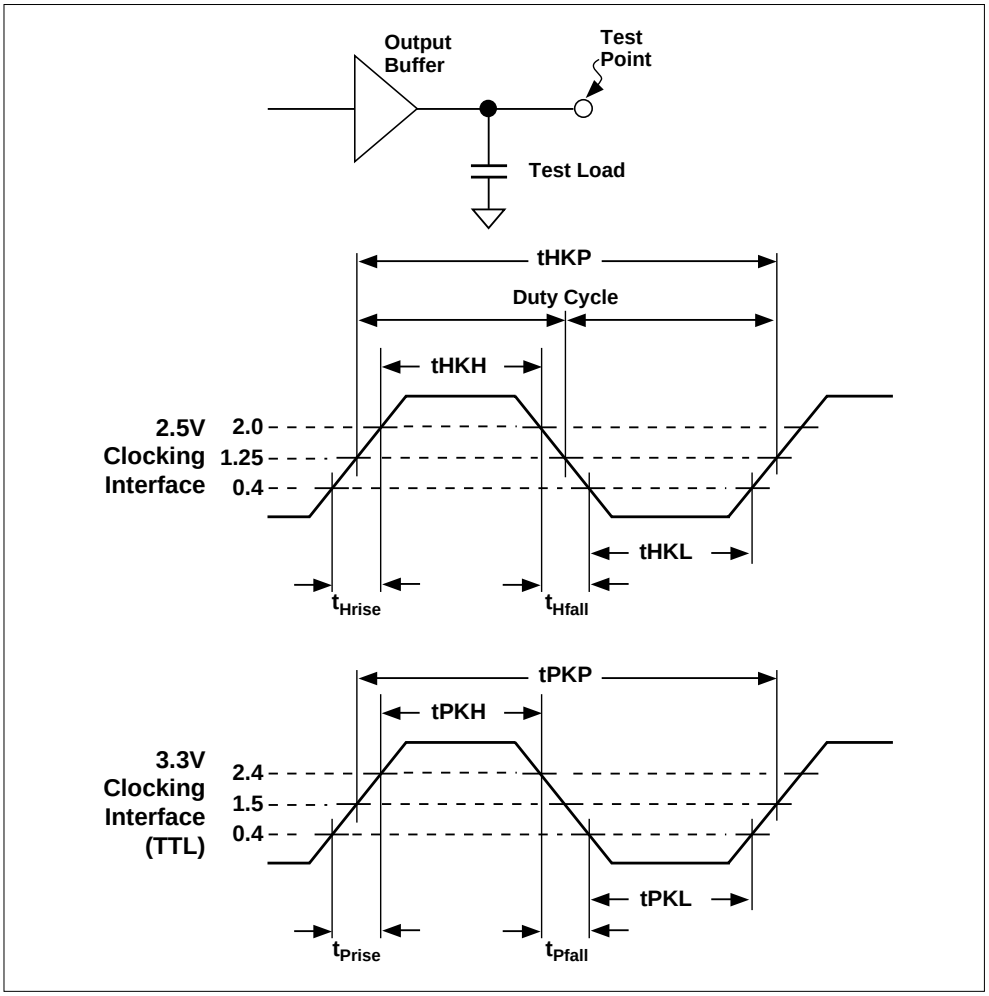
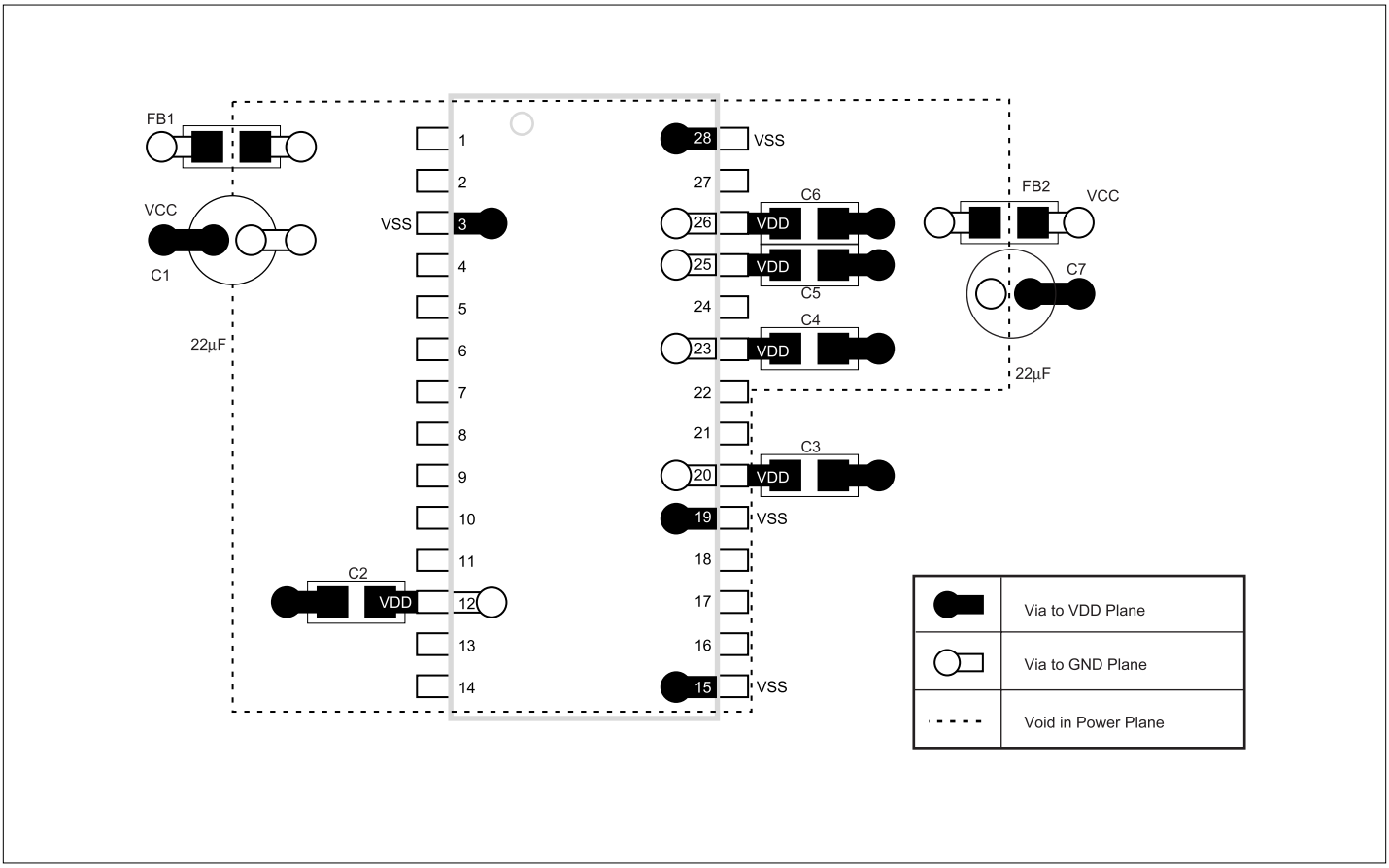


Figure 2. Clock Output Waveforms

PCB Layout Suggestion



Note:

This is only a suggested layout. There may be alternate solutions depending on actual PCB design and layout.

As a general rule, C2-C6 should be placed as close as possible to their respective V_{DD}.

Recommended capacitor values:

C2-C6 ..... 0.1uF, ceramic

C1, C7 ..... 22uF

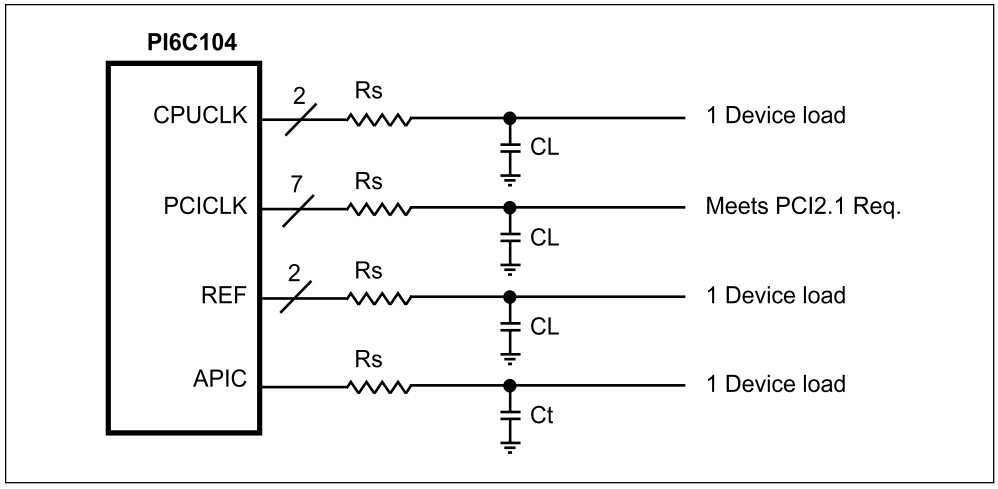
Minimum and Maximum Expected Capacitive Loads

Clock	Min. Load	Max. Load	Units	Notes
CPU Clocks (HCLK)	10	20	pF	1 device load, possible 2 loads
PCI Clocks (PCLK)	30	30		Meets PCI 2.1 requirements
REF, 48MHz	10	20		1 device load

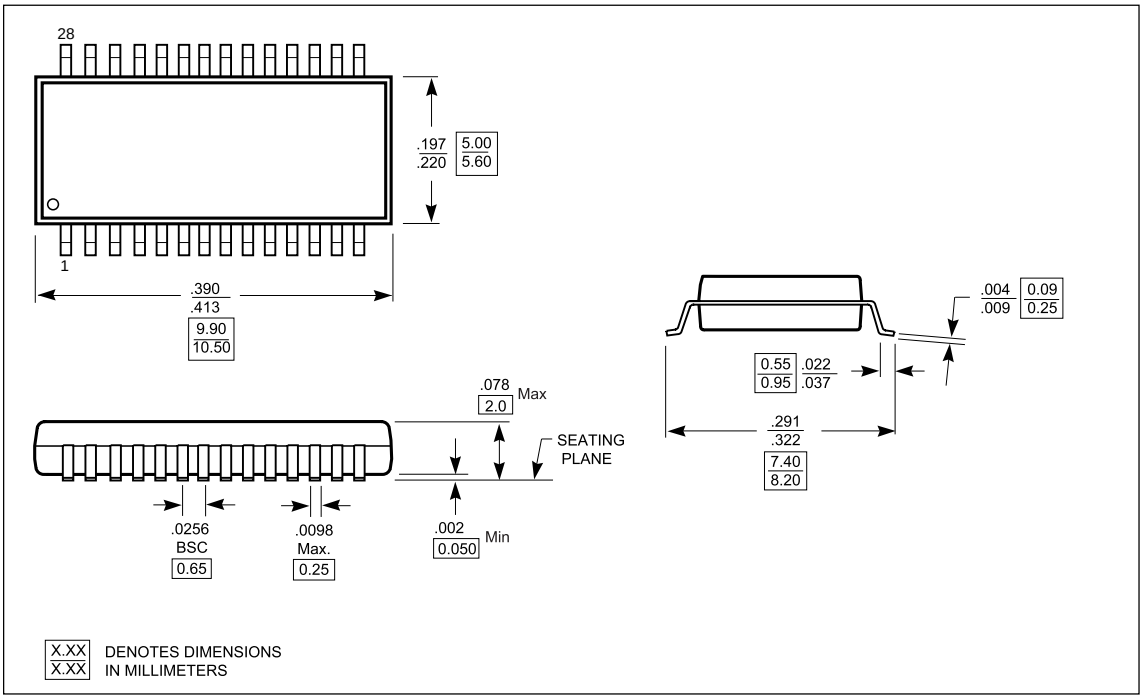
Notes:
1. Maximum rise/fall times are guaranteed at maximum specified load for each type of output buffer.
2. Minimum rise/fall times are guaranteed at minimum specified load for each type of output buffer.
3. Rise/fall times are specified with pure capacitive load as shown. Testing is done with an additional 500Ω resistor in parallel.

Design Guidelines to Reduce EMI

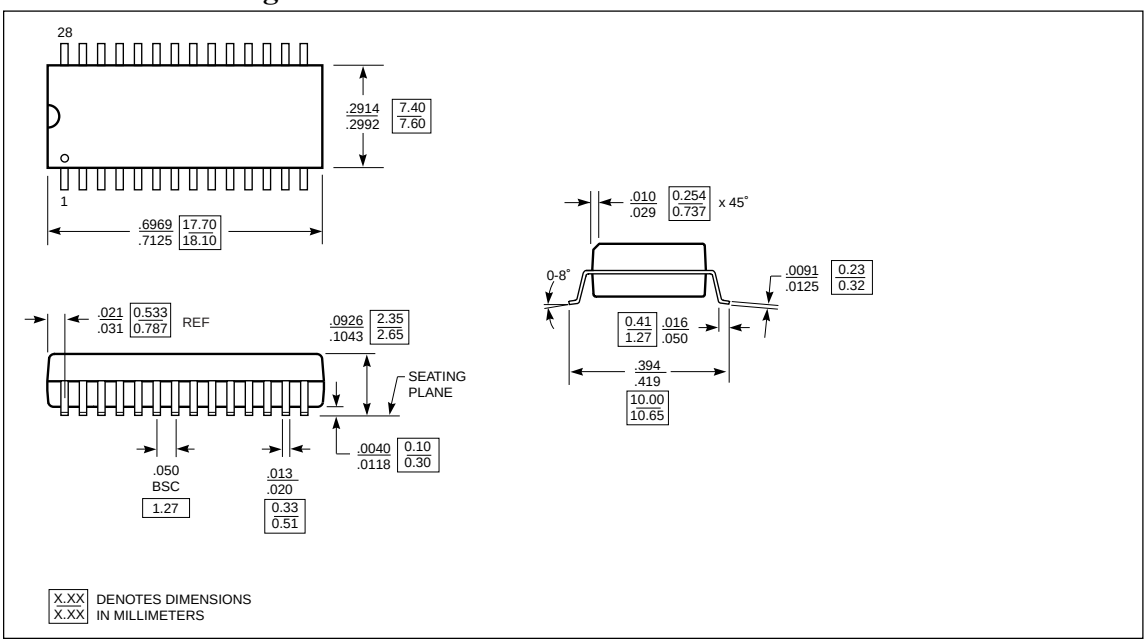
1. Place series resistors and CI capacitors as close as possible to the respective clock pins. Typical value for CI is 10pF. R_S Series resistor value can be increased to reduce EMI provided that the rise and fall time are still within the specified values.
2. Minimize the number of "vias" of the clock traces.
3. Route clock traces over a continuous ground plane or over a continuous power plane. Avoid routing clock traces from plane to plane (refer to rule #2).
4. Position clock signals away from signals that go to any cables or any external connectors.



28-Pin SSOP Package Data



28-Pin SOIC Package Data



Ordering Information

P/N	Description
PI6C104H	28-pin SSOP Package
PI6C104S	28-pin SOIC Package

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2380 Bering Drive • San Jose, CA 95131 • 1-800-435-2336 • Fax (408) 435-1100 • http://www.pericom.com