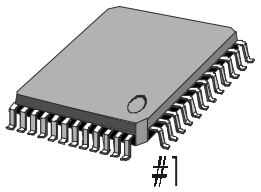
INTRODUCTION

48–LQFP–0707



The S1T8536 is a single chip RF transceiver optimized for use in ISM 2.45GHz wireless systems. It is fabricated using Samsung's ASP5HB 0.5um advanced BiCMOS process.
The S1T8536 contains receiver, transmitter, frequency doubler, voltage controlled oscillator (VCO), phase locked loop(PLL) and crystal oscillator.
The receiver consists of a 2.4 - 2.5GHz high frequency mixer, an intermediate frequency (IF) amplifier, a FM quadrature demodulator, a received signal strength indicator (RSSI), a baseband filter buffer amplifier and a high speed data slicer with sample & hold function.
The transmitter consists of 2.4 - 2.5GHz high frequency buffer amplifier.
The PLL operates upto 1.3GHz with 32/33 prescaler and selectable charge pump current. S1T8536 contains on-chip PLL regulator to minimize switching noise.
The VCO operates 1.15 - 1.3GHz and requires only external tank circuit and loop filter.
S1T8536 contains on-chip VCO regulator to minimize VCO frequency variation due to supply pushing.
The frequency doubler receives 1.15 - 1.3GHz signal from VCO and outputs 2.3 - 2.6GHz signal to receiver and transmitter.
The crystal oscillator operates 5 - 40MHz and can accept external clock signal.
Two additional voltage regulators provide a stable supply source to external discrete stages in the Rx and Tx chains.

FEATURES

- 2.4GHz - 2.5GHz Single-Chip RF Transceiver
- Samsung ASP5HB 0.5um Advanced BiCMOS Process
- 3.0V to 5.5V Operation (RX / TX mode supply current of 75mA / 50mA)
- Single Conversion Receiver with 110MHz IF Frequency
- Quadrature Demodulator with Greater than 1MHz Bandwidth
- Wideband Buffer Amplifier for Baseband Filtering
- High Speed Data Slicer Operating Upto 2Mbps with Sample & Hold
- 1.3GHz PLL with VCO and Frequency Doubler
- PLL, VCO, RX and TX Voltage Regulator Included (2.85V)

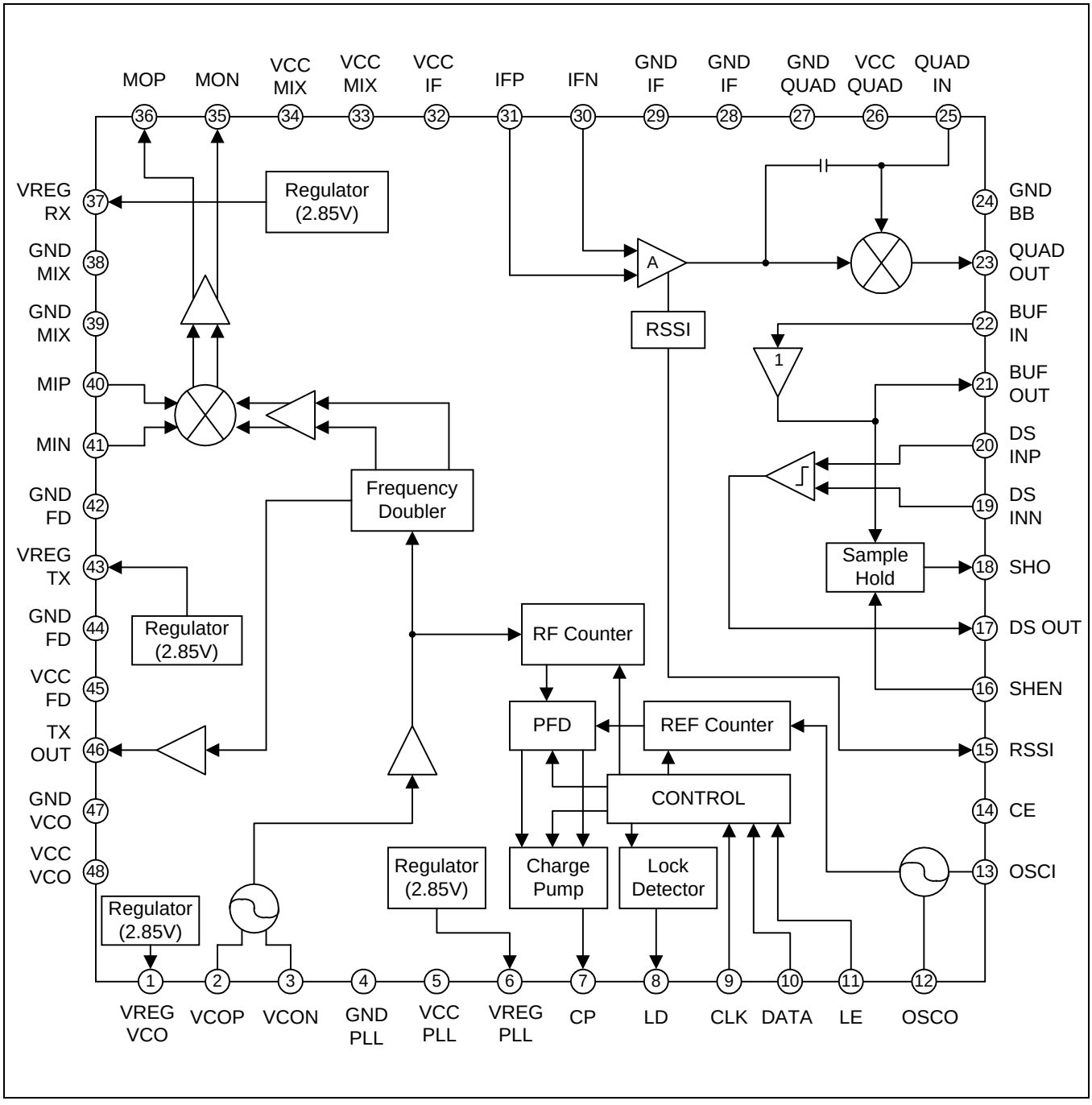
APPLICATION

- 2.45GHz ISM Band Wireless Communication Systems

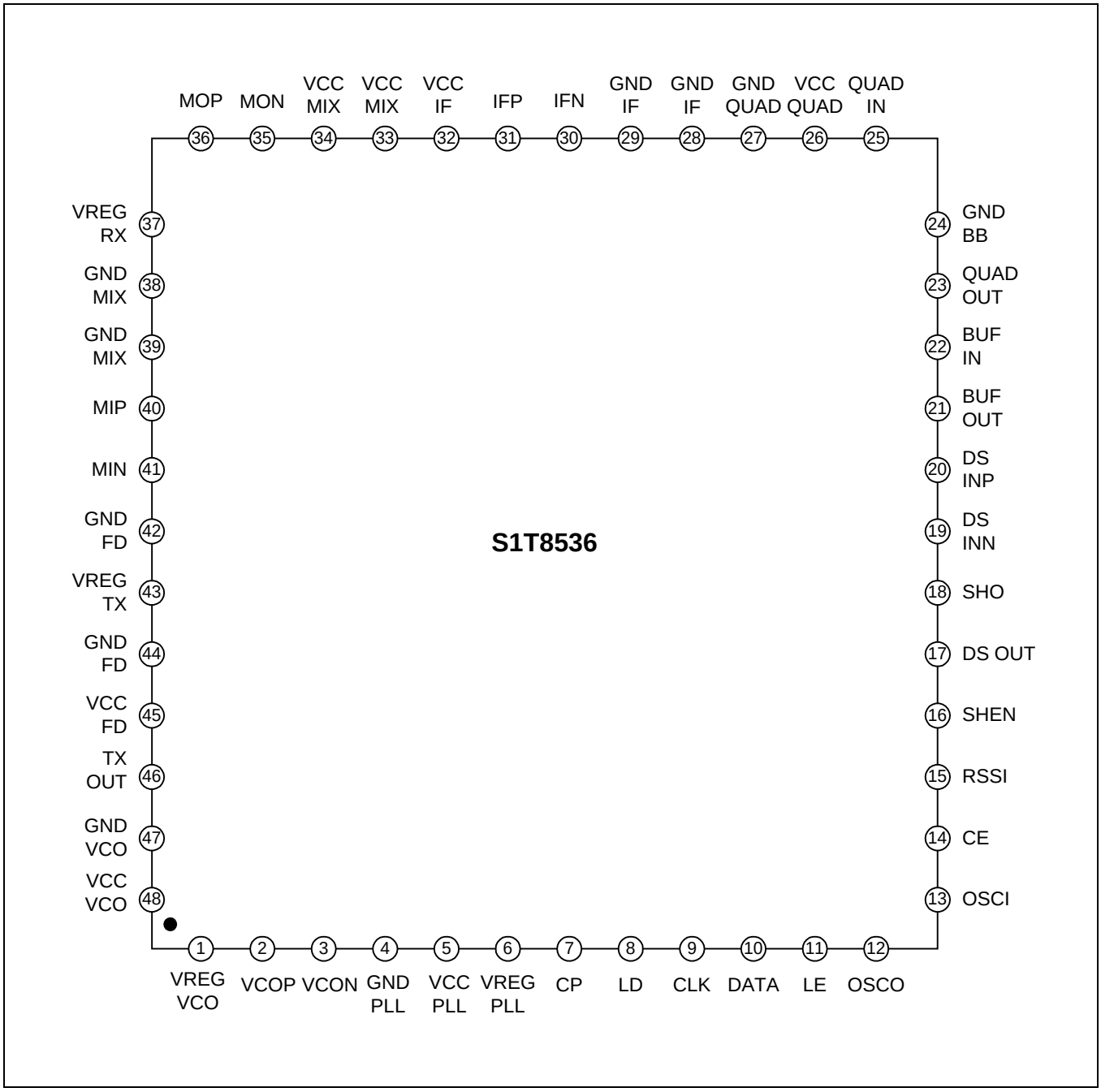
ORDERING INFORMATION

Device	Package	Operating Temperature
S1T8536X01-T0R0	48-LQFP-0707	- 10 to + 70°C

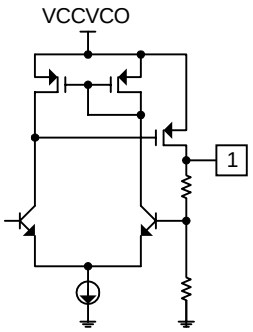
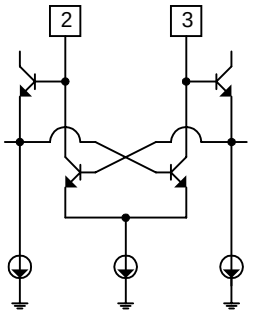
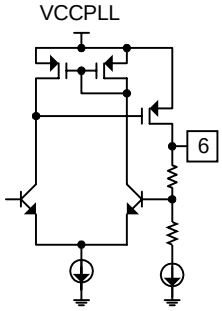
BLOCK DIAGRAM



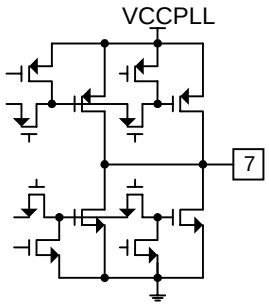
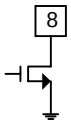
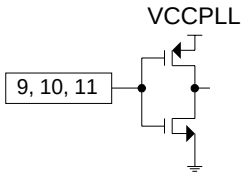
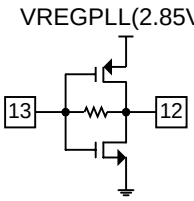
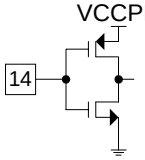
PIN CONFIGURATION



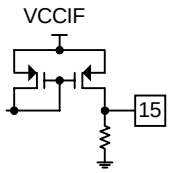
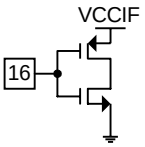
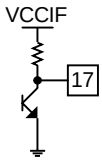
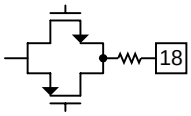
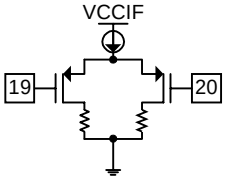
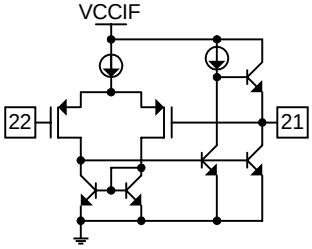
PIN DESCRIPTION

Pin	Name	Schematic	Description
1	VREGVCO		VCO regulator output (2.85V). Requires external bypass capacitor.
2 3	VCOP VCON		These differential ports are used to supply DC voltage to the VCO as well as tune the center frequency of the VCO.
4	GNDPLL		Ground of PLL section (Note 1).
5	VCCPLL		Supply of PLL section.
6	VREGPLL		PLL regulator output (2.85V). Requires external bypass capacitor.

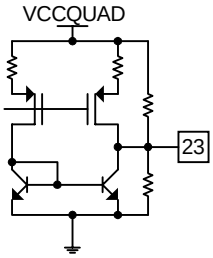
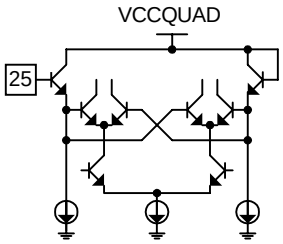
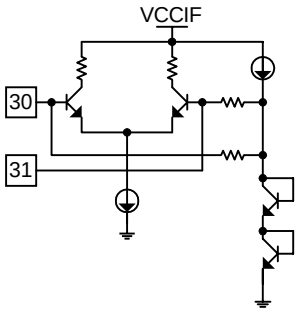
PIN DESCRIPTION (Continued)

Pin	Name	Schematic	Description
7	CP		Charge pump output.
8	LD		Lock detector open drain output.
9 10 11	CLK DATA LE		Programming clock input. Programming data input. Programming load enable input.
12 13	OSCO OSCI		Crystal oscillator input. Crystal oscillator output.
14	CE		Chip enable input. Logic high input enables the chip and logic low input disables the chip.

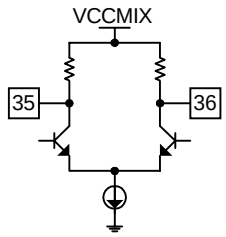
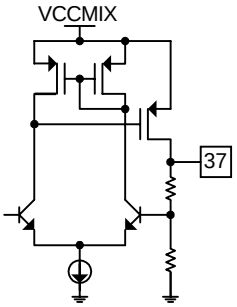
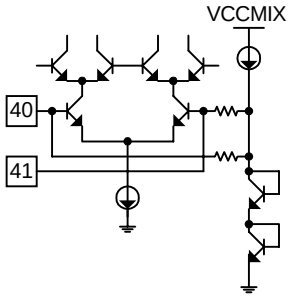
PIN DESCRIPTION (Continued)

Pin	Name	Schematic	Description
15	RSSI		Received signal strength indicator output.
16	SHEN		Sample and hold enable input. High signal input enable sample and hold function and low signal input disable sample and hold function .
17	DSOUT		Data slicer output.
18	SHO		Sample and hold output.
19 20	DSINN DSINP		Data slicer negative input. Data slicer positive input.
21 22	BUFOUT BUFIN		Baseband filter buffer amplifier output. Baseband filter buffer amplifier input.

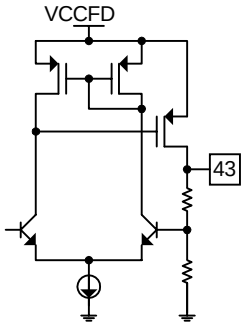
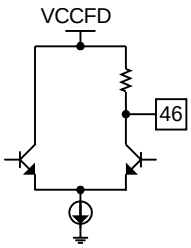
PIN DESCRIPTION (Continued)

Pin	Name	Schematic	Description
23	QUADOUT		Quadrature demodulator output.
24	GNDBB		Ground of baseband section (Note 1).
25	QUADIN		Quadrature demodulator tank input.
26	VCCQUAD		Supply of quadrature detector section.
27	GNDQUAD		Ground of quadrature detector section (Note 1).
28 29	GNDIF GNDIF		Ground of IF amplifier section (Note 1). Pin28 and Pin29 are connected internally.
30 31	IFN IFP		IF amplifier differential inputs. DC blocking is required.
32	VCCIF		Supply of IF amplifier section.
33 34	VCCMIX VCCMIX		Supply of mixer section. Pin33 and Pin34 are connected internally.

PIN DESCRIPTION (Continued)

Pin	Name	Schematic	Description
35 36	MON MOP		RF mixer differential IF outputs.
37	VREGRX		RX regulator output (2.85V). Requires external bypass capacitor.
38 39	GNDMIX GNDMIX		Ground of mixer section (Note 1). Pin38 and Pin39 are connected internally.
40 41	MIP MIN		RF mixer differential inputs. DC blocking is required.
42	GNDFD		Ground of frequency doubler section (Note 1).

PIN DESCRIPTION (Continued)

Pin	Name	Schematic	Description
43	VREGTX		TX regulator output (2.85V). Requires external bypass capacitor.
44	GNDFD		Ground of frequency doubler section (Note 1).
45	VCCFD		Supply of frequency doubler section.
46	TXOUT		TX buffer amplifier output.
47	GNDVCO		Ground of VCO section (Note 1).
48	VCCVCO		Supply of VCO section.

NOTE: All ground pads of the chip are down bonded to package ground paddle and each ground pin of the IC is connected to that package ground paddle.
So all the ground pins are connected together through the exposed ground paddle of the IC package. Proper connection of package ground to board ground is essential and highly required.

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	6.0	V
Voltage applied to any pin	V_{IN}	VCC + 0.3	V
Storage Temperature Range	T_{STG}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	3.6	V
Operating Temperature	T_a	-10 to +70	°C

Caution : S1T8536 is a high performance RF integrated circuit and is ESD sensitive.
Handling and assembly of this device should be done at ESD work stations.

DC ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 3.6V, unless otherwise noted.)

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
RX Mode Supply Current (Receiver + Frequency Doubler + PLL + VCO)	ICC-RX	-	-	75	100	mA
TX Mode Supply Current (Transmitter+Frequency Doubler+PLL+VCO)	ICC-TX	-	-	50	70	mA
Locking Mode Supply Current (PLL + VCO)	ICC-LOCK	-	-	20	30	mA
Power Down Mode Supply Current (All Off)	ICC-PD	CE(PIN14)=LOW	-	10	100	uA

RECEIVER / TRANSMITTER ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{CC}=3.6V, unless otherwise noted. RF=2.45GHz/-47dBm, LO=1.17GHz/-15dBm, IF=110.592MHz

Data = 1Mbps pseudo random sequence with BTb = 0.5 GFSK modulation. Modulation index = 0.5)

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
Mixer Input RF Frequency	RF In Freq.	50ohm matching	2.4	-	2.5	GHz
Mixer Output IF Frequency	IF Out Freq	SAW matching	50	110.6	200	MHz
1E-3 BER Sensitivity (Notes 1 and 2)	SENS	data out	-	-82	-76	dBm
IF Amplifier Bandwidth	IFAmp BW	-	50	-	200	MHz
IF Amplifier Voltage Gain	IFAmp Gain	-	70	75	-	dB
Quadrature Demodulator Output Voltage	DET Out	External load variable	100	150	200	mVrms
Quadrature Demodulator Bandwidth	DET BW	-	0.6	1	-	MHz
Baseband Filter Buffer Amplifier Bandwidth	BB Amp BW	External load variable	1	2	-	MHz
Baseband Filter Buffer Amplifier Voltage Gain	BB Amp Gain	-	-3	0	+3	dB
Data Slicer Maximum Operating Frequency	DS BW	-	1	2	-	Mbps
RSSI Dynamic Range (110MHz IF Amp Input)	RSSI DR	-	50	60	-	dB
RSSI Output Level (110MHz IF Amp Input)	RSSI Out	IF input(110MHz)	0.5	-	2.0	V
TX Output Power (Notes 1 and 2)	TX Out	50ohm matching	-	-15	-	dBm

NOTES:

1. Not 100% AC tested but guaranteed by design and characterization.
2. Measured result on evaluation board with proper impedance matching.

VCO / PLL ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 3.6V, unless otherwise noted)

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
VCO Operating Frequency (Note 1)	VCO Freq.	-	1150	-	1300	MHz
PLL Operating Frequency	RF In Freq	-	1150	-	1300	MHz
PLL Input Sensitivity (external VCO Input)	RF In Power	-	-15	-	5	dBm
OSC Operating Frequency	OSC In Freq.	-	5	-	40	MHz
OSC Input Sensitivity	OSC In Power	-	100	500	2000	mVpp
Charge Pump Output Current	CPI = Low	-	± 1.1	± 1.5	± 2.0	mA
	CPI = High	-	± 2.1	± 3.0	± 4.0	mA

NOTE: Not 100% AC tested but guaranteed by design and characterization.

REGULATOR ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 3.6V, unless otherwise noted.)

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
PLL Regulator Voltage (Note 1)	VREG-PLL	load regulated	2.7	2.85	3.0	V
VCO Regulator Voltage (Note 1)	VREG-VCO	load regulated	2.7	2.85	3.0	V
RX Regulator Voltage (Notes 1 and 2)	VREG-RX	load regulated	2.7	2.85	3.0	V
TX Regulator Voltage (Notes 1 and 2)	VREG-TX	load regulated	2.7	2.85	3.0	V

NOTES:
1. Voltage regulation operates under the condition of supply voltage greater than 3.3V.
2. RX and TX regulator are tested with load current of 10mA.

DIGITAL I / O ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 3.6V, unless otherwise noted)

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
High Level Input Voltage	VIH	-	VCC-0.4	-	VCC	V
Low Level Input Voltage	VIL	-	0	-	0.4	V
High Level Output Voltage	VOH	-	VCC-0.4	-	VCC	V
Low Level Output Voltage	VOL	-	0	-	0.4	V

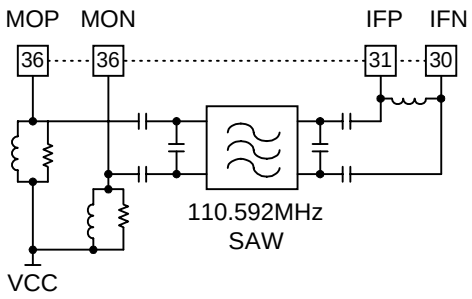
RECEIVER FUNCTIONAL DESCRIPTION

General

The S1T8536's receiver is a single conversion wideband FM / FSK receiver. This device is designed for use as the receiver in analog and digital FM systems such as 2.4GHz ISM band cordless phones and wideband data links with data rates up to 2Mbps. It contains high frequency mixer, IF amplifier, quadrature detector, baseband filter amplifier and data slicer with sample and hold function.

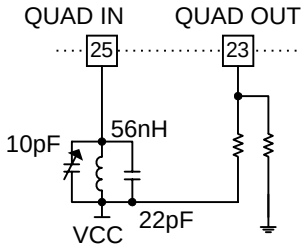
Mixer

The mixer is a double-balanced with fully differential RF inputs and fully differential IF outputs. Following figure shows the external components required for wideband 110.592MHz IF operation.



Quadrature Demodulator

The quadrature demodulator requires tank circuit with loaded Q depending on detection bandwidth. Following figure shows external components required for 110.592 MHz IF operation.



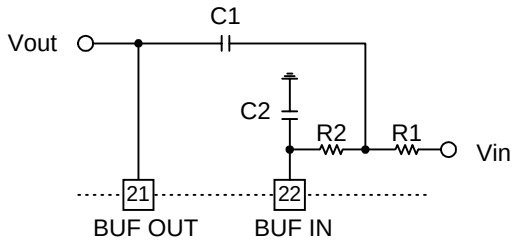
Baseband Filter Buffer Amplifier

Baseband filter amplifier is a wideband buffer and it can be configured as a second-order sallen-key low pass filter. Following figure shows the external components required.

Cutoff frequency = 1 / [2π*SQRT(R1R2C1C2)]
Quality factor = SQRT(R1R2C1C2) / (R1C2 + R2C2)

The component value of R1 should contain the quadrature detector output resistance.

RECEIVER FUNCTIONAL DESCRIPTION



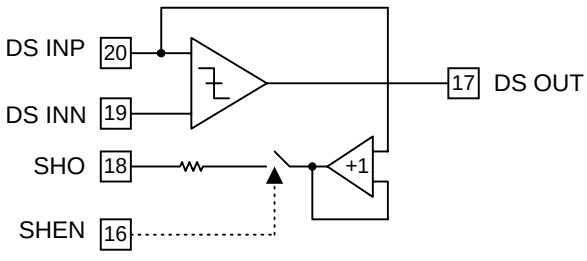
Data Slicer with Sample and Hold

The data slicer is a comparator that is designed to square up the data signal. The recovered data signal from the baseband filter output can be DC coupled to the data slicer DS-INP(Pin 20). The S1T8536's data slicer incorporates an sample and hold used to derive the data slicer reference voltage by means of an external integration circuit. The sample and hold is 'ON' during reception of the preamble data pattern, and is otherwise 'OFF' in TDD (Time Division Duplex) system. The external integration circuit is formed by an RC low pass circuit placed between SHO (Pin 18) and ground.

The size of this resistor and capacitor and the nature of the data signal determine how faithfully the data slicer shapes up the recovered signal. The time constant is short for large peak to peak voltage swings or when there is a change in DC level at the detector output. For small signal or for continuous bits of the same polarity which drift close to the threshold voltage, the time constant is longer.

The sample and hold is able to sink/source 3mA to/from the external integration circuit in order to minimize the settling time. When the sample and hold is 'OFF' the output (SHO) is in high impedance state with extremely low leakage current.

Following figure shows the internal block diagram.



The output of the data slicer (DS-OUT) is a CMOS compatible bitstream. However, it is recommended that an external NPN amplifier stage be used to drive the CMOS baseband processor, in order to minimize the amount of ground and supply currents in the S1T8536 which might desensitize the chip.

PLL / VCO FUNCTIONAL DESCRIPTION

GENERAL

The S1T8536's PLL / VCO is a high performance frequency synthesizer with high frequency voltage controlled oscillator and integrated high frequency prescalers for RF operation upto 1.3GHz. It contains two voltage regulator of VCO and PLL, dual modulus prescalers providing 32/33 division, no dead-zone PFD, selectable charge pump current, lock detector output and crystal oscillator.

VCO / PLL VOLTAGE REGULATOR

The S1T8536's PLL / VCO incorporates one on-chip 2.85V voltage regulators for stable VCO operation and another on-chip 2.85V voltage regulators for minimizing ECL and CMOS switching noise eliminating the need for an external regulator. They insures stable high frequency operation at 3.0V through 5.5V supply voltage .

VCO regulated voltage is used only for VCO. PLL regulated voltage is used for ECL-prescaler, CMOS-counter, internal logic circuits and crystal oscillator. All digital input / output pins are referenced to supply voltage rather than regulated voltage.

CRYSTAL OSCILLATOR

S1T8536 has a oscillator circuit composed of CMOS inverter amplifier. In case of inputting the external reference frequency directly, use OSCI terminal (Pin 13).

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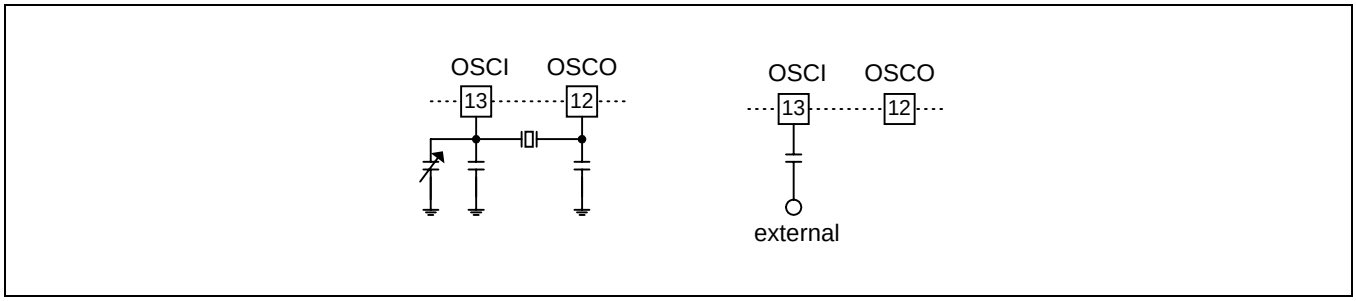
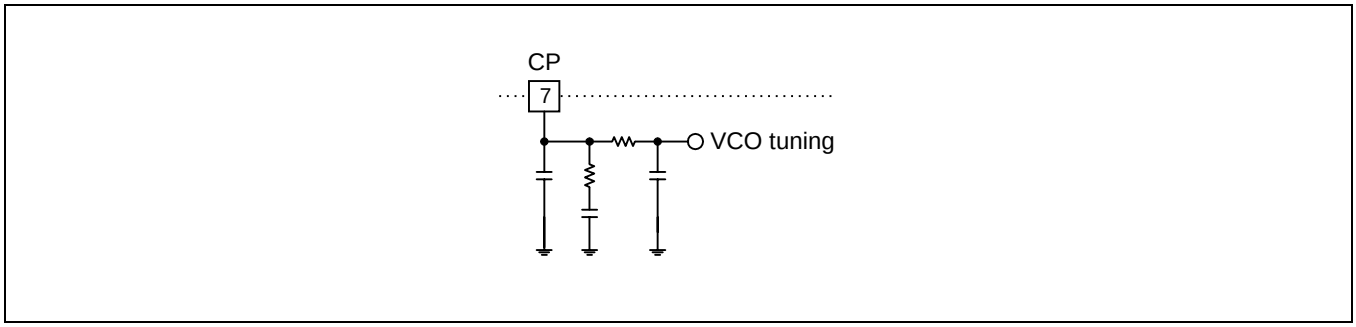
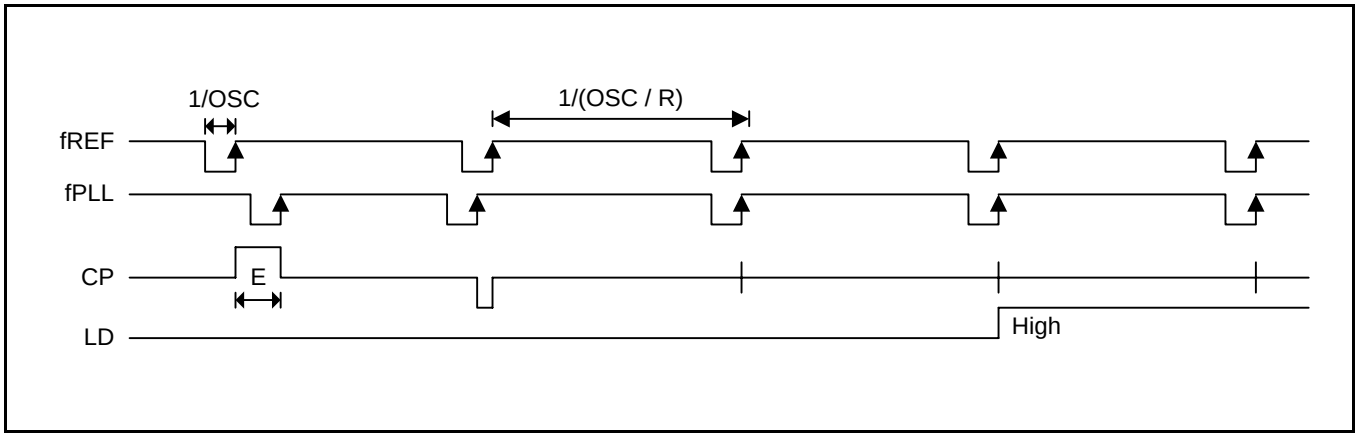


LOOP FILTER

Following figure shows third order passive loop filter



LOCK DETECTOR OPERATION

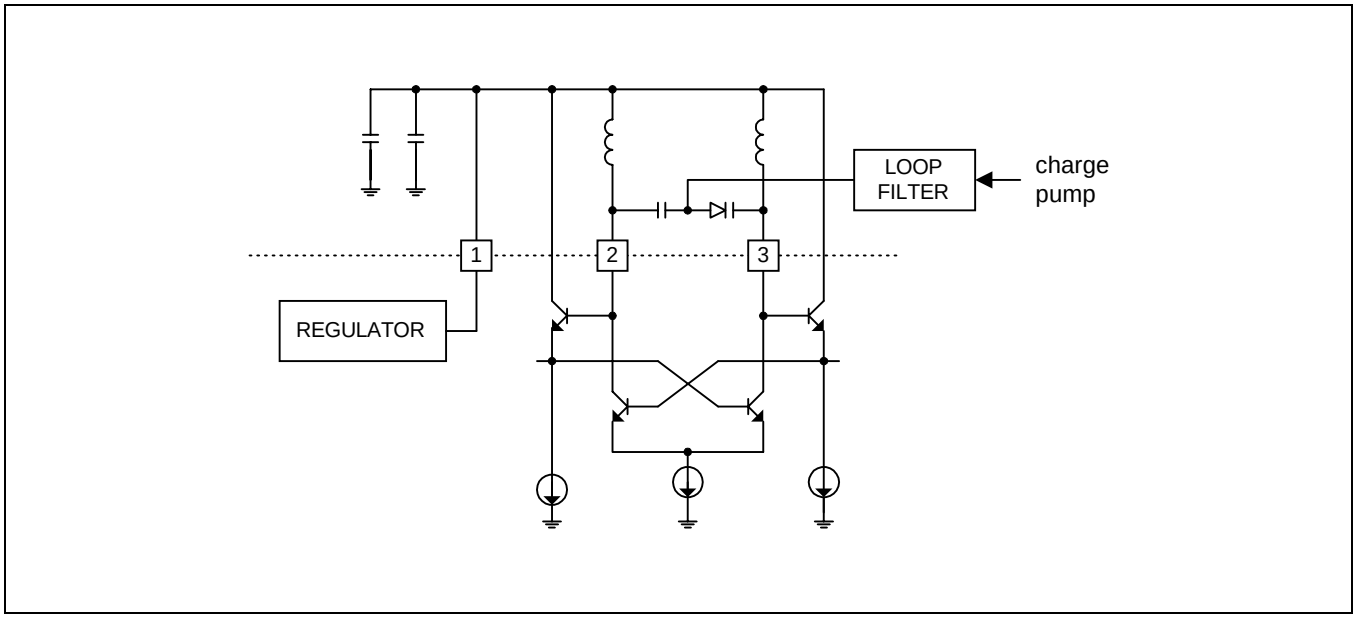


When the situation that E(error) is less than one period of reference frequency, 1/OSC, continues more than three cycles of reference counter output, 1/(OSC/R), lock detector outputs 'High'.

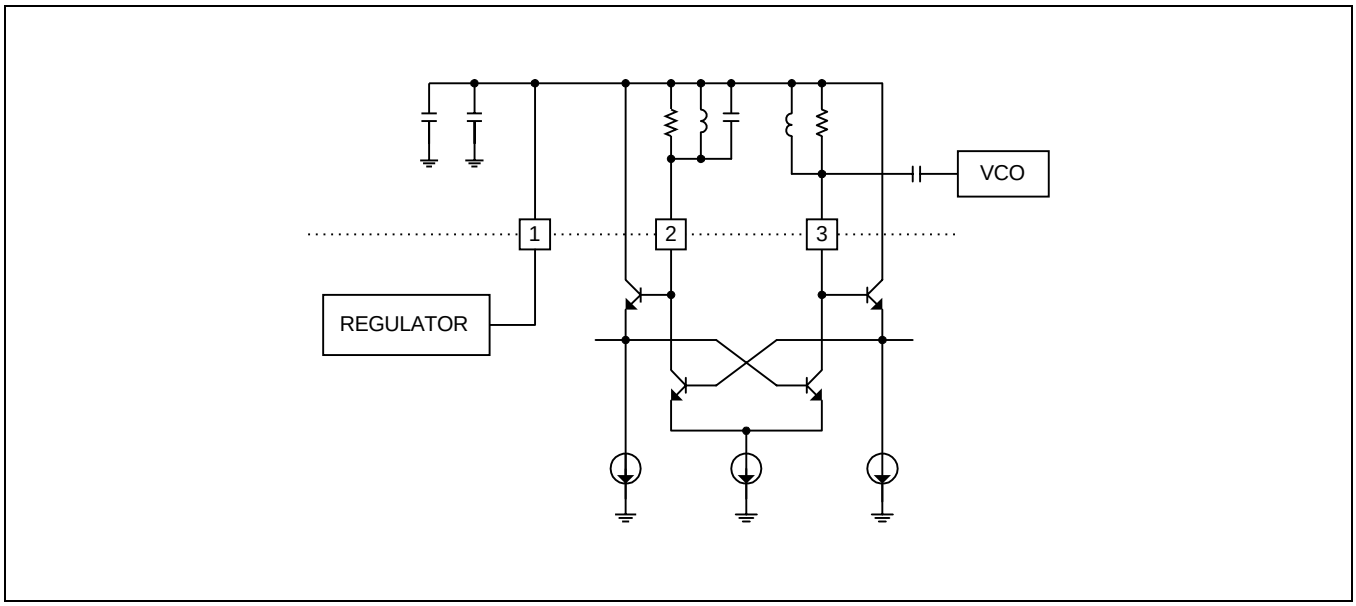
PLL / VCO FUNCTIONAL DESCRIPTION

VOLTAGE CONTROLLED OSCILLATOR

S1T8536's voltage controlled oscillator (VCO) uses a fully differential topology, with L-C resonant tank circuit off-chip.
Following figure shows external components for VCO operation.



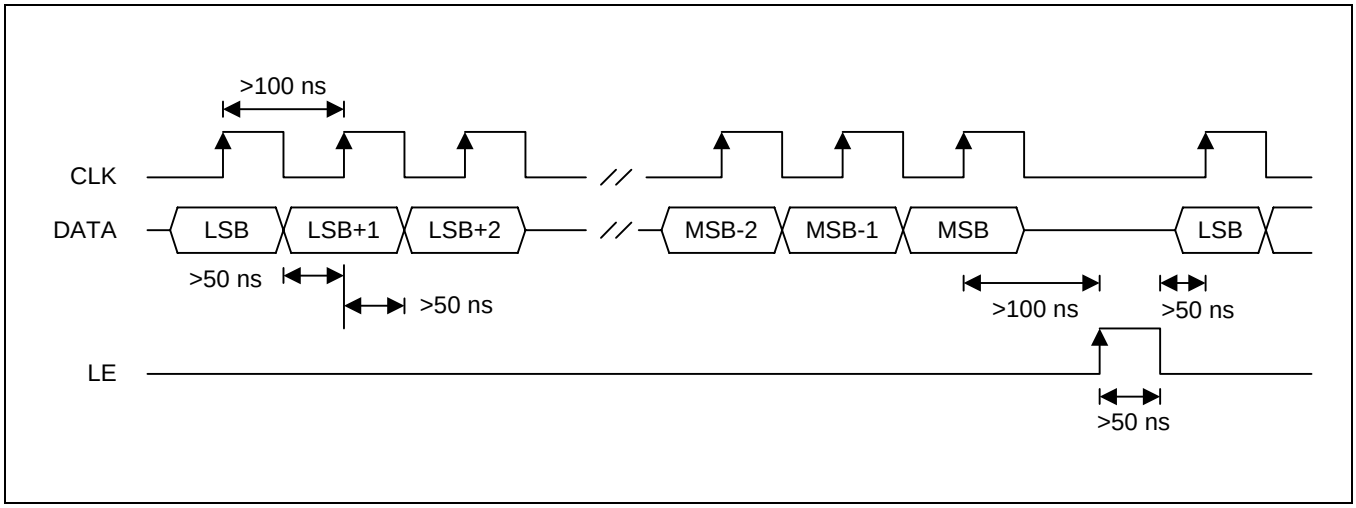
Following figure shows external components in case of using external VCO.



PROGRAMMING DESCRIPTION

SERIAL DATA PROGRAMMING TIMING

Every bit of data is shifted into the internal shift register on the rising edge of the clock. When the load enable (LE) pin goes to high, stored data is latched according to the group code. The three terminals, CLK, DATA and LE, contain schmitt trigger circuits to keep the programming from errors caused by noise and etc.



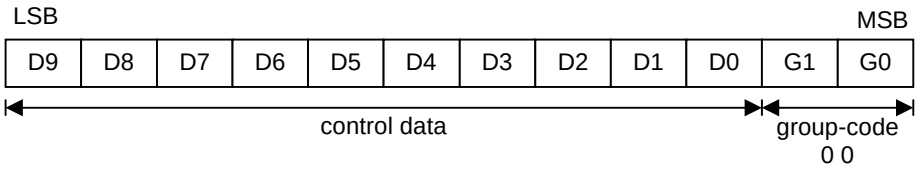
SERIAL DATA PROGRAMMING GROUP

S1T8536 can be controlled through 3 kinds of program group. Each group is identified by selective 2 bits group codes given below.

MSB-1	MSB	Group Selection
GC1	GC0	
0	0	Control Latch
0	1	N-Counter Latch
1	0	R-Counter Latch
1	1	Not Allowed

PROGRAMMING DESCRIPTION

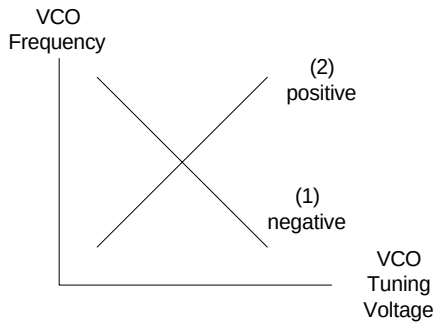
CONTROL DATA PROGRAMMING (Data should be shifted in LSB first)



Bit	Name	Description	Setting to '0'	Setting to '1'
D0	PDP	Phase detector polarity select.	Negative VCO	Positive VCO
D1	CPI	Charge pump output current select.	+ 1.5mA	+ 4.5mA
D2	CPZ	Charge pump output state select.	Normal operation	High Impedance
D3	RXPD	Receiver power down control.	Receiver 'ON'	Receiver 'OFF'
D4	TXPD	Transmitter power down control.	Transmitter 'ON'	Transmitter 'OFF'
D5	VCOPD	VCO power down control.	VCO 'ON'	VCO 'OFF'
D6	PLLPD	PLL power down control.	PLL 'ON'	PLL 'OFF'
D7	OSCPD	Crystal oscillator power down control	Oscillator 'ON'	Oscillator 'OFF'
D8	TEST0	Test mode control.	See below.	
D9	TEST1	Test mode control.		

Charge Pump Polarity

Depending upon VCO characteristics, phase detector polarity should be set accordingly.
When VCO characteristics are like (1), phase detector polarity bit (PDP) should be set low ('0').
When VCO characteristics are like (2), phase detector polarity bit (PDP) should be set high ('1').



PROGRAMMING DESCRIPTION

Charge Pump Output State Control

CPZ bit is provided for open loop modulation during TX time slot in TDD (Time Division Duplex) system.

D2		
CPZ	Charge pump output state	VCO operation
0	Normal	Closed loop
1	High impedance	Open Loop

Power Mode Control

D3	D4	D5	D6	D7	Power down state				
RX PD	TX PD	VCO PD	PLL PD	OSC PD	Frequency Doubler	VCO Regulator	PLL Regulator	RX Regulator	TX Regulator
0	1	0	0	0	ON	ON	ON	ON	OFF
1	0	0	0	0	ON	ON	ON	OFF	ON
1	1	0	0	0	OFF	ON	ON	OFF	OFF
1	1	0	1	0	OFF	ON	ON	OFF	OFF
1	1	1	1	0	OFF	OFF	ON	OFF	OFF
1	1	1	1	1	OFF	OFF	OFF	OFF	OFF

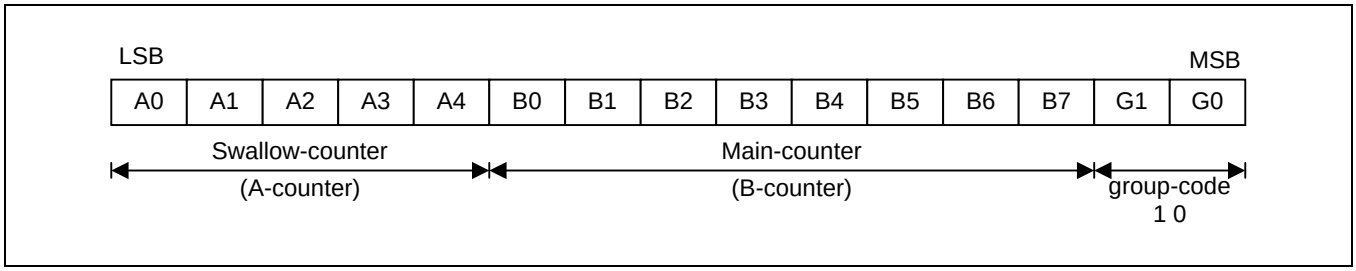
Test Mode Control

D9	**D8**	**LD Output**
TEST1	**TEST0**	
0	0	Lock Detect
0	1	fPLL (VCO / N)
1	0	fREF (OSC / R)
1	1	High

PROGRAMMING DESCRIPTION

N-COUNTER DIVISION RATIO DATA PROGRAMMING (Data should be shifted in LSB first)

The N-counter consists of the 5-bit swallow counter (A-counter), 8-bit programmable main counter (B-counter) and dual-modulus prescaler providing 32 / 33 division.



5-Bit Swallow Counter (A-Counter) Division Ratio
A = A4*2^4 + A3*2^3 + A2*2^2 + A1*2^1 + A0*2^0
Division ratio : 0 to 31, A < B

Division Ratio (A-Counter)	A4	A3	A2	A1	A0
0	0	0	0	0	0
1	1	0	0	0	0
•	•	•	•	•	•
31	1	1	1	1	1

8-Bit Main Counter (B-Counter) Division Ratio
B = B7*2^7 + B6*2^6 + B5*2^5 + B4*2^4 + B3*2^3 + B2*2^2 + B1*2^1 + B0*2^0
Division ratio : 3 to 255, B > A

Division Ratio (B-Counter)	B7	B6	B5	B4	B3	B2	B1	B0
3	1	1	0	0	0	0	0	0
4	0	0	1	0	0	0	0	0
•	•	•	•	•	•	•	•	•
255	1	1	1	1	1	1	1	1

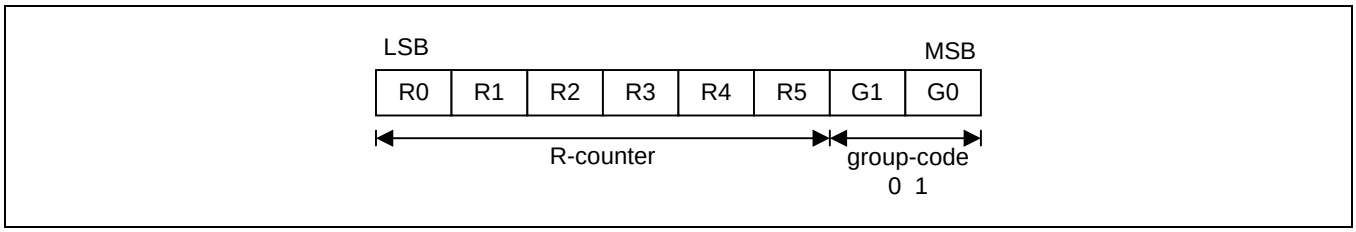
N-Counter Division Ratio

N = (PXB) + A
P : Modulus of dual modulus prescaler which is 32
B : Division ratio of 8-bit main counter
A : Division ratio of 5-bit swallow counter

PROGRAMMING DESCRIPTION

REFERENCE-COUNTER DIVISION RATIO DATA PROGRAMMING (Data should be shifted in LSB first)

The R-counter consists of the 6-bit reference counter.



6-Bit Reference Counter Division Ratio

R = R5*2^5 + R4*2^4 + R3*2^3 + R2*2^2 + R1*2^1 + R0*2^0
Division ratio : 3 to 63

Division Ratio	R5	R4	R3	R2	R1	R0
3	1	1	0	0	0	0
4	0	0	1	0	0	0
•	•	•	•	•	•	•
63	1	1	1	1	1	1

Example) If a 19.2MHz oscillator is connected, the internal PLL reference frequency is 400KHz,and the VCO frequency is 1.2GHz,then equation is as follows.

R = X-tal / Reference Frequency

R = 19.2MHz / 400KHz = 48(d) = **110000(**b)

The R register setting is **000011**01(b).

N = Fvco / Freference

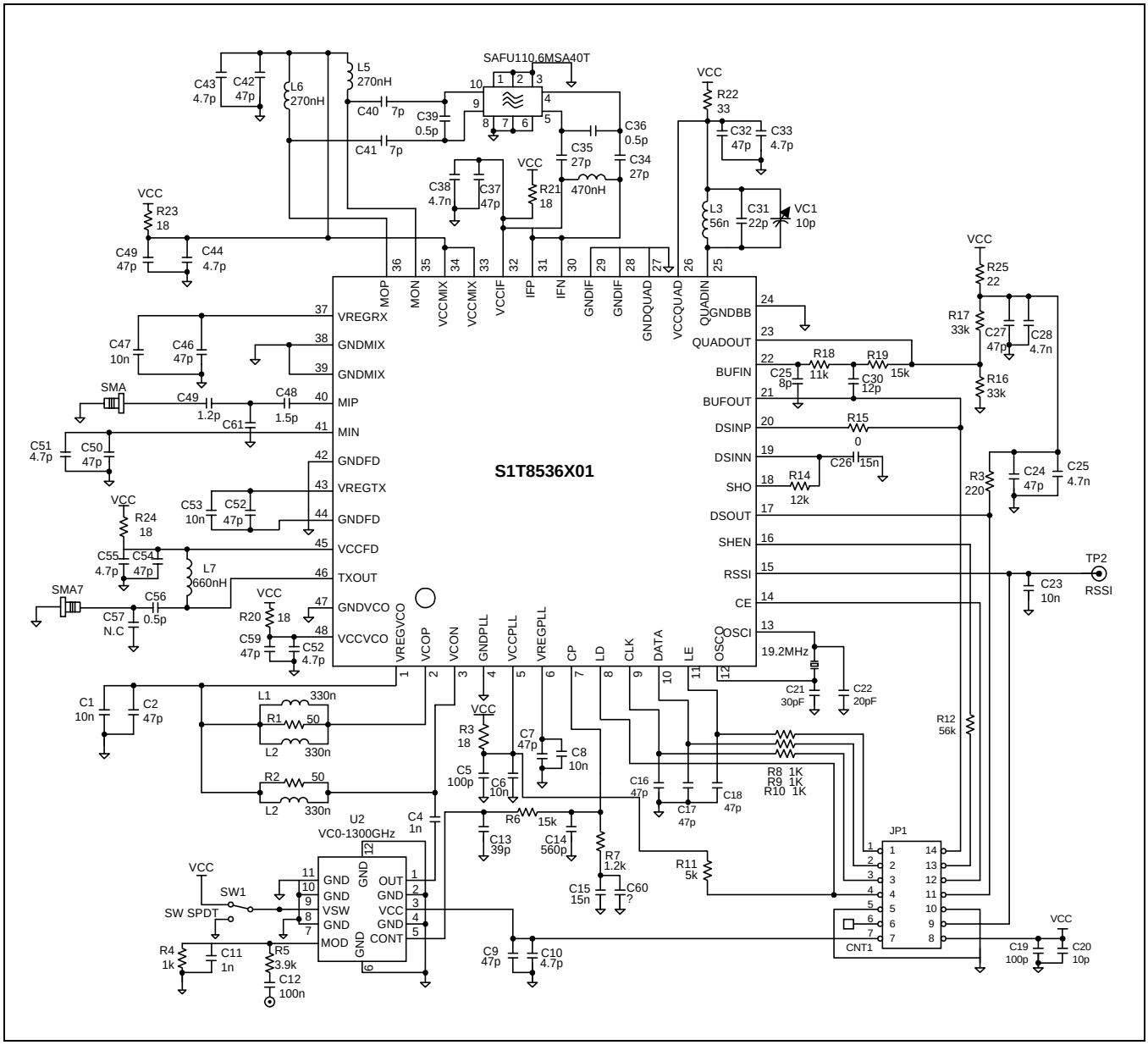
N =1.2GHz / 400KHz = 3000

N = 3000 / 32 = 93.75 , The B(main counter) is 93(d) = ***1011101(***b)

S = 0.75 * 32 = 24 , The S(swallow counter) is 24(d) = **11000(**b)

The N register setting is **00011*10111*01**010(b).

TEST CIRCUIT



APPLICATION CIRCUIT