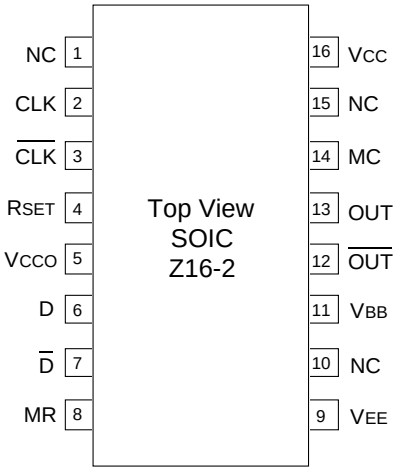
LASER DIODE DRIVER WITH INPUT D FLIP-FLOP

PRELIMINARY
SY100EL1001

FEATURES

- **Up to 1.25Gb/s operation**
- **75mA peak drive current**
- **Separate modulation control**
- **Separate master reset for laser safety**
- **Differential inputs for data and clock**
- **75KΩ input pulldown resistor**
- **Single power supply**
- **Available in 16-pin SOIC package**

PIN CONFIGURATION



DESCRIPTION

The SY100EL1001 is a high speed current source for driving a semiconductor laser diode in optical transmission applications. The output current modulation is DC – voltage controlled. The integrated circuit contains the following functional blocks:

- Input Line Receiver
- D Flip-Flop
- Bias Control Circuitry
- Output Current Switch

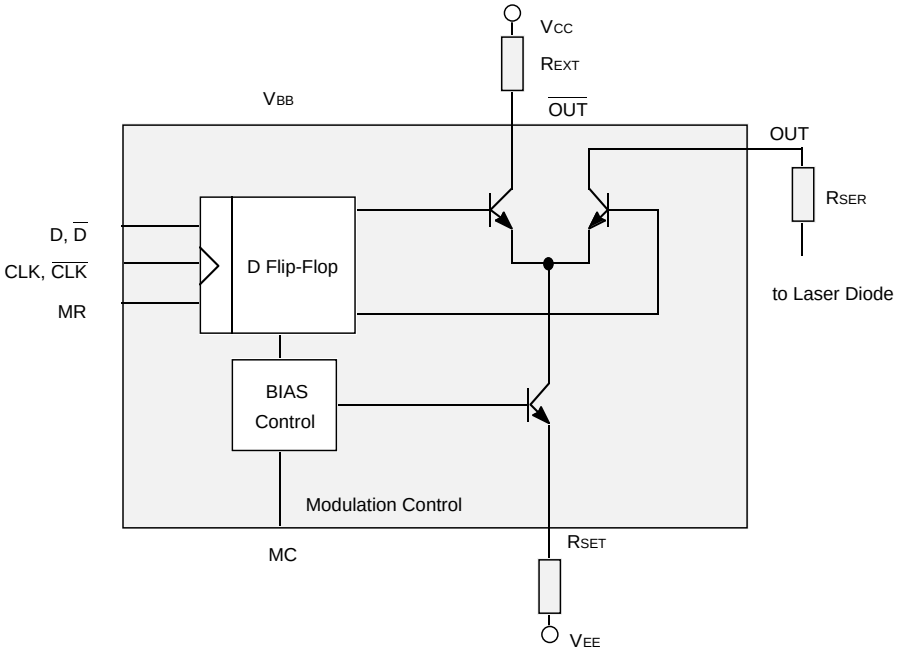
A logic HIGH level at the data input results in the modulation current flowing through the OUT pin on the next rising edge of the clock. A logic HIGH level at the master reset input will disable the modulation current.

The device incorporates complementary open collector outputs with a capability of driving peak current of 75 mA.

The laser driver current is adjustable by selection of RSET. The resistor REXT must be placed between $\overline{OUT}$ and VCC to dissipate the worst case power. RSER is recommended to fix laser diode matching issues.

The SY100EL1001 utilizes the high performance bipolar ASSET technology.

BLOCK DIAGRAM



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Issue Date: August, 1998

PIN NAMES

Pin	Function
V_{CC}, V_{CCO}	Most positive power supply pins separation helps to isolate sensitive circuitry from noise generating function. +5V for PECL operation or ground for ECL operation.
V_{EE}	Most negative power supply input. Ground for PECL operation or -5V for ECL operation.
V_{BB}	This pin provides a reference voltage for use in single ended applications or when the input signal is AC coupled into the device.
D,$\overline{D}$	These differential ECL/PECL 100K compatible inputs receive NRZ data.
CLK, $\overline{CLK}$	These differential clock inputs
MR	This ECL/PECL 100K compatible input resets the Laser Driver Logic - modulation current transitions to zero when asserted high.
OUT, $\overline{OUT}$	Open collector outputs from the modulation buffer drive these differential current outputs.
MC	An external voltage sets the main value of modulation current I_O.
R_{SET}	An external resistor sets the source current for modulation I_{mod}.
NC	These pins are not connected.

TRUTH TABLE(1)

D	$\overline{D}$	CLK	$\overline{CLK}$	MR	OUT	$\overline{OUT}$
L	H	Z	ZZ	L	H	L
H	L	Z	ZZ	L	L	H
X	X	X	X	H	H	L

NOTE:

1. L = LOW, H = HIGH, Z = LOW-to-HIGH transition, ZZ = HIGH-to-LOW transition, X = don't care.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{CC}	Power Supply Voltage (V_{CC} = 0V)	0 to -7.0	V
V_{IN}	Input Voltage (V_{CC} = 0V)	0 to -6.0	V
I_O	Output Current	75	mA
T_A	Operating Temperature Range	-40 to +85	˚C
P_{tot}	Power Dissipation	500	mW

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

OPERATIONING CONDITIONS(1)

Symbol	Rating	Value	Unit
V_{EE}	Power Supply Voltage	-4.75 to -5.25	V
R_{SET}	Resistor to Adjust Current	10 to 100	Ω
R_{EXT}	Resistor to Dissipate Power	10 to 50	Ω
R_{SER}	Laser Diode Serial Resistor	0 to 50	Ω

NOTE:

1. The voltage drop across R_{EXT} and R_{SER} should not be greater than 2V.

DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = V_{CCO} = 0V; V_{EE} = -5.0V ± 5%

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IH}	Input HIGH Voltage (D, CLK, MR)	-1165	—	-880	-1165	—	-880	-1165	—	-880	-1165	—	-880	mV
V_{IL}	Input LOW Voltage (D, CLK, MR)	-1810	—	-1475	-1810	—	-1475	-1810	—	-1475	-1810	—	-1475	mV
V_{Imod}	Input Voltage (Modulation Control)	V_{EE}	—	V_{CC}	V_{EE}	—	V_{CC}	V_{EE}	—	V_{CC}	V_{EE}	—	V_{CC}	V
V_{BB}	Output Reference Voltage	-1380	—	-1260	-1380	—	-1260	-1380	—	-1260	-1380	—	-1260	mV
I_{IH}	Input HIGH Current (D, CLK, MR)	—	—	150	—	—	150	—	—	150	—	—	150	µA
I_{Imod}	Input Current (Modulation Control)	—	—	150	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current[2] (D, CLK, MR)	0.5	—	—	0.5	—	—	0.5	—	—	0.5	—	—	µA
I_{CC}	Supply Current[3]	8	14	25	8	14	25	8	14	25	8	14	25	mA
I_{OH}	Output HIGH Current[4] (MR LOW)[5]	60	64 —	68 —	60 5	64 —	68 —	60 5	64 —	68 —	60 5	64 —	68 —	mA 5
I_{OL}	Output LOW Current (MR HIGH)	—	—	500	—	—	500	—	—	500	—	—	500	µA
I_{OR}	Output Current Ringing[6]	—	—	10	—	—	10	—	—	10	—	—	10	%
I_{Omod}	Laser Diode Modulation Current Range	5	—	60	5	—	60	5	—	60	5	—	60	mA

NOTE:

1. R_{SET} = 10Ω ± 1%
2. V_I = V_{IL}(Min.)
3. V_{Imod} = V_{CC}
4. V_{Imod} = -3.5V
5. V_{Lmod} = -0.8V
6. I_{OH} = 5 to 60mA

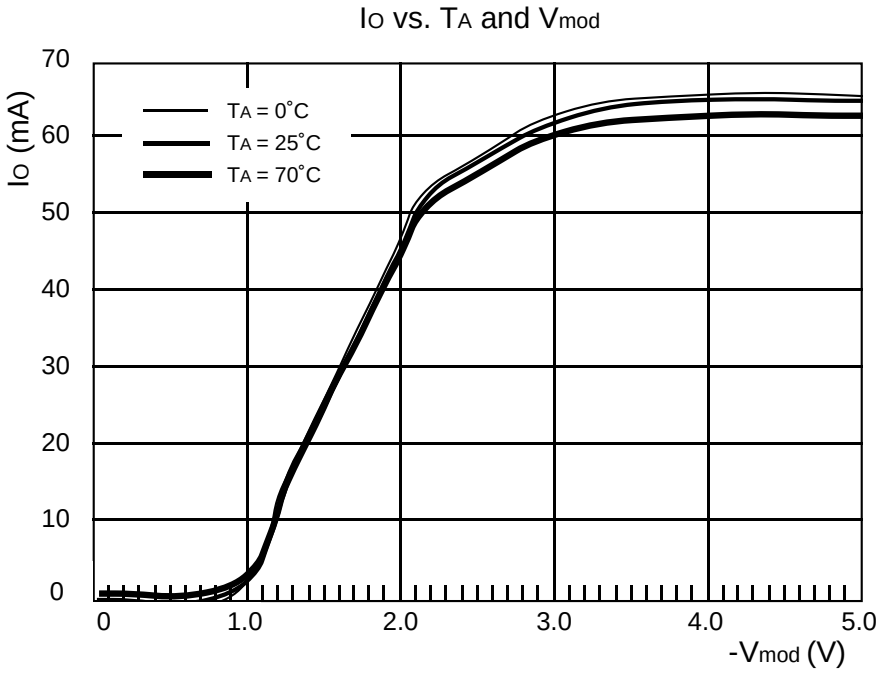
AC ELECTRICAL CHARACTERISTICS[1]

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{pd} CLK	Propagation Delay CLK - OUT	—	—	1000	—	—	1000	—	—	1000	—	—	1000	ps
t_{pd} MR	Propogation Delay MR - OUT	—	—	1000	—	—	1000	—	—	1000	—	—	1000	ps
t_r t_f	Rise/Fall Time (20% to 80%)	—	—	400	—	—	400	—	—	400	—	—	400	ps
t_S	Set-up Time	100	—	—	100	—	—	100	—	—	100	—	—	ps
t_H	Hold Time	500	—	—	500	—	—	500	—	—	500	—	—	ps
t_{PW}	Minimum Pulse Width (CLK, MR)	400	—	—	400	—	—	400	—	—	400	—	—	ps

NOTE:

1. R_{SET} = 10Ω ± 1%, R_{EXT} = R_{SER} = 50Ω ± 1%

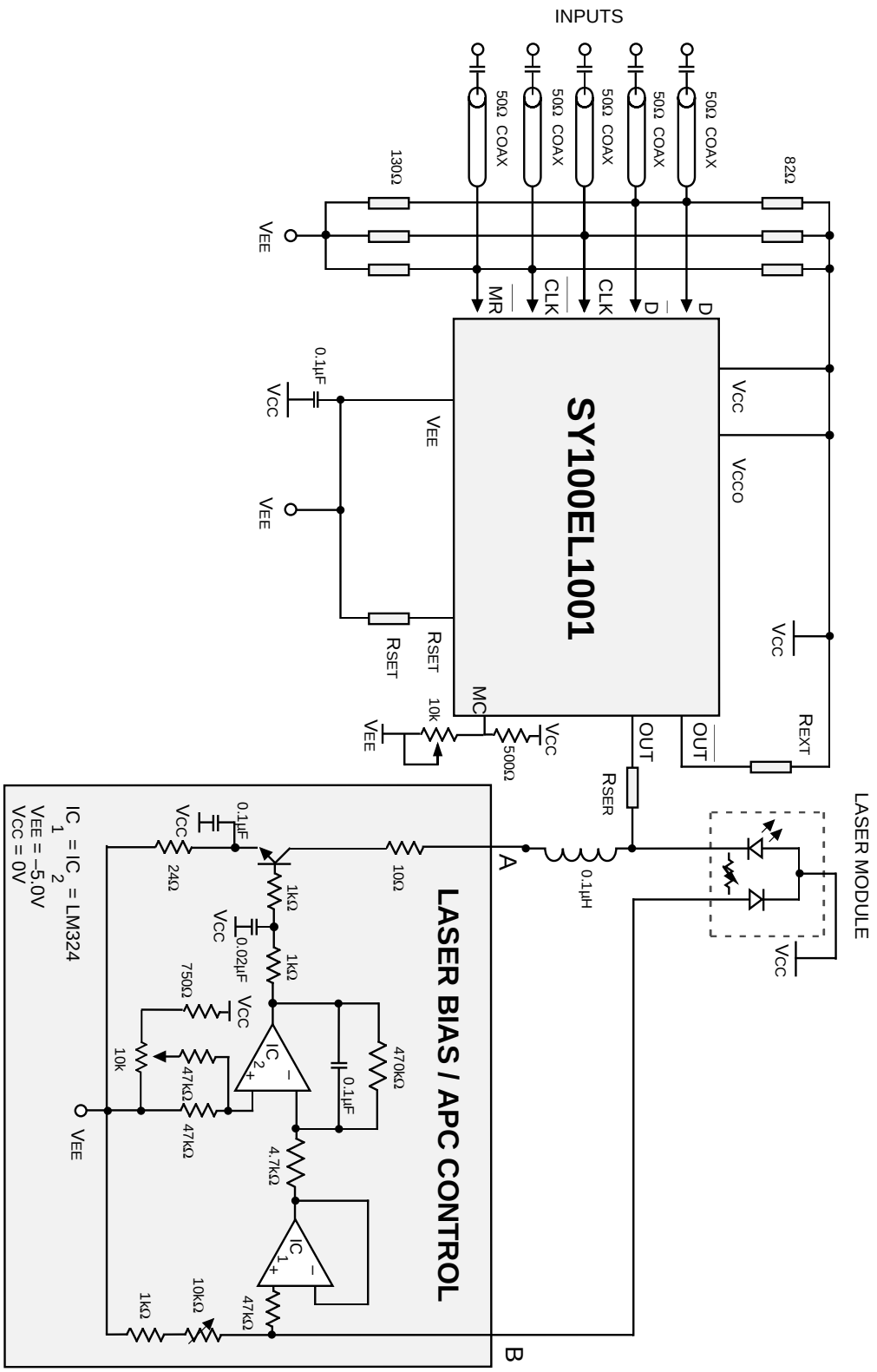
PERFORMANCE CURVES



PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100EL1001ZC	Z16-2	Commercial
SY100EL1001ZCTR	Z16-2	Commercial

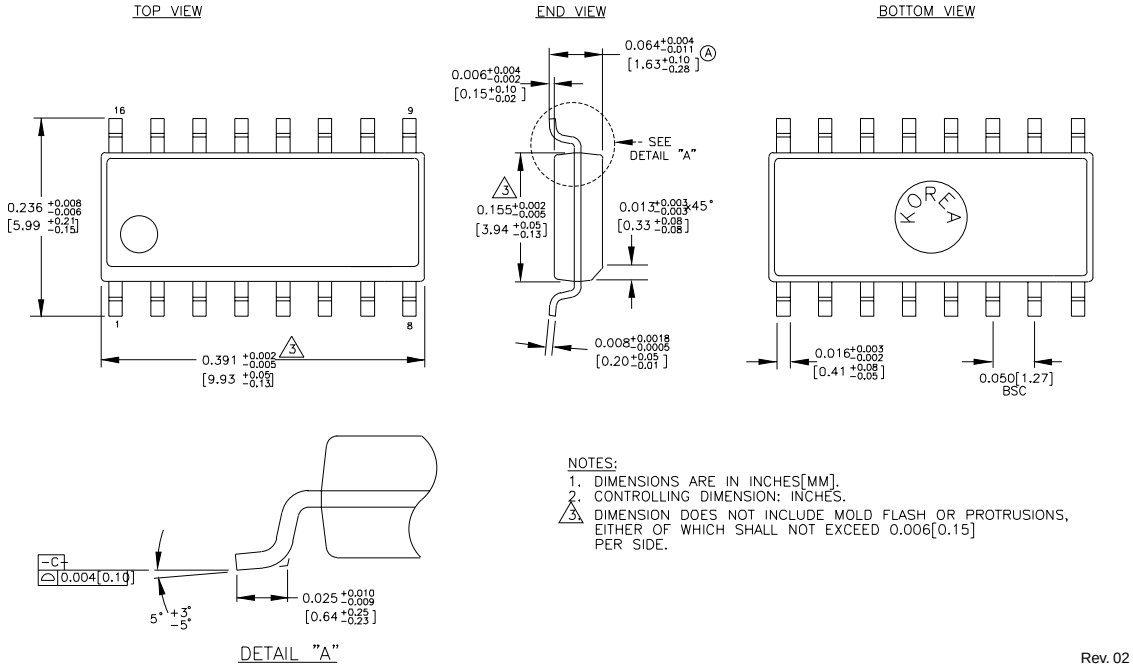
APPLICATION EXAMPLE



NOTES:

1. Split 100K ECL terminations are 82Ω and 130Ω to V_{CC} and V_{EE} respectively.
2. Recommended power supply bypass capacitors are 0.1µF with optional 10µF Tantalum in parallel.
3. High frequency design techniques are required for board layout. A double sided or multilayer board is recommended in conjunction with a low impedance ground plane and properly terminated transmission lines for all signal paths.
4. V_{BB} voltage pin may be used as reference for single ended input applications.

16 LEAD SOIC .150" WIDE (Z16-2)



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