# Compact +30V/±15V 256-Position Digital Potentiometer

Preliminary Technical Data

# AD5290

## FEATURES

**256-position**
**+2.7V to +30V Single Supply Operation**
**±2.7V to ±15V Dual Supply Operation**
**End-to-end resistance 10 kΩ, 50 kΩ, 100 kΩ**
**Low temperature coefficient 35 ppm/°C**
**Power-on preset to midscale**
**SPI compatible interface**
**Automotive temperature range –40°C to +105°C**
**Compact MSOP-10 (3 mm × 4.9 mm) package**

## APPLICATIONS

**Programmable Gain and Offset**
**Programmable Power Supply**
**Industrial Actuator Control**
**LED Array Driver**
**Audio Volume Control**
**General Purpose DAC Replacement**
**Mechanical Potentiometer Replacement**

## GENERAL OVERVIEW

The AD5290 is a low cost, compact 2.9 mm × 3 mm +30V/±15V, 256-position digital potentiometer. This device performs the same electronic adjustment function as mechanical potentiometers or variable resistors, with enhanced resolution, solid-state reliability, and superior low temperature coefficient performance.

The wiper settings are controllable through an SPI compatible digital interface. The resistance between the wiper and either end point of the fixed resistor varies linearly with respect to the digital code transferred into the RDAC latch.

The AD5290 is available in 10k, 50k, and 100kΩ in compact MSOP-10 package. AD5290 can be operated from a single supply +2.7 V to +30 V or dual supply ±2.7 V to ±15 V. All parts are guaranteed to operate over the automotive temperature range of -40°C to +105°C.

## FUNCTIONAL BLOCK DIAGRAM

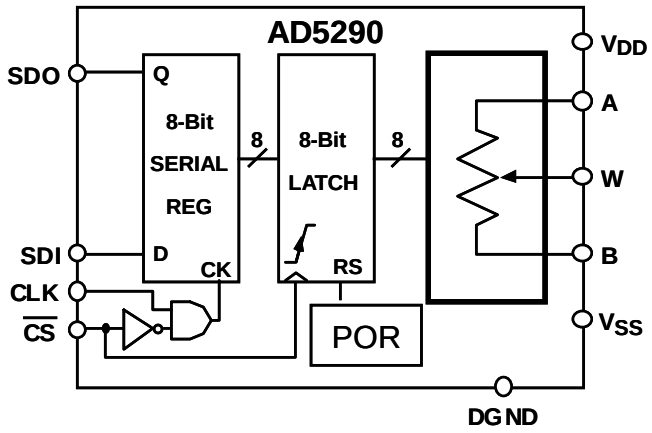


*Figure 1.*

Note:
The terms *digital potentiometer* and *RDAC* are used interchangeably.

**Rev. PrC**


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# ELECTRICAL CHARACTERISTICS—10 kΩ, 50 kΩ, 100 kΩ VERSIONS

($V_{DD}/V_{SS}$ = ±15V±10% or ±5V±10%, $V_A = +V_{DD}$, $V_B = V_{SS}$/0V, -40°C < $T_A$ < +105°C unless otherwise noted)

**Table 1.**

| Parameter | Symbol | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| DC CHARACTERISTICS—RHEOSTAT MODE | | | | | | |
| Resistor Differential Nonlinearity[2] | R-DNL | $R_{WB}$, $V_A$ = no connect | –1 | ±0.1 | +1 | LSB |
| Resistor Integral Nonlinearity[2] | R-INL | $R_{WB}$, $V_A$ = no connect | –2 | ±0.25 | +2 | LSB |
| Nominal Resistor Tolerance[3] | $\Delta R_{AB}$ | $T_A$ = 25°C | –30 | | +30 | % |
| Resistance Temperature Coefficient | $(\Delta R_{AB}/R_{AB})/\Delta T*10^6$ | $V_{AB} = V_{DD}$, Wiper = no connect | | 35 | | ppm/°C |
| Wiper Resistance | $R_W$ | $V_{DD}$ = 30 V | | 50 | 120 | Ω |
| | | $V_{DD}$ = 5 V | | 200 | 400 | Ω |
| DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE | | | | | | |
| Resolution | N | | | | 8 | Bits |
| Differential Nonlinearity[4] | DNL | | –1 | ±0.1 | +1 | LSB |
| Integral Nonlinearity[4] | INL | | –1 | ±0.3 | +1 | LSB |
| Voltage Divider Temperature Coefficient | $(\Delta V_W/V_W)/\Delta T*10^6$ | Code = 0x80 | | 5 | | ppm/°C |
| Full-Scale Error | $V_{WFSE}$ | Code = 0xFF | –3 | –1 | 0 | LSB |
| Zero-Scale Error | $V_{WZSE}$ | Code = 0x00 | 0 | 1 | 3 | LSB |
| RESISTOR TERMINALS | | | | | | |
| Voltage Range[5] | $V_{A,B,W}$ | | $V_{SS}$ | | $V_{DD}$ | V |
| Capacitance[6] A, B | $C_{A,B}$ | f = 1 MHz, measured to GND, Code = 0x80 | | 45 | | pF |
| Capacitance[6] W | $C_W$ | f = 1 MHz, measured to GND, Code = 0x80 | | 60 | | pF |
| Common-Mode Leakage | $I_{CM}$ | $V_A = V_B = V_W$ | | 1 | | nA |
| DIGITAL INPUTS AND OUTPUTS | | | | | | |
| Input Logic High | $V_{IH}$ | $V_{DD}$ = +5V or +15V | 2.4 | | | V |
| Input Logic Low | $V_{IL}$ | $V_{DD}$ = +5V or +15V | | | 0.8 | V |
| Output Logic High | $V_{OH}$ | $R_L$ = 2.2 kΩ to +5 V | 4.9 | | | V |
| Output Logic Low | $V_{OL}$ | $I_{OL}$ = 1.6mA, $V_{LOGIC}$ = +5V, $V_{DD}$ = +15V | | | 0.4 | V |
| Input Current | $I_I$ | $V_{IN}$ = 0 V or +15 V | | | ±1 | µA |
| Input Capacitance | $C_I$ | | | 5 | | pF |
| POWER SUPPLIES | | | | | | |
| Power Supply Range | $V_{DD}/V_{SS}$ | Dual Supply Range | ±2.7 | | ±16.5 | V |
| Power Supply Range | $V_{DD}$ | Single Supply Range, $V_{SS}$ = 0 V | +2.7 | | +30 | V |
| Supply Current6 | $I_{DD}$ | $V_{IH}$ = 5 V or $V_{IL}$ = 0 V, $V_{DD}$ = +5 V | | 0.1 | 10 | µA |
| Supply Current | $I_{DD}$ | $V_{IH}$ = 5 V or $V_{IL}$ = 0 V, $V_{DD}$ = +15 V | | 0.75 | 2 | mA |
| Supply Current | $I_{SS}$ | $V_{IH}$ = 5 V or $V_{IL}$ = 0 V, $V_{SS}$ = -5 V or –15 V | | 0.02 | 0.1 | mA |
| Power Dissipation[7] | $P_{DISS}$ | $V_{IH}$ = 5 V or $V_{IL}$ = 0 V, $V_{DD}$ = +15 V, $V_{SS}$ = -15 V | | 11 | 30 | mW |
| Power Supply Sensitivity | PSS | $\Delta V_{DD}$ = +15V ±10%, or $\Delta V_{SS}$ = -15V ±10%, Code = Midscale | | ±0.01 | ±0.02 | %/% |
| DYNAMIC CHARACTERISTICS[6, 8] | | | | | | |
| Bandwidth –3dB | BW | $R_{AB}$ = 10 kΩ/50 kΩ/100 kΩ, Code = 0x80 | | 525/125/60 | | kHz |

| | | | | | | |
|---|---|---|---|---|---|---|
| Total Harmonic Distortion | $THD_W$ | $V_A$ =1 V rms, $V_B$ = 0 V, f = 1 kHz, $R_{AB}$ = 10 kΩ | | 0.05 | | % |
| $V_W$ Settling Time (10 kΩ/50 kΩ/100 kΩ) | $t_S$ | $V_A$ = 5 V, $V_B$ = 0 V, ±1 LSB error band | | 4 | | µs |
| Resistor Noise Voltage Density | $e_{N\_WB}$ | $R_{WB}$ = 25 kΩ | | 14 | | nV/√Hz |

# TIMING CHARACTERISTICS— 10 kΩ, 50 kΩ, 100 kΩ VERSIONS

($V_{DD}/V_{SS}$ = ±15V±10% or ±5V±10%, $V_A = +V_{DD}$, $V_B$ = 0V, -40°C < $T_A$ < +105°C unless otherwise noted.)

**Table 2.**

| Parameter | Symbol | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| SPI INTERFACE TIMING CHARACTERISTICS[6, 8,9] (Specifications Apply to All Parts) | | | | | | |
| Clock Frequency | $f_{CLK}$ | | | | 4 | MHz |
| Input Clock Pulsewidth | $t_{CH}$, $t_{CL}$ | Clock level high or low | 120 | | | ns |
| Data Setup Time | $t_{DS}$ | | 30 | | | ns |
| Data Hold Time | $t_{DH}$ | | 20 | | | ns |
| CLK to SDO Propagation Delay | $t_{PD}$ | $R_{PU}$ = 1KΩ, $C_L$ < 20pF | 10 | | 100 | ns |
| $\overline{CS}$ Setup Time | $t_{CSS}$ | | 120 | | | ns |
| $\overline{CS}$ High Pulsewidth | $t_{CSW}$ | | 150 | | | ns |
| CLK Fall to $\overline{CS}$ Fall Hold Time | $t_{CSH0}$ | | TBD | | | ns |
| CLK Fall to $\overline{CS}$ Rise Hold Time | $t_{CSH1}$ | | 120 | | | ns |
| $\overline{CS}$ Rise to Clock Rise Setup | $t_{CS1}$ | | 120 | | | ns |

NOTES
1. Typical specifications represent average readings at +25°C and $V_{DD}$ = 5 V.
2. Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
3. $V_{AB} = V_{DD}$, Wiper ($V_W$) = no connect.
4. INL and DNL are measured at $V_W$ with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A$=$V_{DD}$ and $V_B$=0 V.
5. Resistor terminals A, B, W have no limitations on polarity with respect to each other.
6. Guaranteed by design and not subject to production test.
7. $P_{DISS}$ is calculated from ($I_{DD} \times V_{DD}$+ $I_{SS} \times V_{SS}$) CMOS logic level inputs result in minimum power dissipation.
8. All dynamic characteristics use $V_{DD}$ / $V_{SS}$ = ±5 V.
9. See timing diagram for location of measured values. All input control voltages are specified with $t_R = t_F$ = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

# ABSOLUTE MAXIMUM RATINGS[1]

($T_A$ = +25°C, unless otherwise noted.)

**Table 3.**

| Parameter | Value |
|---|---|
| $V_{DD}$ to VSS | –0.3 V to +33 V |
| $V_{DD}$ to GND | –0.3 V to +33 V |
| $V_{SS}$ to GND | +0.3 V to –16.5 V |
| $V_A$, $V_B$, $V_W$ to GND | $V_{SS}$ , $V_{DD}$ |
| Maximum Current | |
| $I_{WB}$, $I_{WA}$ Pulsed | ±20 mA |
| $I_{WB}$ Continuous ($R_{WB}$ ≤ 1 kΩ, A open)[1] | ±5 mA |
| $I_{WA}$ Continuous ($R_{WA}$ ≤ 1 kΩ, B open)[1] | ±5 mA |
| Digital Inputs Voltage to GND | $V_{DD}$ + 0.3 V |
| Digital Output Voltage to GND | 0 V, +30 V |
| Operating Temperature Range | –40°C to +105°C |
| Maximum Junction Temperature ($T_{JMAX}$) | 150°C |
| Storage Temperature | –65°C to +150°C |
| Lead Temperature (Soldering, 10 – 30 sec) | 245°C |
| Thermal Resistance[2] $\theta_{JA}$: MSOP-10 | 230°C/W |

NOTES

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Package power dissipation = $(T_{JMAX} – T_A)/\theta_{JA}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

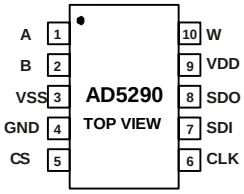


*Figure 2. AD5290 Pin Configuration*

**Table 7. AD5290 Pin Function Descriptions**

| Pin | Menmonic | Description |
|---|---|---|
| 1 | A | A Terminal. $V_{SS} \leq V_A \leq V_{DD}$ |
| 2 | B | B Terminal. $V_{SS} \leq V_B \leq V_{DD}$ |
| 3 | $V_{SS}$ | Negative Supply. Connect to zero volts for single supply applications. |
| 4 | GND | Digital Ground. |
| 5 | $\overline{CS}$ | Chip Select Input, Active Low. When $\overline{CS}$ returns high, data will be loaded into the Wiper Register |
| 6 | CLK | Serial Clock Input. Positive edge triggered |
| 7 | SDI | Serial Data Input Pin. Shifts in one bit at a time on positive clock CLK edges. MSB loaded first. |
| 8 | SDO | Serial Data Output Pin. Internal N-Ch FET with open-drain output that requires external pull-up resistor. It shifts out the previous 8 SDI bits that allows daisy-chain operation of multiple packages |
| 9 | $V_{DD}$ | Positive Power Supply |
| 10 | W | W Terminal. $V_{SS} \leq V_W \leq V_{DD}$ |

# SPI Interface

**Table 4. AD5290 Serial Data-Word Format**

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| MSB | | | | | | | LSB |
| $2^7$ | | | | | | | $2^0$ |

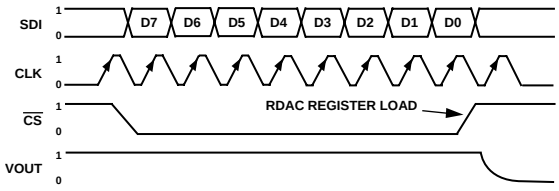


*Figure 3. AD5290 SPI Interface Timing Diagram ($V_A$ = VDD, $V_B$ = 0 V, $V_W = V_{OUT}$)*

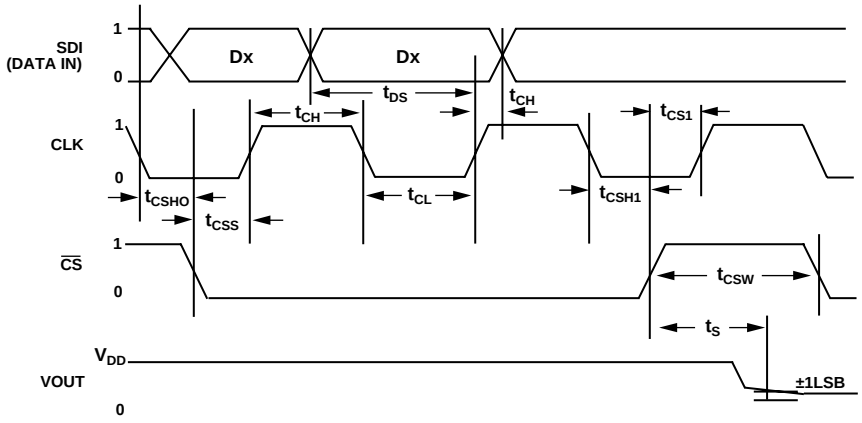


*Figure 2. SPI Interface Detailed Timing Diagram ($V_A$ = VDD, $V_B$ = 0 V, $V_W = V_{OUT}$)*

# OPERATION

The AD5290 is a 256-position digitally controlled variable resistor device that can be controlled digitally through SPI interface.

An internal power-on preset places the wiper at midscale during power-on, which simplifies the fault condition recovery at power-up.

## DETERMINING THE VARIABLE RESISTANCE AND VOLTAGE

### *Rheostat Mode Operation*

If only the W-to-B or W-to-A terminals are used as variable resistors, the unused terminal can be opened or shorted with W. This operation is called rheostat mode (Figure 3).

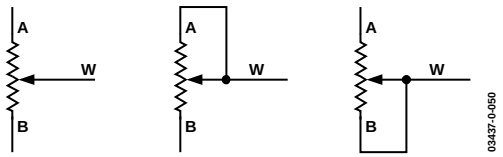


*Figure 3. Rheostat Mode Configuration*

The nominal resistance ($R_{AB}$) of the RDAC has 256 contact points accessed by the wiper terminal, plus the B terminal contact if $R_{WB}$ is considered. The 8-bit data in the RDAC latch is decoded to select one of the 256 settings. Assuming that a 10 kΩ part is used, the wiper's first connection starts at the B terminal for data 0x00. Such connection yields a minimum of 60 Ω resistance between terminals W and B because of the 60 Ω wiper contact resistance. The second connection is the first tap point, which corresponds to 99 Ω ($R_{WB} = (1) \times R_{AB}/256 + R_W$) for data 0x01, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10020 Ω ($(255) \times R_{AB}/256 + R_W$). Figure 6 shows a simplified diagram of the equivalent RDAC circuit. The general equation determining $R_{WB}$ is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \quad (1)$$

where:

*D* is the decimal equivalent of the 8-bit binary code.
$R_{AB}$ is the end-to-end resistance.
$R_W$ is the wiper resistance contributed by the on-resistance of the internal switch.

**Table 1. $R_{WB}$ vs. Codes; $R_{AB}$ = 10 kΩ and the A Terminal Is Opened**

| D (Dec) | $R_{WB}$ (Ω) | Output State |
|---|---|---|
| 255 | 10020 | Full-Scale ($R_{AB} + R_W$) |
| 128 | 5060 | Midscale |
| 1 | 99 | 1 LSB |
| 0 | 60 | Zero-Scale (Wiper Contact Resistance) |

Since a finite wiper resistance of 60 Ω is present in the zero-scale condition, care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a complementary resistance $R_{WA}$. When these terminals are used, the B terminal can be opened or shorted to W. Setting the resistance value for $R_{WA}$ starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \quad (2)$$

**Table 2. $R_{WA}$ vs. Codes; $R_{AB}$ =10 kΩ and B Terminal Is Opened**

| D (Dec) | $R_{WA}$ (Ω) | Output State |
|---|---|---|
| 255 | 60 | Full-Scale |
| 128 | 5060 | Midscale |
| 1 | 10020 | 1 LSB |
| 0 | 10060 | Zero-Scale |

The typical distribution of the resistance tolerance from device to device is process lot dependent, and it is possible to have ±30% tolerance.

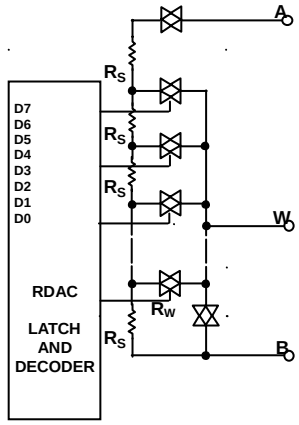


*Figure 6. AD5290 Equivalent RDAC Circuit*

### *Potentiometer Mode Operation*

If all three terminals are used, the operation is called the potentiometer mode. The most common configuration is the voltage divider operation (Figure 7).

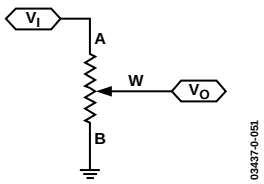


*Figure 7. Potentiometer Mode Configuration*

Ignoring the effect of the wiper resistance, the transfer function is simply

$$V_W(D) = \frac{D}{256} V_A \quad (3)$$

A more accurate calculation, which includes the wiper resistance effect, yields

$$V_W(D) = \frac{\frac{D}{256} R_{AB} + R_W}{R_{AB} + 2R_W} V_A \quad (4)$$

If there is an applied voltage at the B terminal, then the transfer function becomes

$$V_W(D) = \frac{D}{256} V_A + \frac{256 - D}{256} V_B \quad (5)$$

Unlike in rheostat mode operation where the absolute tolerance is high, potentiometer mode operation yields an almost ratiometric function of D/256 with a relatively small error contributed by the RW terms, and therefore the tolerance effect is almost cancelled. Although the thin film step resistor $R_S$ and CMOS switches resistance $R_W$ have very different temperature coefficients, the ratiometric adjustment also reduces the overall temperature coefficient effect to 5 ppm/°C, except at low value codes where $R_W$ dominates.

Potentiometer mode operations include others such as op amp input, feedback resistor networks, and other voltage scaling applications. A, W, and B terminals can in fact be input or output terminals provided that $|V_A|$, $|V_W|$, and $|V_B|$ do not exceed $|V_{DD}|$ and $|V_{SS}|$.

## SPI COMPATIBLE 3-WIRE SERIAL BUS

The AD5290 contains a 3-wire SPI compatible digital interface (SDI, $\overline{CS}$, and CLK). The 8-bit serial word must be loaded MSB first. The format of the word is shown in Table .

The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. $\overline{CS}$ should start high, when it goes low, the clock loads data into the serial register on each positive clock edge (see Figure 3).

The data setup and data hold times in the specification table determine the valid timing requirements. The AD5290 uses an 8-bit serial input data register word that is transferred to the internal RDAC register when the $\overline{CS}$ returns to logic high. If dataword contains more than 8-bit, the extra MSB bits will be ignored.

## ESD PROTECTION

All digital inputs are protected with a series input resistor and parallel Zener ESD structures shown in 8 and Figure 9. This applies to the digital input pins SDI, CLK, and $\overline{CS}$.

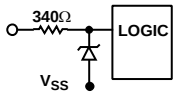


*Figure 8. ESD Protection of Digital Pins*

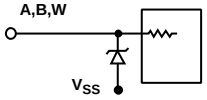


*Figure 9. ESD Protection of Resistor Terminals*

## TERMINAL VOLTAGE OPERATING RANGE

The AD5290 $V_{DD}$ and GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on terminals A, B, and W that exceed $V_{DD}$ or GND will be clamped by the internal forward biased diodes (see Figure 10).

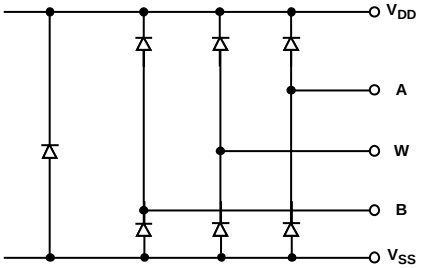


*Figure 10. Maximum Terminal Voltages Set by $V_{DD}$ and $V_{SS}$*

## POWER-UP SEQUENCE

Since the ESD protection diodes limit the voltage compliance at terminals A, B, and W (see Figure 10), it is important to power $V_{DD}$–to-GND and $V_{SS}$-to-GND before applying any voltage to terminals A, B, and W; otherwise, the diode will be forward biased such that $V_{DD}$ will be powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND, $V_{SS}$,$V_{DD}$, digital inputs, and then

$V_{A/B/W}$. The relative order of powering $V_A$, $V_B$, $V_W$, and the digital inputs is not important as long as they are powered after $V_{DD}$ and $V_{SS}$ with respect to GND.

## LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to employ compact, minimum lead length layout design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also a good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with disc or chip ceramic capacitors of 0.01 µF to 0.1 µF. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 4). Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

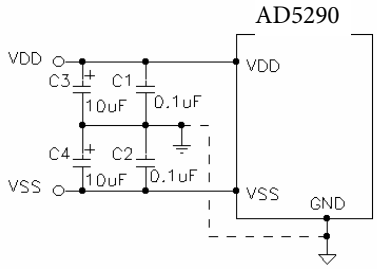


*Figure 4. Power Supply Bypassing*

## DAISY CHAIN OPERATION

The serial data output pin (SDO) can be used to daisy chain multiple devices for simultaneous operations, see Figure 12. The SDO pin contains an open drain N-Ch FET and requires a pull-up resistor. Users need to tie the SDO pin of one package to the SDI pin of the next package. If many devices are daisy-chained, users may need to increase the clock period to accommodate the time delay introduced by the pull-up resistors and the capacitive loading at the SDO-SDI interface, see Figure 12.

If two AD5290 are daisy chained, this requires total 16 bits of data. The first 8 bits goes to U2 and the second 8 bits goes to U1. The $\overline{CS}$ should be kept low until all 16 bits are clocked into their respective serial registers. The $\overline{CS}$ is then pulled high to complete the operation.

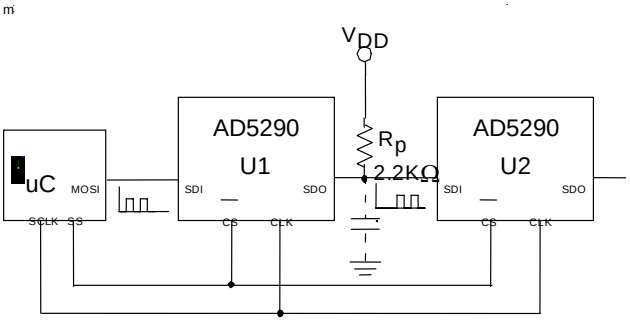


*Figure 12. Daisy Chain Configuration*

# OUTLINE DIMENSIONS

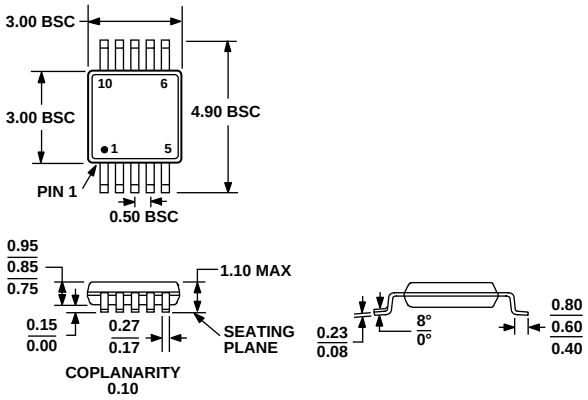


*Figure 5. 10-Lead Mini Small Outline Package [MSOP]*
*(RM-10)*
*Dimensions shown in millimeters*

## Ordering Guide

| Model[1] | $R_{AB}$ (kΩ) | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|---|
| AD5290YRMZ10 | 10 | –40°C to +105°C | MSOP-10 | RM-10 | D4U |
| AD5290YRMZ10-RL7 | 10 | –40°C to +105°C | MSOP-10 | RM-10 | D4U |
| AD5290YRMZ50 | 50 | –40°C to +105°C | MSOP-10 | RM-10 | D4T |
| AD5290YRMZ50-RL7 | 50 | –40°C to +105°C | MSOP-10 | RM-10 | D4T |
| AD5290YRMZ100 | 100 | –40°C to +105°C | MSOP-10 | RM-10 | D4V |
| AD5290YRMZ100-RL7 | 100 | –40°C to +105°C | MSOP-10 | RM-10 | D4V |
| AD5290EVAL | | | Evaluation Board | | |

NOTES:
1. Z in Model Number denotes Lead Free Package

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.