BATRON

Specification for
BT 96040AV-FSTF-12-I2C-COG

Version March 2004

DATA MODUL AG Landsberger Str. 322 80687 München Tel.: 089/ 56017-**0** Fax 089/ 56017-119 www.data-modul.de

DOCUMENT REVISION HISTORY 1:

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2004.03.23	First Release. Based on a.) Test Specification: VL-TS-COG-BT96040-03 REV. A, 2003-10-31. b.) VL-QUA-012A-S, REV. P, APR/2003 (English version). According to VL-QUA-012A-S, LCD size is small because Unit Per Laminate=35 which is more than 6pcs/Laminate.	CHEN HUI JUAN	SUNNY LEE

CONTENTS

Specification
of
LCD Module Type
Item No.: COG-BT96040-03

1. General Description

- É 96 x 40 dots FSTN Black & White Positive Transflective Dot Matrix LCD module.
- É Viewing Angle: 12 O'clock direction.
- É Driving duty: 1/40 Duty, 1/7.3 bias.
- É Driving IC: 'PHILIPS' PCF 8558U/2/F2 (Gold Bump) LCD controller/driver or equivalent.
- É COG.
- É Data interface: I^2C-bus.
- É Bonded pins.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	46.0(W) x 36.2(H) x 1.845(D) (Excluded pins)	mm
Viewing area	40.0(W)x 23.0(H)	mm
Active area	35.2(W)x 18.2(H)	mm
Display format	96 x 40	dots
Weight:	TBD	grams

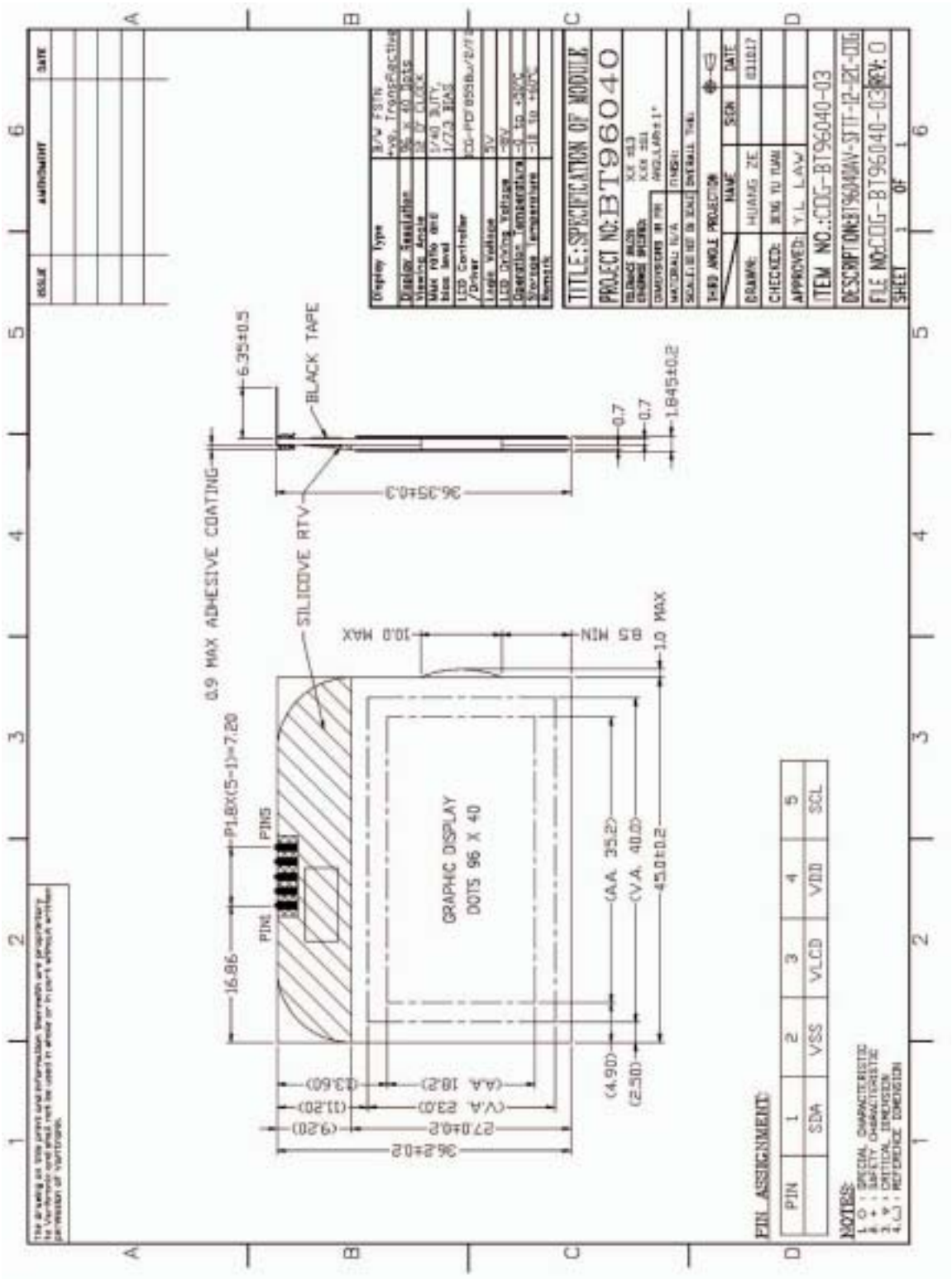


Figure 1: Module Specification.

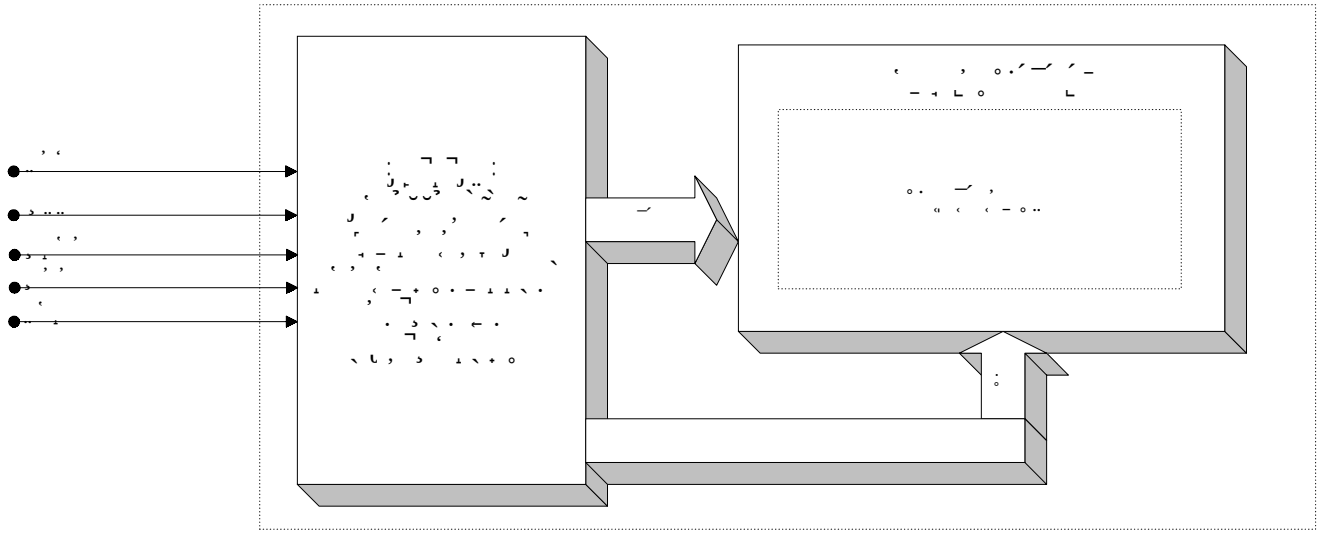


Figure 2: Block Diagram

3. Interface signals

Table 2

Pin No.	Symbol	Description
1	SDA	I^2C-bus serial data input/output
2	VSS	Ground (0V).
3	VLCD	Power supply for LCD driver.
4	VDD	Power supply for logic (+5V).
5	SCL	I^2C-bus serial clock input

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings(Ta = 25 ºC)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD - VSS	-0.5	+8.0	V
Input voltage range (SDA,SCL)	Vin	VSS-0.5	+8.0	V
Supply voltage (LCD)	Vop=VDD-VLCD	0	+11.0	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0∀C	+50∀C	-10∀C	+60∀C	Dry
Humidity	95% max. RH for Ta Ω 40∀C < 95% RH for Ta > 40∀C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ℑ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 ∀C, VDD = 5V∂5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		4.95	5.0	5.0 5	V
Operating voltage for LCD	Vop = VDD -VLCD	Ta= 0∀C,VDD =+5V, Character mode, Note 1	-	7.3	-	V
		Ta=+25 ∀C,VDD =+5V, Character mode, Note 1	6.9	7.1	7.3	V
		Ta=+50 ∀C,VDD =+5V, Character mode, Note 1	-	6.9	-	V
Operating supply current (Logic&LCD)	IDD	Character mode, VDD =5.0V	-	100	150	µA
		Checker board, VDD =5.0V	-	110	160	µA
Input signal voltage low (SDA, SCL)	Vil		VSS	-	0.3 VDD	V
Input signal voltage high (SDA, SCL)	Vih		0.7 VDD	-	VDD	V

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

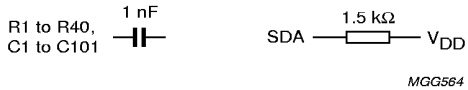
Ta = 0 ∀C to +50 ∀C, VDD = +5.0V∂5%, VSS=0V; V_{LCD}= VDD-3.5V to VDD-9V, VSS=0V.
Refer to Figure 3, I^2C Bus Timing Diagram of 'PHILIPS' PCF8558.

Table 6

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_{FR)}$	LCD frame frequency (internal oscillator)		37	62.5	94	Hz
$f_{OSC(ext)}$	external clock frequency		90	150	225	kHz
t_{PLCD}	driver delays	$V_{DD} - V_{LCD}$ = 9 V; with test loads	–	–	100	µs
I^2C-bus (see Fig.12)						
f_{SCL}	SCL clock frequency		–	–	400	kHz
t_{CLKL}	SCL LOW time		1.3	–	–	µs
t_{CLKH}	SCL HIGH time		0.6	–	–	µs
t_{BUF}	bus free time	between successive STOP and START conditions	1.3	–	–	µs
t_r	SCL and SDA rise time	note 1	–	–	300	ns
t_f	SCL and SDA fall time	note 1	20 + 0.1C_b	–	300	ns
$t_{SU;STA}$	START condition set-up time	repeated start codes only	0.6	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	STOP condition set-up time		0.6	–	–	µs
t_{SW}	tolerable spike width on bus	note 2	–	–	50	ns
C_b	capacitive load per bus line		–	–	400	pF

Notes

1. The rise and fall times specified here refer to the driver device (i.e. not PCF8558) and are part of the general fast I^2C-bus specification. However, when PCF8558 asserts an acknowledge on SDA, the fall time is given by parameter t_f. C_b = capacitive load per bus line.
2. The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of width $<t_{SW(max)}$.



AC test loads.

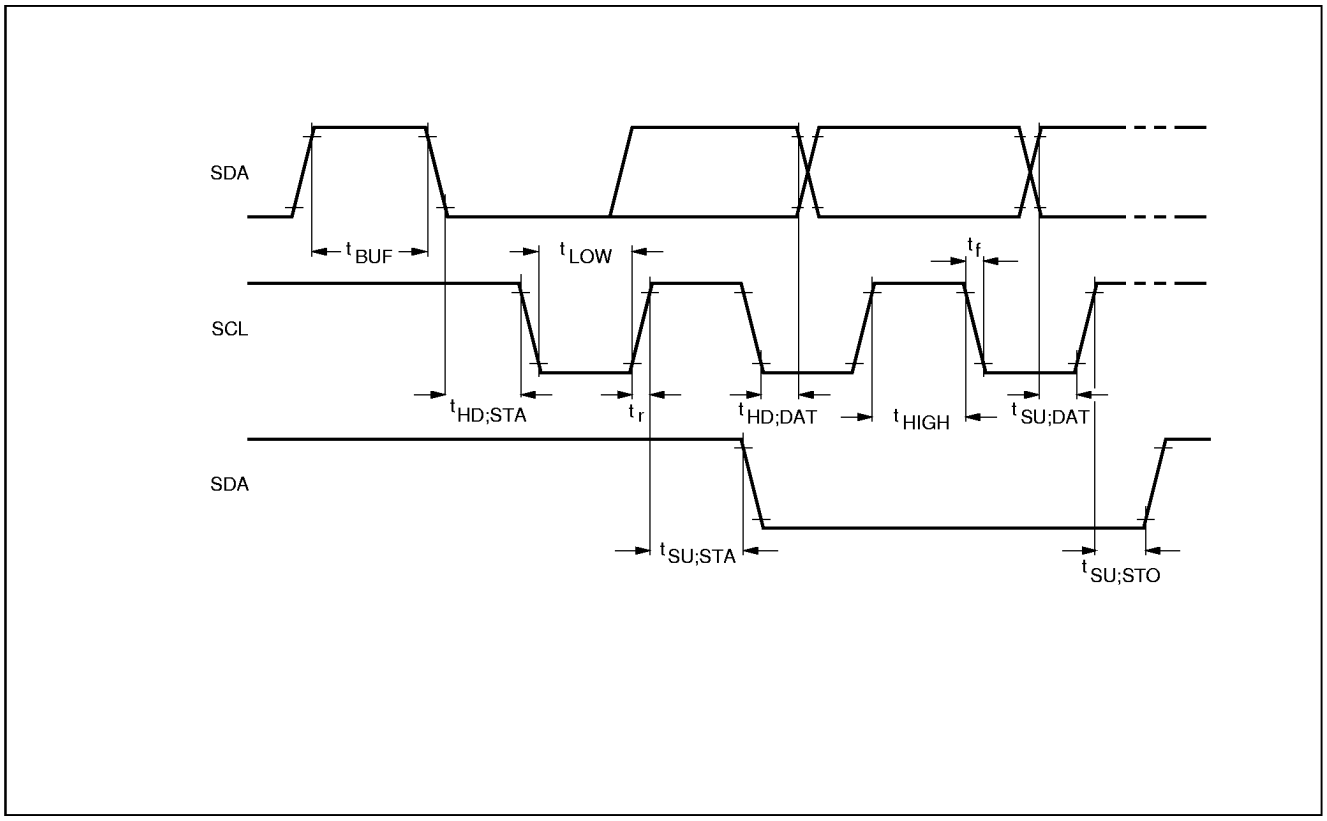


Figure 3: I²C-Bus Timing Diagram

6. LCD Cosmetic Conditions

Refer to VL-QUA-012A-S

- END -