GS820V32Q/T
4/5/6, 2.5V I/O, 2.0mA

64K x 32 Burst

80-133MHz (P/L)
66MHz Flow-Thru

Features

- Single 3.3V +5%/-5% power supply
- Separate VDDQ to allow 2.375V to 3.465V output supply level
- High frequency operation: 117MHz
- Fast access time: 4.5ns Clock to Q
- Low power: 0.5mA ISB and IDD static
- $\overline{FT}$ mode pin for either flow-thru or pipeline operation
- $\overline{LBO}$ mode pin for linear or interleave (Pentium™ and X86) burst mode
- Byte write ($\overline{BWE}$) and global write ($\overline{GW}$) operation
- 3 chip enable signals for easy depth expansion
- 2 cycles enable (pipeline mode) and 1 cycle disable to allow multiple bank without data buss contention
- Compatible to both 3.3V and 2.5V interface level
- Standard Industrial Temperature Option: -40 to +85C
- JEDEC standard 100 lead package:
  Q: QFP
  T: TQFP

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Functional Description

The GS820V32 is a 64Kx32 high performance synchronous SRAM with 2 bit burst counter. It is designed to provide L2 Cache for Pentium™ and other high performance CPU. Addresses (A0-15), data IOs (DQ1-32), chip enables ($\overline{CE1}$, CE2, $\overline{CE3}$), address control inputs ($\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$) and write control inputs ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$, $\overline{GW}$) are synchronous and are controlled by a positive edge triggered clock (CLK).

Output enable ($\overline{OE}$) and power down control (ZZ) are asynchronous. 2 mode control pins ($\overline{LBO}$ & $\overline{FT}$) define 4 operation modes of linear/interleave burst order and output flow-thru/pipeline.

Burst can be initiated with either $\overline{ADSP}$ or $\overline{ADSC}$ inputs. Subsequent burst address are generated internally and are controlled by $\overline{ADV}$. The burst sequence is either interleave order (Pentium™ and X86) or linear order and is defined by $\overline{LBO}$.

Output registers are provided and are controlled by $\overline{FT}$ mode pin. With $\overline{FT}$ mode pin, Output registers can be programmed in either pipeline mode for very high frequency operation (117MHz) or flow-thru mode for reduced latency.

Byte write operation can be obtained through byte write enable ($\overline{BWE}$) input combined with 4 individual byte write signals $\overline{BW}$1-4. In addition, global write ($\overline{GW}$) signal is also available to write all bytes at once.

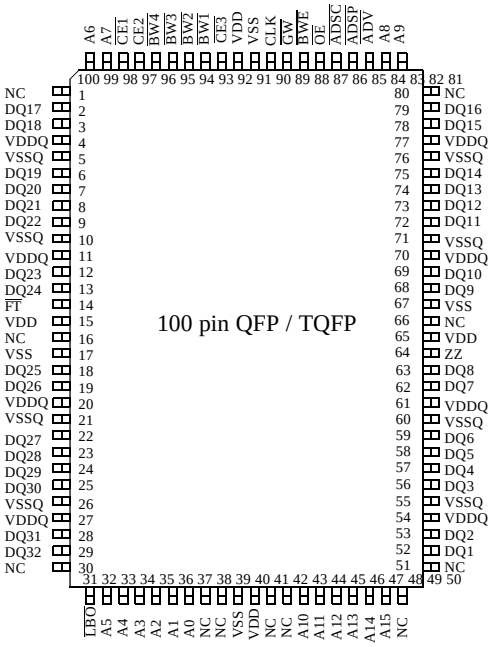
Low power state (standby mode) can be obtained either through the assertion of ZZ signal or simply stop the clock (CLK). In standby mode, memory data are still retained. Low power design of 0.5mA standby are provided on L version.

The GS820V32 operates from a 3.3V power supply and all inputs and outputs are LVTTL compatible. Separate output power (VDDQ) and ground (VSSQ) pins are employed to decouple output noise from internal circuit and VDDQ allow user the flexibility to employ lower output supply level like 2.5V. GS820V32's interface level is also compatble to 2.5V supply level.

The GS820V32 is implemented with GSI's high performance CMOS technology and is available in JEDEC standard 100 lead QFP (Q version) and TQFP (T version) package.

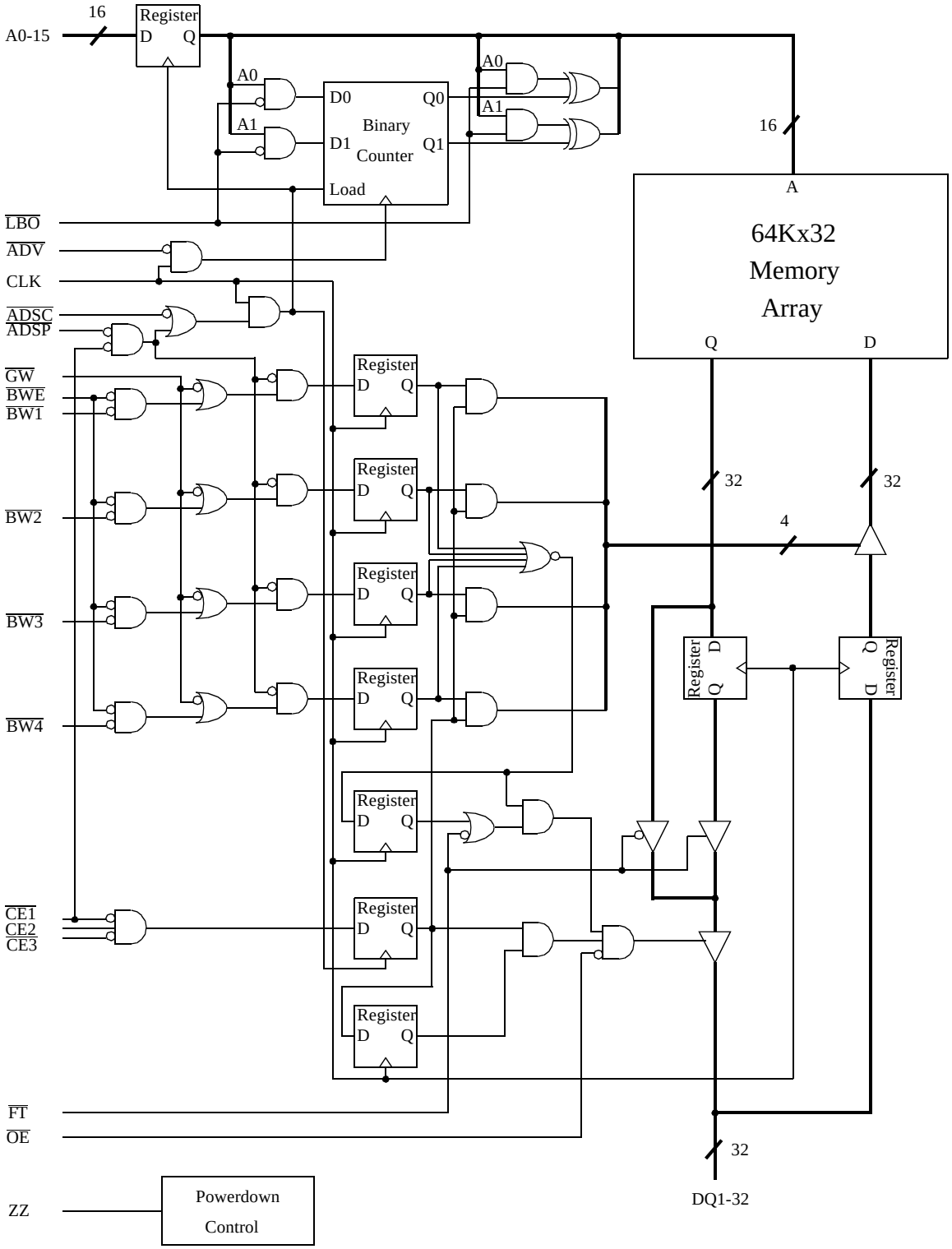
Pin configuration

Top view



A0-15	Address Inputs
CLK	Clock Input
$\overline{BWE}$	Byte Write Enable
$\overline{BW1}$,$\overline{BW2}$ $\overline{BW3}$,$\overline{BW4}$	Byte Write. $\overline{BW1}$ for DQ1-8; $\overline{BW2}$ for DQ9-16; $\overline{BW3}$ for DQ17-24; $\overline{BW4}$ for DQ25-32
$\overline{GW}$	Global Write Enable
$\overline{CE1}$,CE2, $\overline{CE3}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{ADV}$	Burst Address advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
DQ1-32	Data I/O
ZZ	Power down control
$\overline{FT}$	Flow-Thru mode
$\overline{LBO}$	Linear Burst mode
VDD	3.3V Power Supply
VSS	Ground
VDDQ	Output Power Supply, 2.375V to VDD (3.465Vmax)
VSSQ	Output Ground
NC	No Connect

Functional Block Diagram



Mode pin function

$\overline{LBO}$	Function
L	Linear Burst
H or NC	Interleaved Burst

$\overline{FT}$	Function
L	Flow-Thru
H or NC	Pipeline

Power down control

ZZ	Function
L or NC	Active
H	Standby IDD=ISB

Note: There are pull up devices on $\overline{LBO}$ and $\overline{FT}$ pins and pull down device on ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

Linear Burst sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

The burst wrap around to initial state upon completion

Interleaved Burst sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

The burst wrap around to initial state upon completion

Byte Write Function

Function	$\overline{SGW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write all bytes	L	X	X	X	X	X
Write all bytes	H	L	L	L	L	L
Write byte 1	H	L	L	H	H	H
Write byte 2	H	L	H	L	H	H
Write byte 3	H	L	H	H	L	H
Write byte 4	H	L	H	H	H	L

Note: H=logic high, L=logic low, NC= no connect

Synchronous truth table

Cycle	Address used	$\overline{CE1}$	CE2	$\overline{CE3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{BWx}$
Deselect	none	H	X	X	X	L	X	X
Deselect	none	L	L	X	X	L	X	X
Deselect	none	L	X	H	X	L	X	X
Deselect	none	L	L	X	L	X	X	X
Deselect	none	L	X	H	L	X	X	X
Read, begin burst	external	L	H	L	L	X	X	X
Read, begin burst	external	L	H	L	H	L	X	H
Read, continue burst	next	X	X	X	H	H	L	H
Read, continue burst	next	H	X	X	X	H	L	H
Read, suspend burst	current	X	X	X	H	H	H	H
Read, suspend burst	current	H	X	X	X	H	H	H
Write, begin burst	external	L	H	L	H	L	X	L
Write, continue burst	next	X	X	X	H	H	L	L
Write, continue burst	next	H	X	X	X	H	L	L
Write, suspend burst	current	X	X	X	H	H	H	L
Write, suspend burst	current	H	X	X	X	H	H	L

Note: 1. X=don't care, H=logic high, L=logic low
2. $\overline{BWx}$ is the logic function of $\overline{GW}$, $\overline{BWE}$, $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$. See Byte Write Function table for detail.
3. All inputs in the table must meet setup and hold on rising edge of CLK.

DQ Bus Control and Asynchronous $\overline{OE}$

Cycle	$\overline{OE}$	DQ
Read	L	Q
Read	H	Hi-Z
Write	X	Hi-Z; D
Deselect	X	Hi-Z

Note: On the write cycle that follows read cycle, $\overline{OE}$ need to be held high prior to the start of write cycle to tri-state DQ buss and allow data input to SRAM.

Absolute Maximum Ratings (Voltage reference to VSS=0V)

Parameter	*Symbol*	*Rating*	*Unit*
Supply Voltage	VDD	-0.5 to 4.6	V
Output Supply Voltage	VDDQ	-0.5 to VDD	V
CLK Input Voltage	VCLK	-0.5 to 6	V
Input Voltage	VIN	-0.5 to VDD+0.5 (≤ 4.6 V max.)	V
Output Voltage	VOUT	-0.5 to VDD+0.5 (≤ 4.6 V max.)	V
Power Dissipation	PD	1.5	W
Operating Temperature	Topr	0 to 70	^{o}C
Storage Temperature	Tstg	-55 to 150	^{o}C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions (Voltage reference to VSS=0V)
(VDD=3.135V to 3.465V, Ta=0 70C)

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Unit*
Supply Voltage	VDD	3.135	3.3	3.465	V
Output Supply Voltage	VDDQ	2.375	3.3	3.465	V
Input High Voltage	VIH	1.7	---	VDD+0.3	V
Input Low Voltage	VIL	-0.3	---	0.8	V

Note: Input overshoot voltage should be less than VDD+2V and not exceed 5ns.
Input undershoot voltage should be higher than -2V and not exceed 5ns.

Capacitance (Ta=25C, f=1MHz)

Parameter	*Symbol*	*Test conditions*	*Typ.*	*Max.*	*Unit*
Input Capacitance	CIN	VIN=0V	4	5	pF
Output Capacitance	COUT	VOUT=0V	6	7	pF

Note: These parameters are sampled and are not 100% tested.

DC Characteristics (Voltage reference to VSS=0V)

(VDD=3.135V to 3.465V, Ta=0 to 70C)
(T_A= -40 to +85C for Industrial Temperature Offering)

Parameter	*Symbol*	*Test Conditions*	133MHz		-4		-5		-6	
			Min	Max	Min	Max	Min	Max	Min	Max
Input Leakage Current (except ZZ, $\overline{FT}$, $\overline{LBO}$ pins)	I_{IL}	V_{IN} = 0 to V_{DD}	-1uA	1uA	-1uA	1uA	-1uA	1uA	-1uA	1uA
ZZ Input Current	IIN_{ZZ}	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0V \leq V_{IN} \leq V_{IH}$	-1uA -1uA	1uA 300uA	-1uA -1uA	1uA 300uA	-1uA -1uA	1uA 300uA	-1uA -1uA	1uA 300uA
Mode Input Current ($\overline{FT}$ & $\overline{LBO}$ pins)	IIN_M	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0V \leq V_{IN} \leq V_{IH}$	-300uA -1uA	1uA 1uA	-300uA -1uA	1uA 1uA	-300uA -1uA	1uA 1uA	-300uA -1uA	1uA 1uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	-1uA	1uA	-1uA	1uA	-1uA	1uA	-1uA	1uA
Output High Voltage	V_{OH}	I_{OH} = - 8mA	2.4V		2.4		2.4V		2.4V	
Output Low Voltage	V_{OL}	I_{OL} = + 8mA		0.4V		0.4V		0.4V		0.4V

Parameter	*Symbol*	*Test Conditions*	133MHz		-4		-5		-6	
			0 to 70C	-40 to +85C	0 to 70C	-40 to +85C	0 to 70C	-40 to +85C	0 to 70C	-40 to +85C
Operating Supply Current (V_{DD} = man, E = V_{IH})	I_{DD}	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	240mA	245mA	210mA	215mA	180mA	185mA	150mA	155mA
Standby Current	I_{SB}	ZZ $\geq V_{DD}$ - 0.2V	2mA	7mA	2mA	7mA	2mA	7mA	2mA	7mA
Deselect Supply Current	I_{DD}	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$	80mA	85mA	70mA	75mA	60mA	65mA	50mA	55mA

AC Test Conditions

(VDD=3.135V to 3.465V, Ta=0 to 70C)

Parameter	*Conditions*
Input high level	VIH=2.4V
Input low level	VIL=0.4V
Input rise time	tr=1V/ns
Input fall time	tf=1V/ns
Input reference level	1.4V
Output reference level	1.4V
Output load	Fig. 1& 2

Note: 1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted
3. Output load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}.

Output load 1

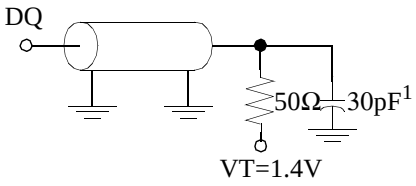


Fig. 1

Output load 2

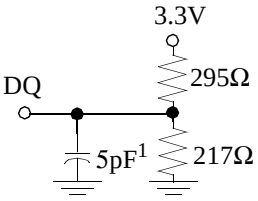


Fig. 2

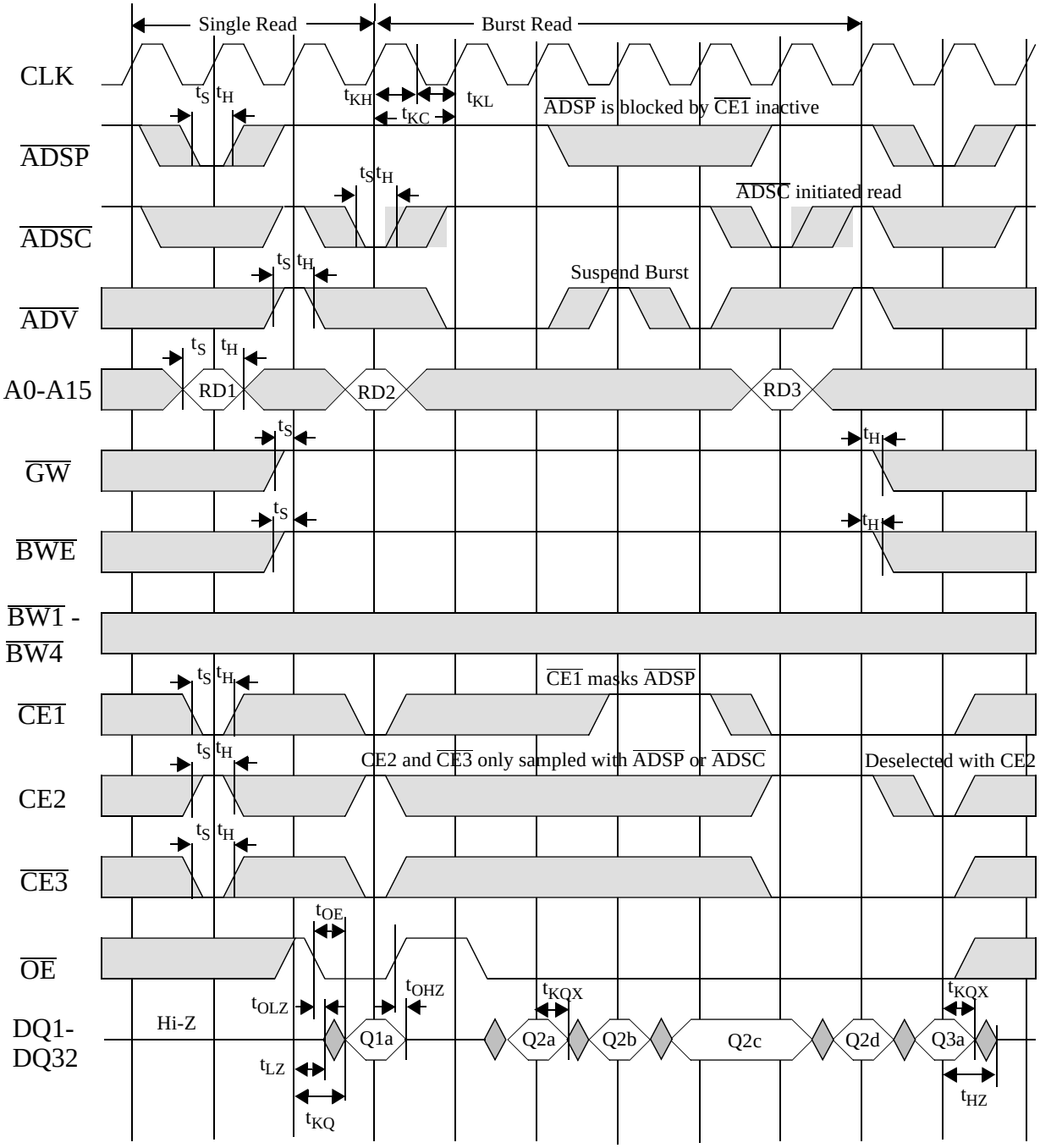
AC Electrical Characteristics

(VDD=3.135V to 3.465V, Ta=0 to 70°C)

	Parameter	*Symbol*	-4		-5		-6		Unit
			Min	Max	Min	Max	Min	Max	
Pipeline	Clock to output valid	t_{KQ}	---	4.5	---	5	---	6	ns
	Clock to output invalid	t_{KQX}	2	---	2	---	2	---	ns
	Clock to output in Low-Z	t_{LZ}[2]	2	---	2	---	2	---	ns
	Clock cycle time	t_{KC}	8.5	---	10	---	12.5	---	ns
Flow-Thru	Clock to output valid	t_{KQ}	---	12	NA[1]				ns
	Clock to output invalid	t_{KQX}	3	---					ns
	Clock to output in Low-Z	t_{LZ}[2]	3	---					ns
	Clock cycle time	t_{KC}	15	---					ns
	Clock high time	t_{KH}	2	---	3	---	4	---	ns
	Clock low time	t_{KL}	2	---	3	---	4	---	ns
	Clock to output in Hi-Z	t_{HZ}[2]	---	4	---	5	---	6	ns
	$\overline{OE}$ to output valid	t_{OE}	---	4	---	5	---	6	ns
	$\overline{OE}$ to output in Low-Z	t_{OLZ}[2]	0	---	0	---	0	---	ns
	$\overline{OE}$ to output in Hi-Z	t_{OHZ}[2]	---	4	---	5	---	6	ns
	Setup time	t_S	2.0	---	2.5	---	2.5	---	ns
	Hold time	t_H	0.5	---	0.5	---	0.5	---	ns
	ZZ setup time	t_{ZZS}[3]	5	---	5	---	5	---	ns
	ZZ hold time	t_{ZZH}[3]	1	---	1	---	1	---	ns
	ZZ recovery	t_{ZZR}	20	---	20	---	20	---	ns

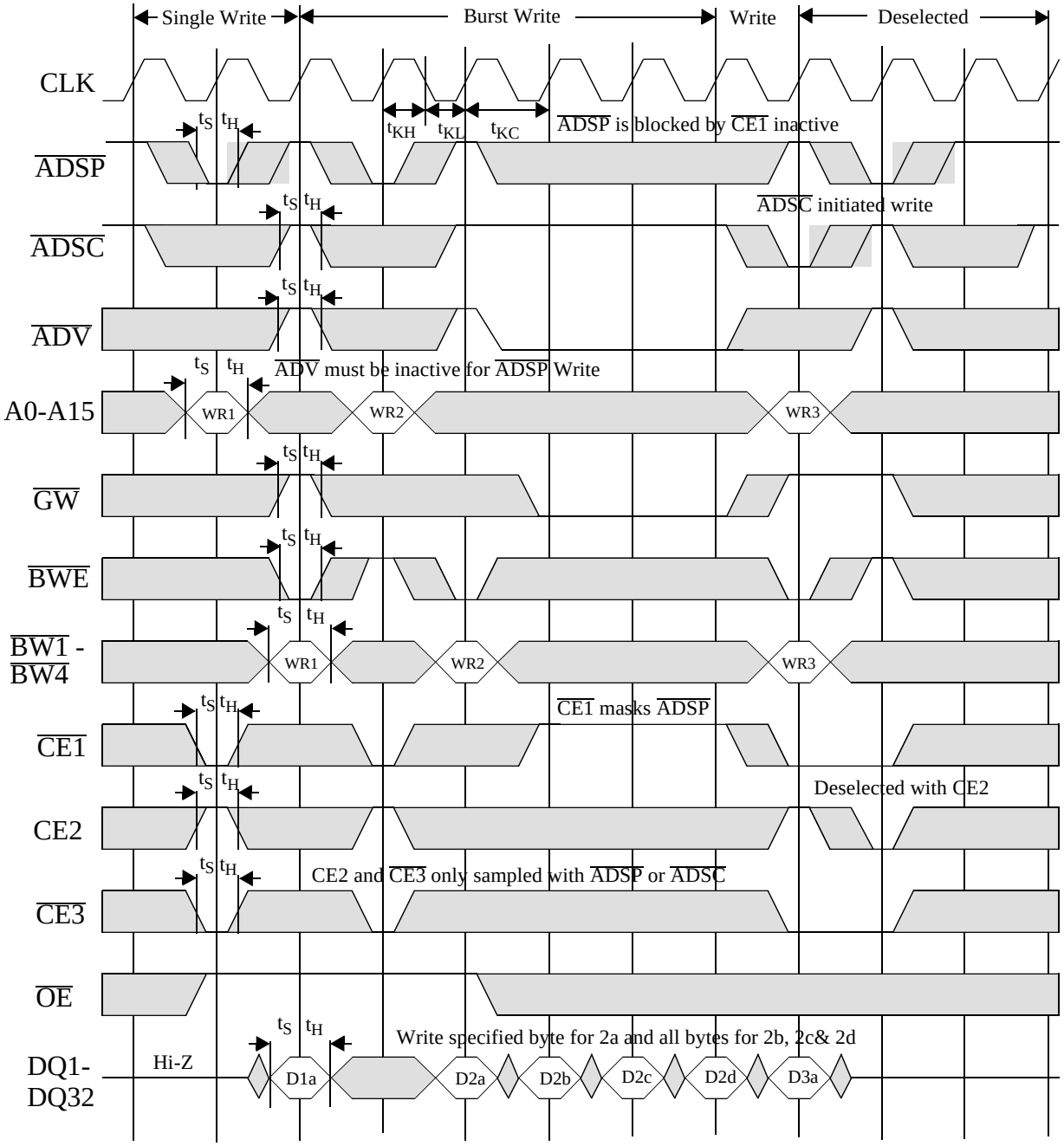
Note:
1. Flow-Thru mode is available in -4 bin only
2. These parameters are sampled and are not 100% tested
3. ZZ is a asynchronous signal. However, in order to be recognized on any given clock cycle, the signal must meet specified setup and hold time.

Read Cycle Timing (Pipeline)

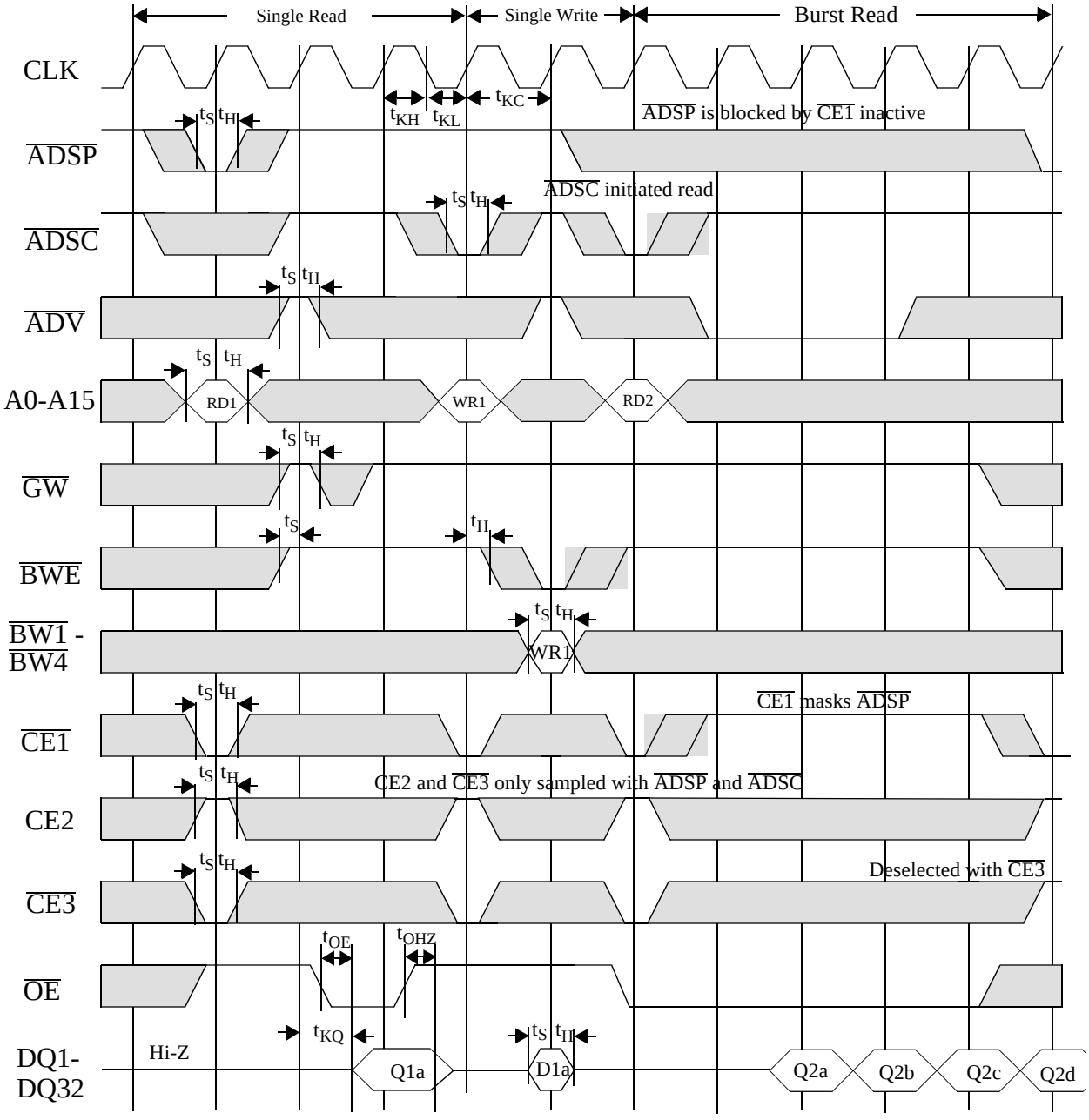


Write Cycle Timing

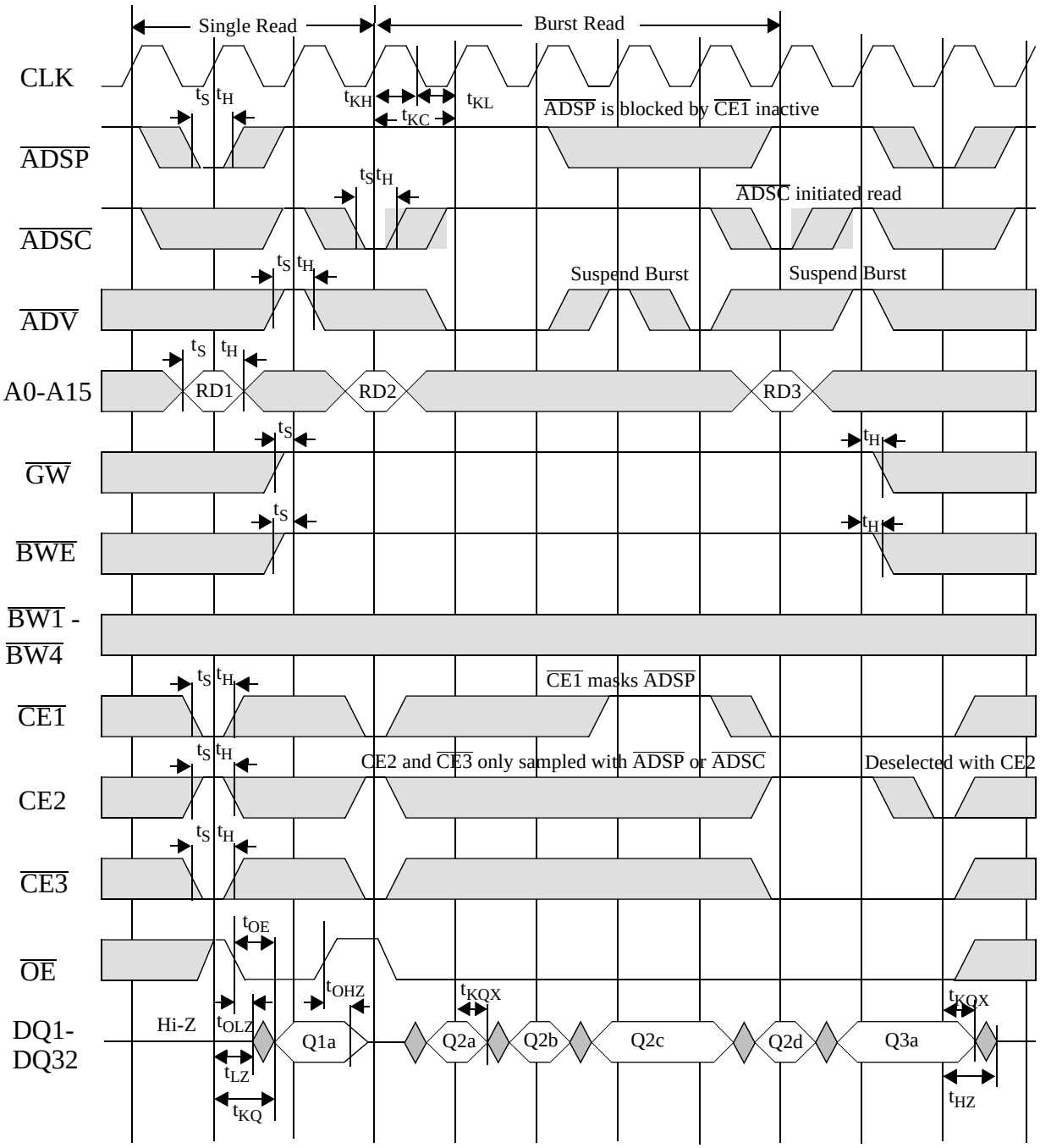
(This waveform can apply to both Pipeline and Flow-Thru modes)



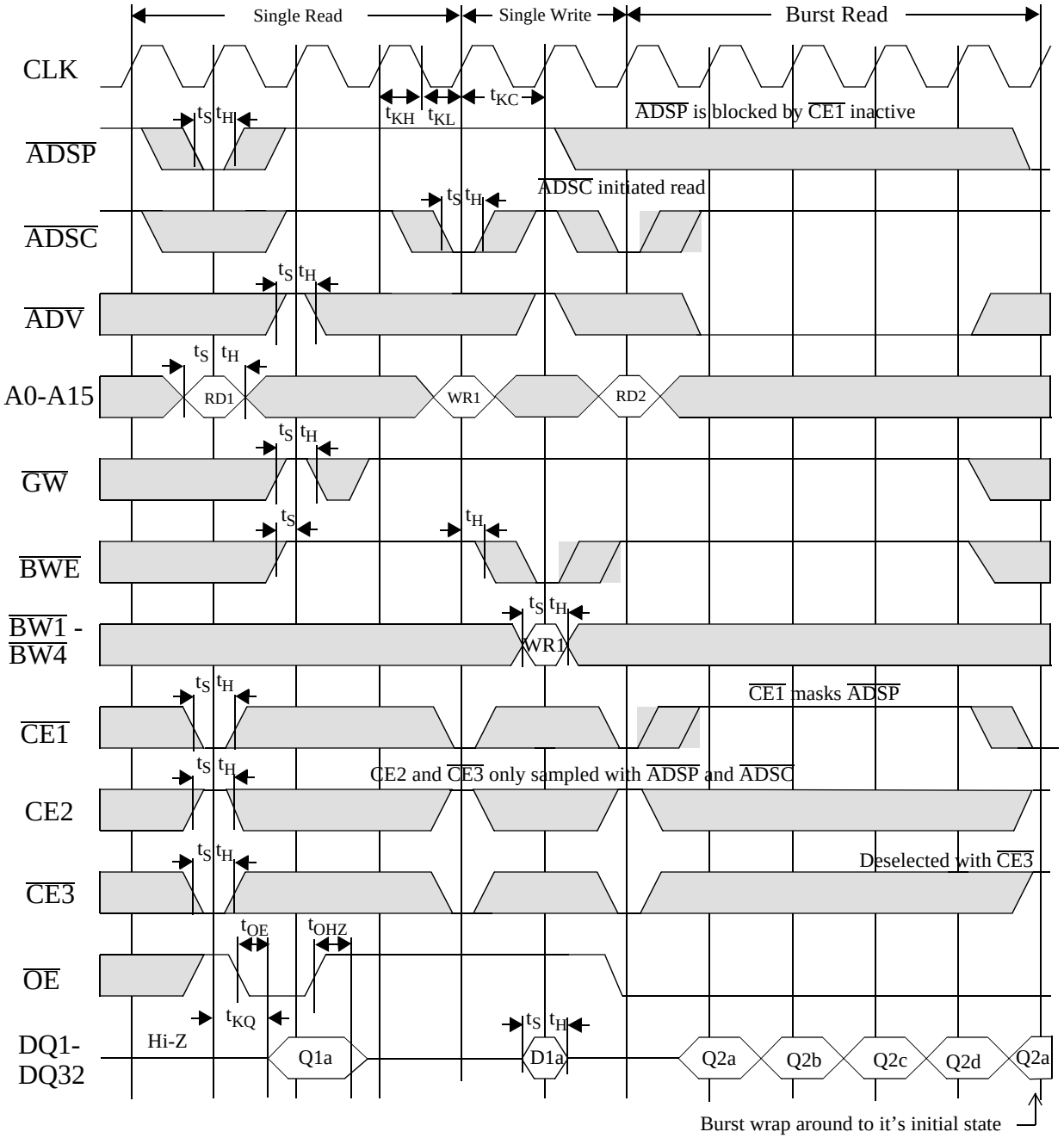
Read/Write Cycle Timing (Pipeline)



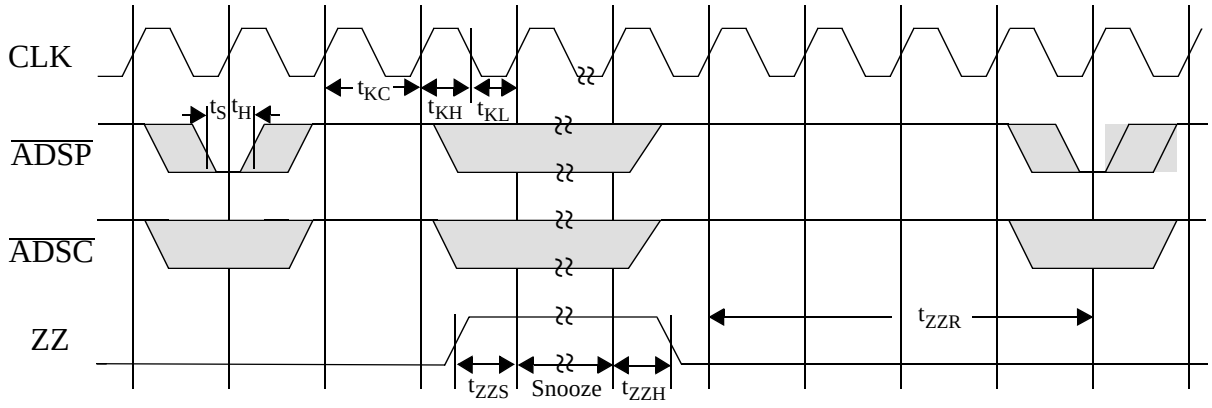
Read Cycle Timing (Flow-Thru)



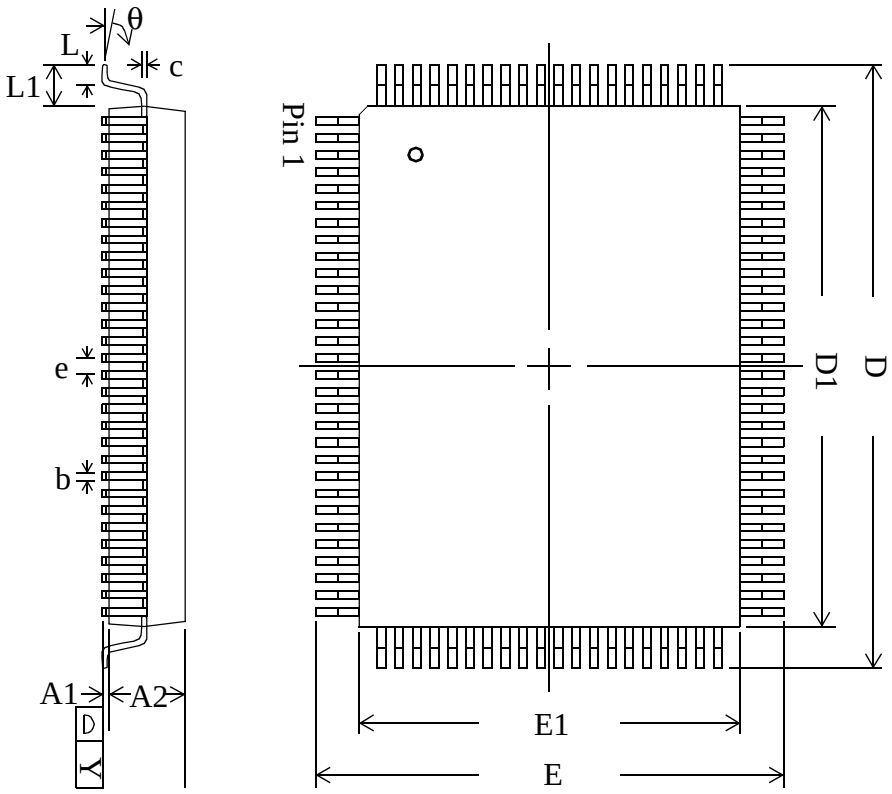
Read/Write Cycle Timing (Flow-Thru)



ZZ Timing



Package Dimension



		QFP (Q)			TQFP (T)		
Symbol	Description	Min.	Nom.	Max	Min.	Nom.	Max
A1	Stand Off	0.25	0.35	0.45	0.05	0.10	0.15
A2	Body Thickness	2.55	2.72	2.90	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40	0.20	0.30	0.40
c	Lead Thickness	0.10	0.15	0.20	0.09		0.20
D	Terminal Dimension	22.95	23.2	23.45	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1	19.9	20.0	20.1
E	Terminal Dimension	17.0	17.2	17.4	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1	13.9	14.0	14.1
e	Lead Pitch		0.65			0.65	
L	Foot Length	0.60	0.80	1.00	0.45	0.60	0.75
L1	Lead Length		1.60			1.00	
Y	Coplanarity			0.10			0.10
θ	Lead Angle	0^o		7^o	0^o		7^o

Note:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.