Integrated Device Technology, Inc.

# QUAD 2:1 MUX/DEMUX BUS SWITCH

**IDT74FST3257**
**PRELIMINARY**

## FEATURES:

- Bus switches provide zero delay paths
- Extended commercial range of –40°C to +85°C
- Low switch on-resistance:
  FST3xxx – 5Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015;
  > 200V using machine model (C = 200pF, R = 0)
- Available in QSOP and SOIC

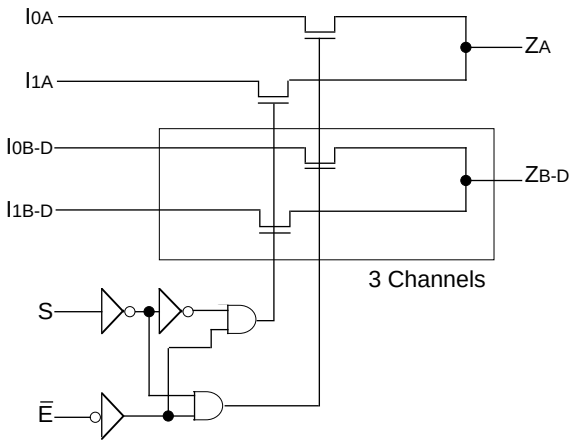
## DESCRIPTION:

The FST3257 belongs to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts or the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no $V_{CC}$ applied, the device has hot insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

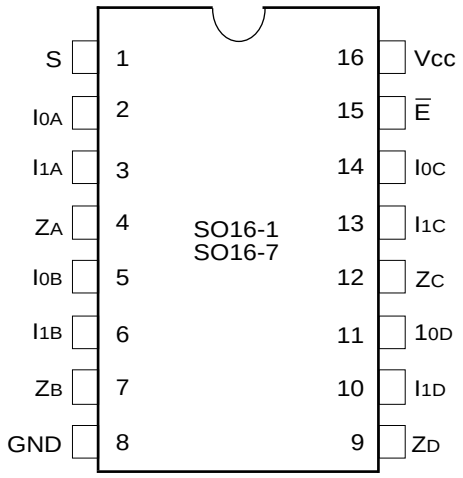
The FST3257 provides a 4-bit 2:1 multiplexer/demultiplexer. The S pin controls the mux select and the $\overline{E}$ pin serves as the switch enable.

## FUNCTIONAL BLOCK DIAGRAM




3257 drw 01

## PIN CONFIGURATION




**SOIC/QSOP**
**TOP VIEW**

3257 drw 02

## PIN DESCRIPTION

| Pin Names | I/O | Description |
|---|---|---|
| $I_{0A}$-$I_{0D}$ | I/O | Port 0 |
| $I_{1A}$-$I_{1D}$ | I/O | Port 1 |
| $\overline{E}$ | I | Switch Enable (Active Low) |
| S | I | Mux Select |
| $Z_A$-$Z_B$ | I/O | Port Z |

3257 tbl 01

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Description | Max. | Unit |
|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | –0.5 to +7.0 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $I_{OUT}$ | Maximum Continuous Channel Current | 128 | mA |

3257 tbl 02

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condiitions for extended periods may affect reliability.
2. $V_{CC}$, Control and Switch terminals.

## FUNCTION TABLE(1)

| $\overline{E}$ | S | $I_{0A-D}$ | $I_{1A-D}$ | $Z_{A-D}$ |
|---|---|---|---|---|
| H | X | X | X | Z |
| L | H | X | L | L |
| L | H | X | H | H |
| L | L | L | X | L |
| L | L | H | X | H |

3257 tbl 03

**NOTE:**
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

## CAPACITANCE(1)

| Symbol | Parameter | Conditions(2) | Typ. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Control Input Capacitance | | 4 | pF |
| $C_{I/O}$ | Switch Input/Output Capacitance | Switch Off | | pF |

3257 tbl 04

**NOTES:**
1. Capacitance is characterized but not tested
2. $T_A$ = 25°C, f = 1MHz, $V_{IN}$ = 0V, $V_{OUT}$ = 0V

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: $T_A$ = –40°C to +85°C, $V_{CC}$ = 5.0V ±5%

| Symbol | Parameter | Test Conditions(1) | | Min. | Typ.(2) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Logic HIGH for Control Inputs | | 2.0 | — | — | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Logic LOW for Control Inputs | | — | — | 0.8 | V |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max. | $V_I$ = $V_{CC}$ | — | — | ±1 | µA |
| $I_{IL}$ | Input LOW Voltage | | $V_I$ = GND | — | — | ±1 | |
| $I_{OZH}$ | High Impedance Output Current | $V_{CC}$ = Max. | $V_O$ = $V_{CC}$ | — | — | ±1 | µA |
| $I_{OZL}$ | (3-State Output pins) | | $V_O$ = GND | — | — | ±1 | |
| $I_{OS}$ | Short Circuit Current | $V_{CC}$ = Max., $V_O$ = GND(3) | | — | 300 | — | mA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = Min., $I_{IN}$ = –18mA | | — | –0.7 | –1.2 | V |
| $R_{ON}$ | Switch On Resistance(4) | $V_{CC}$ = Min., $V_{IN}$ = 0.0V, $I_{ON}$ = 30mA | | — | 5 | 7 | Ω |
| | | $V_{CC}$ = Min., $V_{IN}$ = 2.4V, $I_{ON}$ = 15mA | | — | 10 | 15 | Ω |
| $I_{OFF}$ | Input/Output Power Off Leakage | $V_{CC}$ = 0V, $V_{IN}$ or $V_O \leq$ 4.5V | | — | — | ±1 | µA |
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$ = Max., $V_I$ = GND or $V_{CC}$ | | — | 0.1 | 3 | µA |

3257 tbl 05

**NOTES:**
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Measured by voltage drop between ports at indicated current through the switch.

## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Quiescent Power Supply Current<br>TTL Inputs HIGH | $V_{CC}$ = Max.<br>$V_{IN}$ = 3.4V[3] | | — | 0.5 | 1.5 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[4] | $V_{CC}$ = Max.<br>Outputs Open<br>Enable Pin Toggling<br>50% Duty Cycle | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 30 | 40 | µA/ MHz/ Switch |
| $I_C$ | Total Power Supply Current[6] | $V_{CC}$ = Max.<br>Outputs Open<br>Enable Pin Toggling<br>(4 Switches Toggling)<br>fi = 10MHz<br>50% Duty Cycle | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 1.2 | 1.6 | mA |
| | | | $V_{IN}$ = 3.4<br>$V_{IN}$ = GND | — | 1.5 | 2.4 | |

**NOTES:**

3257 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Per TTL driven input ($V_{IN}$ = 3.4V). All other inputs at $V_{CC}$ or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the $I_{CC}$ formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i N)$
   $I_{CC}$ = Quiescent Current
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input ($V_{IN}$ = 3.4V)
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at $D_H$
   $I_{CCD}$ = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   $f_i$ = Input Frequency
   N = Number of Switches Toggling at $f_i$
   All currents are in milliamps and all frequencies are in megahertz.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: $T_A$ = –40°C to +85°C, $V_{CC}$ = 5.0V ±5%

| Symbol | Description | Condition[1] | Min.[2] | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{PLH}$<br>$t_{PHL}$ | Data Propagation Delay<br>I to Z, Z to I[3,4] | $C_L$ = 50pF<br>$R_L$ = 500Ω | — | — | 0.25 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Switch Multiplex Delay<br>S to I, Z | | 1.5 | — | 5.2 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Switch Turn on Delay<br>$\overline{E}$ to I, Z | | 1.5 | — | 4.8 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Switch Turn off Delay<br>$\overline{E}$ to I, Z[3] | | 1.5 | — | 5.0 | ns |
| $\lvert Q_{CI} \rvert$ | Charge Injection, Typical[5,6] | | — | 1.5 | — | pC |
| $\lvert Q_{CDI} \rvert$ | Charge Injection, Typical[6,7] | | — | 0.5 | — | pC |

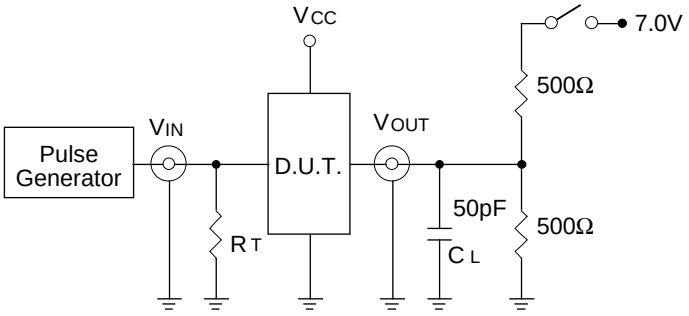
**NOTES:**

3257 tbl 07

1. See test circuit and waveforms.
2. Minimum limits guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.
4. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
5. Measured at switch turn off, load = 50 pF in parallel with 10 mΩ scope probe, $V_{IN}$ = 0.0 volts.
6. Measured at switch turn off through bus multiplexer, (e.g.- $I_0$ to Z = > $I_1$ to Z), load = 50 pF in parallel with 10 MΩ scope probe, $V_{IN}$ at A = 0.0 volts. Charge injection is reduced because the injection from the turn off of the $I_0$ to Z switch is compensated by the turn on of the $I_1$ to Z switch.
7. Characterized parameter. Not 100% tested.

# TEST CIRCUITS AND WAVEFORMS

## TEST CIRCUITS FOR ALL OUTPUTS




3257 lnk 03

## SWITCH POSITION

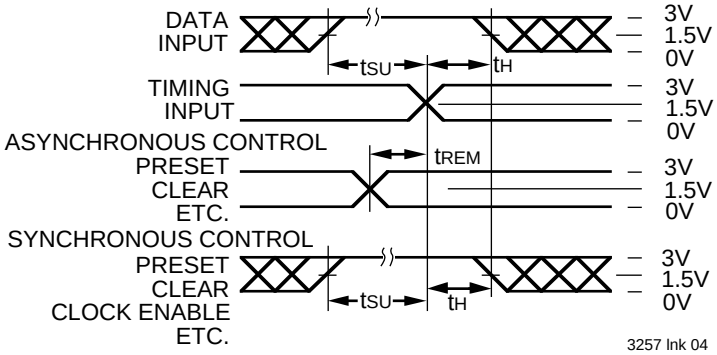
| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests | Open |

3257 lnk 08

**DEFINITIONS:**

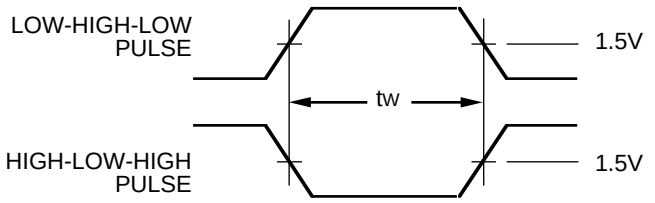
$C_L$= Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

## SET-UP, HOLD AND RELEASE TIMES



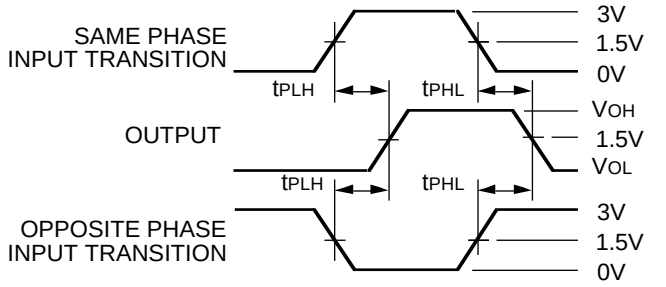

3257 lnk 04

## PULSE WIDTH



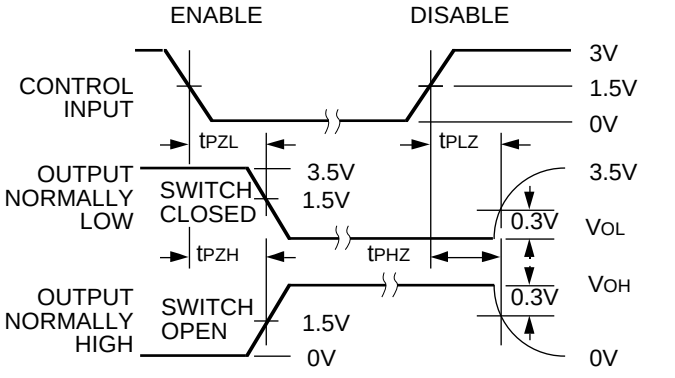

3257 lnk 03

## PROPAGATION DELAY




3257 lnk 06

## ENABLE AND DISABLE TIMES

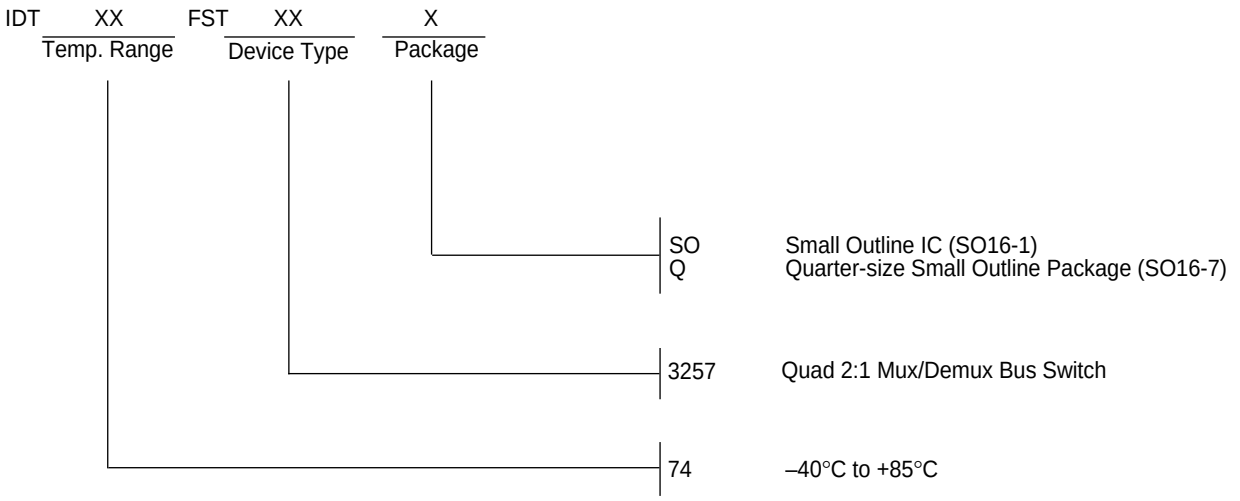



3257 lnk 07

**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns

## ORDERING INFORMATION




3257 drw 08