4.9-5.8 GHz High-Linearity Power Amplifier

SST11LP11

Preliminary Specifications

FEATURES:

- **Gain:**
  - ~24 dB gain across the 4.9-5.8 GHz band
- **High linear output power:**
  - ~25 dBm P1dB
  - EVM~4% at 18 dBm over 4.9-5.8 GHz for 64 QAM/54 Mbps operation
  - ACPR below IEEE 802.11a Mask up to 21 dBm across full band
- **Low idle current**
  - ~80 mA I_{CQ}
- **Low shut-down current (< 1 µA)**
- **20 dB dynamic range on-chip differential linear power detection**
- **Simple RF matching circuits**
- **Packages available**
  - 16-contact VQFN (3mm x 3mm)
  - Non-Pb (lead-free) packages available

APPLICATIONS:

- **WLAN (IEEE 802.11a)**
- **Japan WLAN**
- **HyperLAN2**
- **Multimedia**

PRODUCT DESCRIPTION

The SST11LP11 is a high-performance power amplifier IC based on the highly-reliable InGaP/GaAs HBT technology.

The SST11LP11 is designed to operate over the entire WLAN 802.11a band between 4.9-5.8 GHz frequency band for the U.S., European, and Japanese markets while achieving highly-linear power and low EVM.

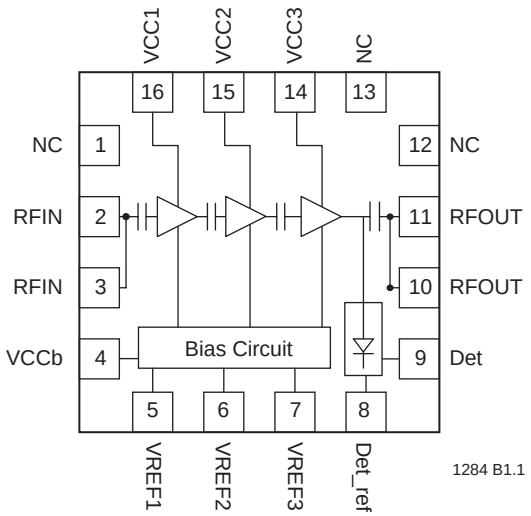
The SST11LP11 power amplifier IC features easy board-level usage along with on-chip linear power detection and power-down control. These features coupled with low current draw at maximum linear power make the SST11LP11 ideal for battery-powered 802.11a WLAN transmitter applications.

The SST11LP11 is offered in 16-contact VQFN package. See Figure 1 for pin assignments and Table 1 for pin descriptions.

Preliminary Specifications

FUNCTIONAL BLOCKS

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS

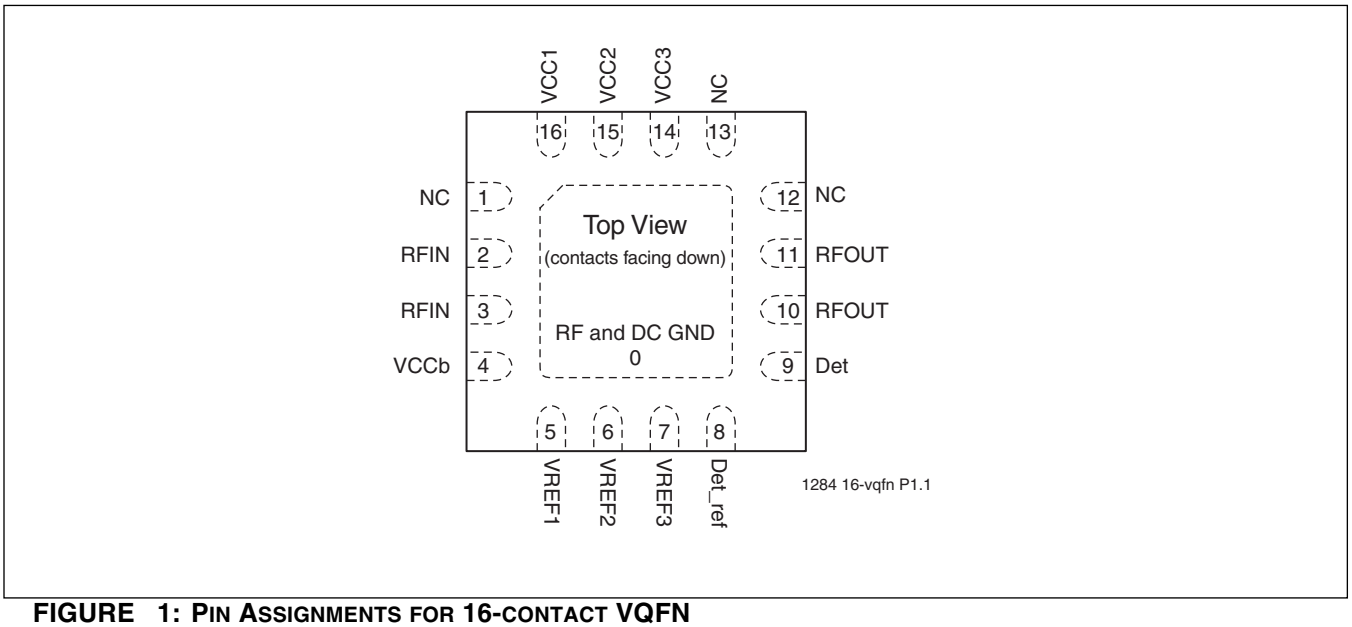


FIGURE 1: PIN ASSIGNMENTS FOR 16-CONTACT VQFN

PIN DESCRIPTIONS

TABLE 1: PIN DESCRIPTION

Symbol	Pin No.	Pin Name	Type[1]	Function
GND	0	Ground		The center pad should be connected to RF ground with several low inductance, low resistance vias.
NC	1	No Connection		Unconnected pins.
RFIN	2		I	RF input, DC decoupled
RFIN	3		I	RF input, DC decoupled
VCCb	4	Power Supply	PWR	Supply voltage for bias circuit
VREF1	5		PWR	1st stage idle current control
VREF2	6		PWR	2nd stage idle current control
VREF3	7		PWR	3rd stage idle current control
Det_ref	8		O	On-chip power detector reference
Det	9		O	On-chip power detector
RFOUT	10		O	RF output
RFOUT	11		O	RF output
NC	12	No Connection		Unconnected pins.
NC	13	No Connection		Unconnected pins.
VCC3	14	Power Supply	PWR	Power supply, 3rd stage
VCC2	15	Power Supply	PWR	Power supply, 2nd stage
VCC1	16	Power Supply	PWR	Power supply, 1st stage

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1. I=Input, O=Output

Preliminary Specifications

ELECTRICAL SPECIFICATIONS

The AC and DC specifications for the power amplifier interface signals. Refer to Table 2 for the DC voltage and current specifications. Refer to Figures 2 through 11 for the RF performance.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Supply Voltage to pins 4, 14, 15, 16 (V_{CC}) . . . . . -0.3V to +5.5V
DC supply current (I_{CC}) . . . . . 500 mA
Operating Temperature (T_A) . . . . . -40ºC to +85ºC
Storage Temperature (T_{STG}) . . . . . -40ºC to +120ºC
Maximum Junction Temperature (T_J) . . . . . +150ºC
Surface Mount Solder Reflow Temperature: . . . . . "with-Pb" units[1]: 240°C for 3 seconds
. . . . . "non-Pb" units: 260°C for 3 seconds

1. Certain "with-Pb" package types are capable of 260°C for 3 seconds; please consult the factory for the latest information.

OPERATING RANGE

Range	Ambient Temp	V_{CC}
Industrial	-40°C to +85°C	3.3V

TABLE 2: DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Typ	Max.	Unit	Test Conditions
V_{CC}	Supply Voltage at pins 4, 14, 15, 16	2.7	3.3	4.2	V	
I_{CC}	Supply Current @ P_{OUT}=21 dBm V_{CC}=3.3V			260	mA	802.11a modulation
Det	Power detector output voltage	0.6		2.2	V	-10 to +22 dBm
Det_ref	Power detector output reference		0.6		V	
I_{CQ}	Idle current		80		mA	
I_{OFF}	Shut down current			<1.0	µA	
VREG1,2,3	Reference Voltages for typical applications		2.90		V	

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TABLE 3: AC ELECTRICAL CHARACTERISTICS FOR CONFIGURATION

Symbol	Parameter	Min.	Typ	Max.	Unit
F_{L-U}	Frequency range	4.9		5.8	GHz
P_{OUT}	Output power @ P_{IN} = -6 dBm for OFDM signal		18		dBm
G	Small signal gain		24		dB
S	Power detector sensitivity		0.04		V/dB
G_{VAR1}	Gain variation over band (4900~5855 MHz)		1.75		dB
2f, 3f, 4f, 5f	Harmonics at 21 dBm		-40		dBc

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TYPICAL PERFORMANCE CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 3.3V, T_A = 25°C, VREG1,2,3 = 2.85V UNLESS OTHERWISE NOTED

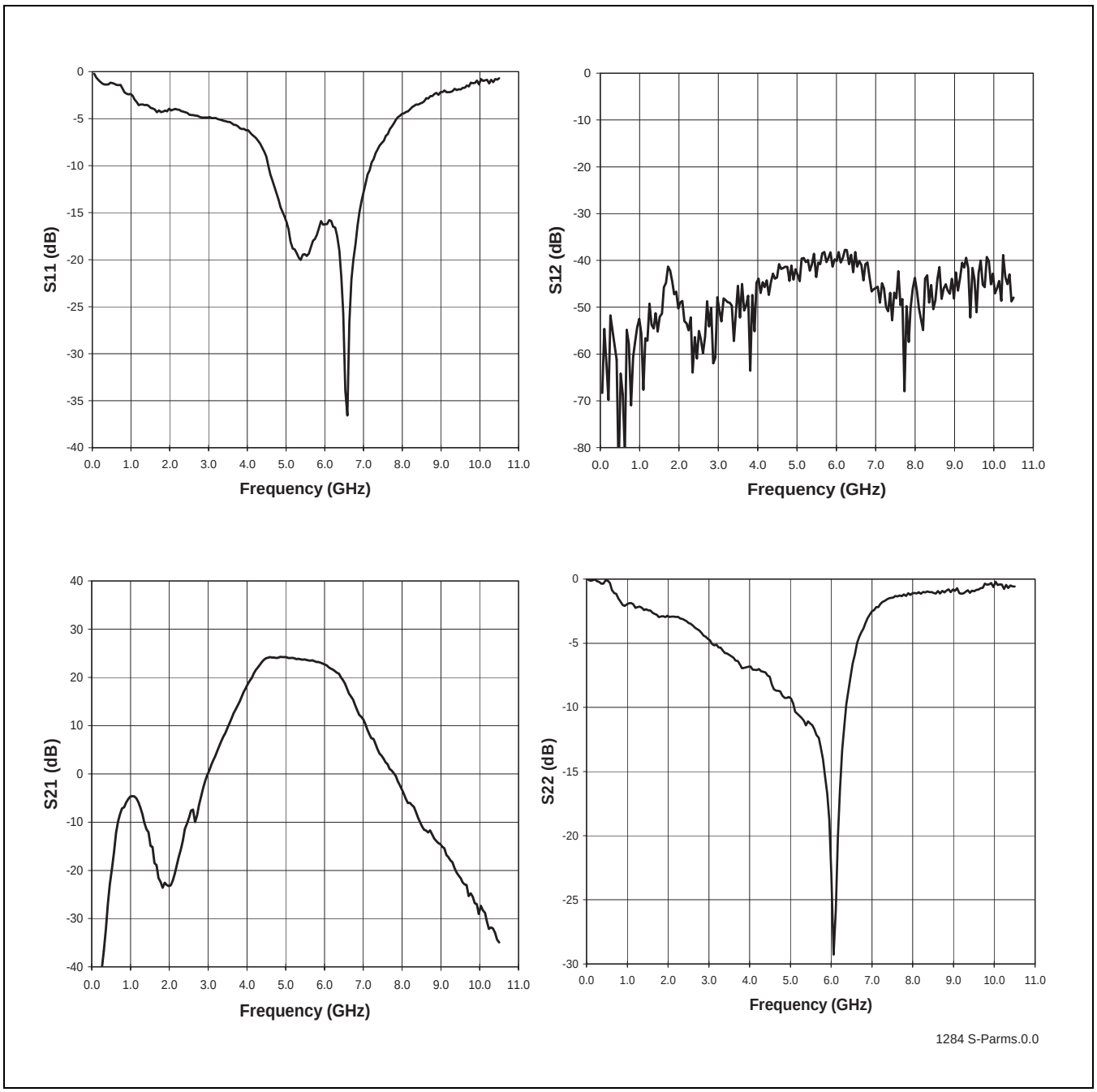


FIGURE 2: S-PARAMETERS

TWO-TONE MEASUREMENTS
TEST CONDITIONS: ΔF = 1 MHZ

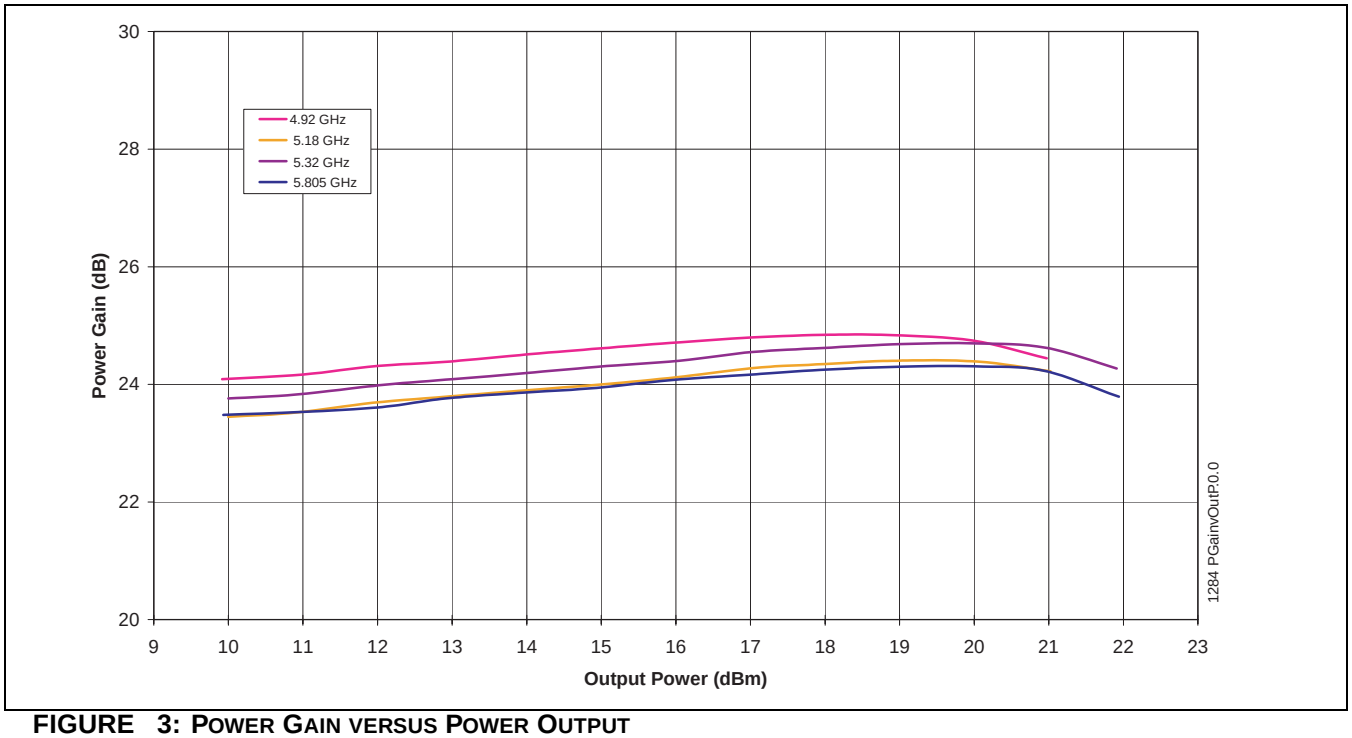


FIGURE 3: POWER GAIN VERSUS POWER OUTPUT

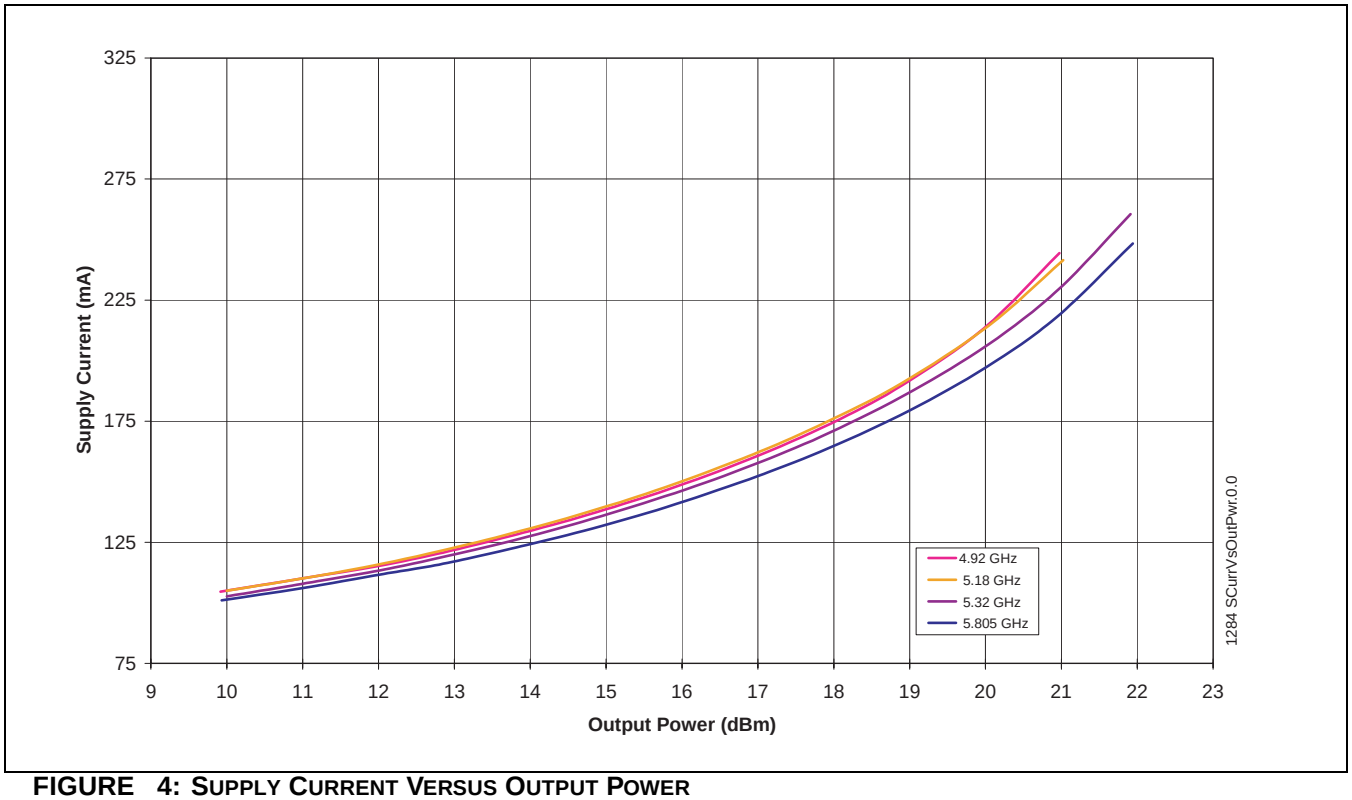


FIGURE 4: SUPPLY CURRENT VERSUS OUTPUT POWER

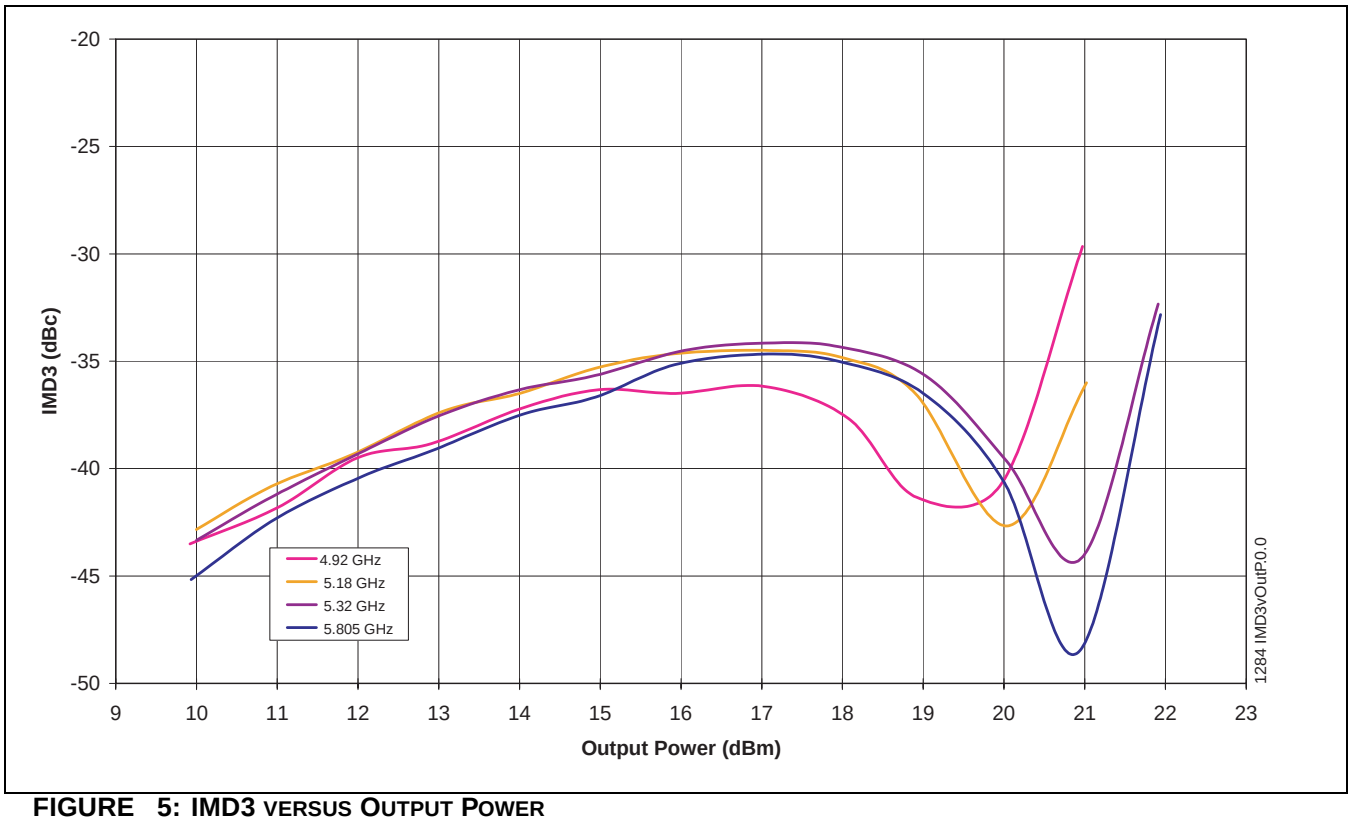


FIGURE 5: IMD3 VERSUS OUTPUT POWER

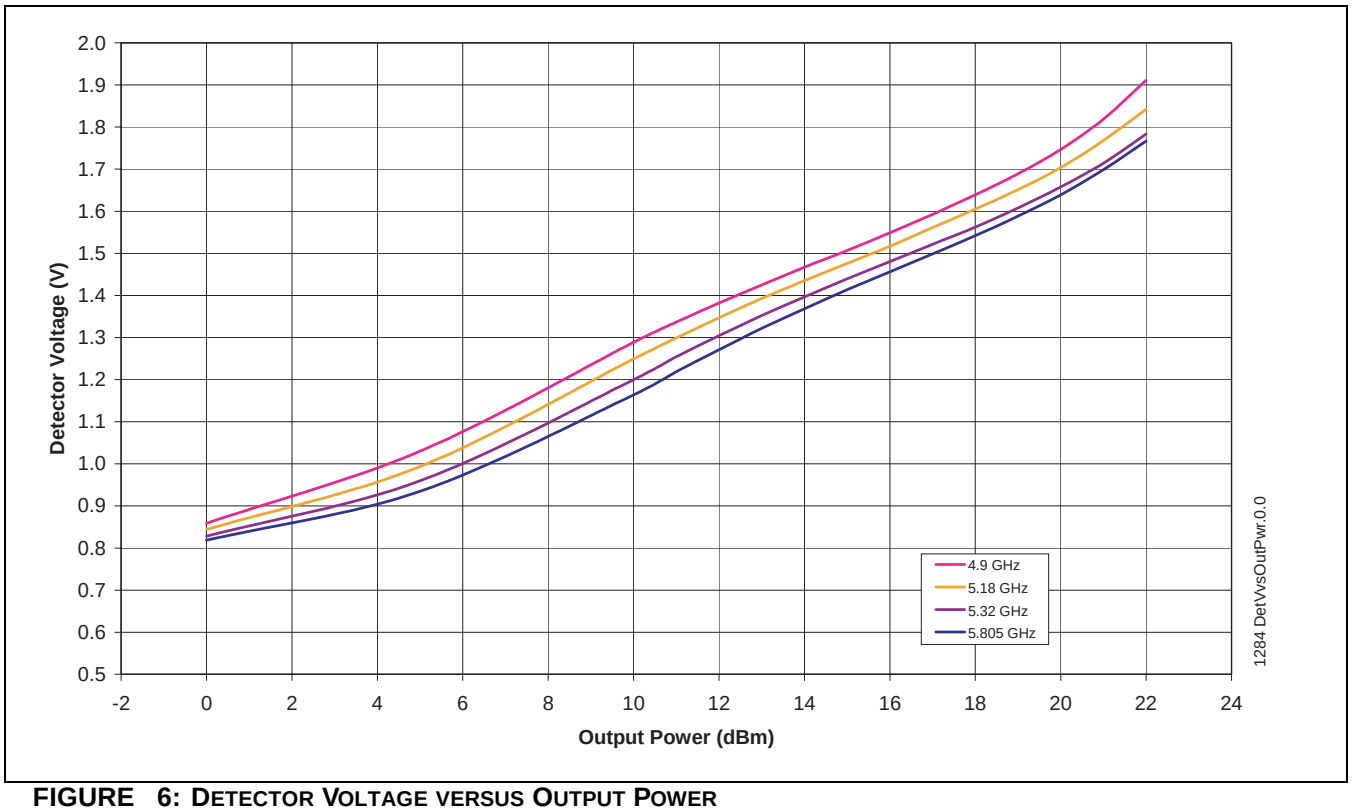


FIGURE 6: DETECTOR VOLTAGE VERSUS OUTPUT POWER

OFDM SIGNAL MEASUREMENTS

TEST CONDITIONS: 54 MBPS OFDM SIGNAL

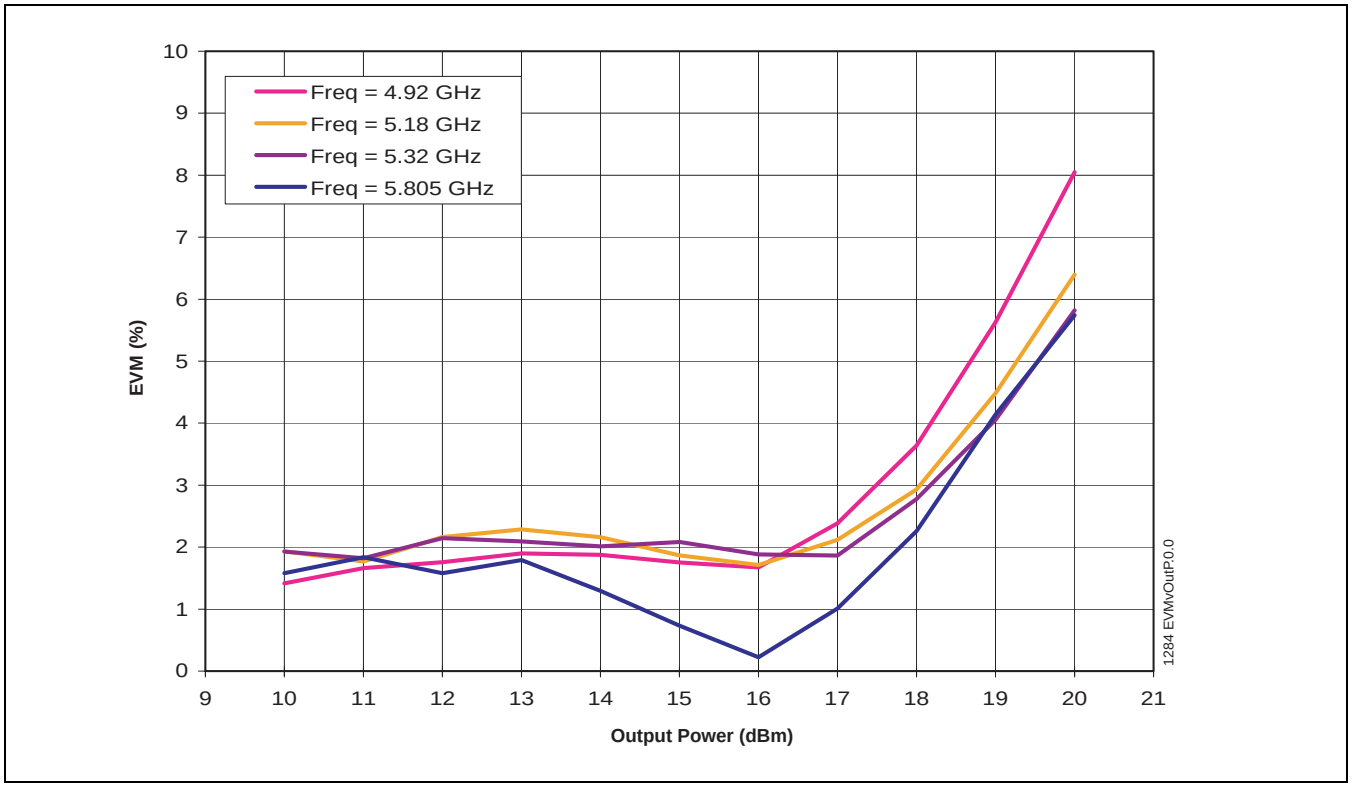


FIGURE 7: EVM VERSUS OUTPUT POWER

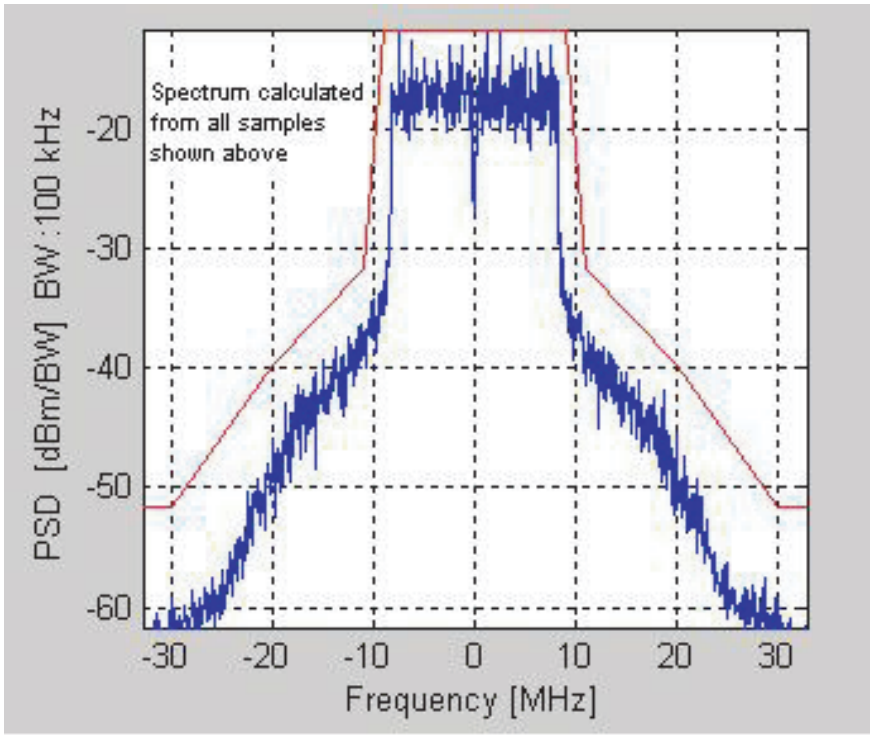


FIGURE 8: SPECTRUM MASK @ POUT = 21 DBM WITH FREQUENCY = 4.92 GHZ AND ICC = 235 MA

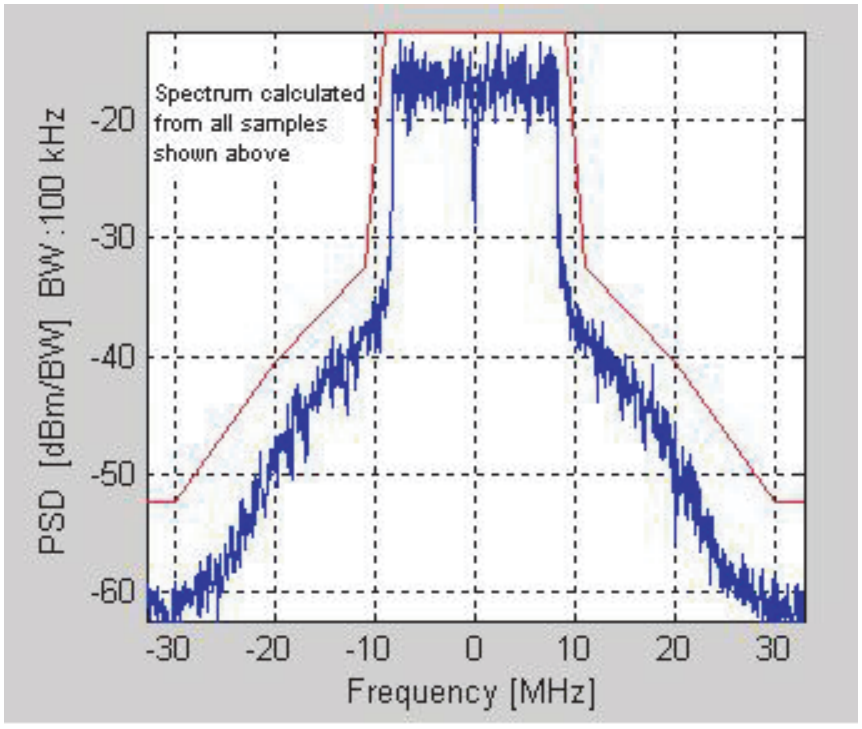


FIGURE 9: SPECTRUM MASK @ POUT = 21 DBM WITH FREQUENCY = 5.18 GHZ AND ICC = 230 MA

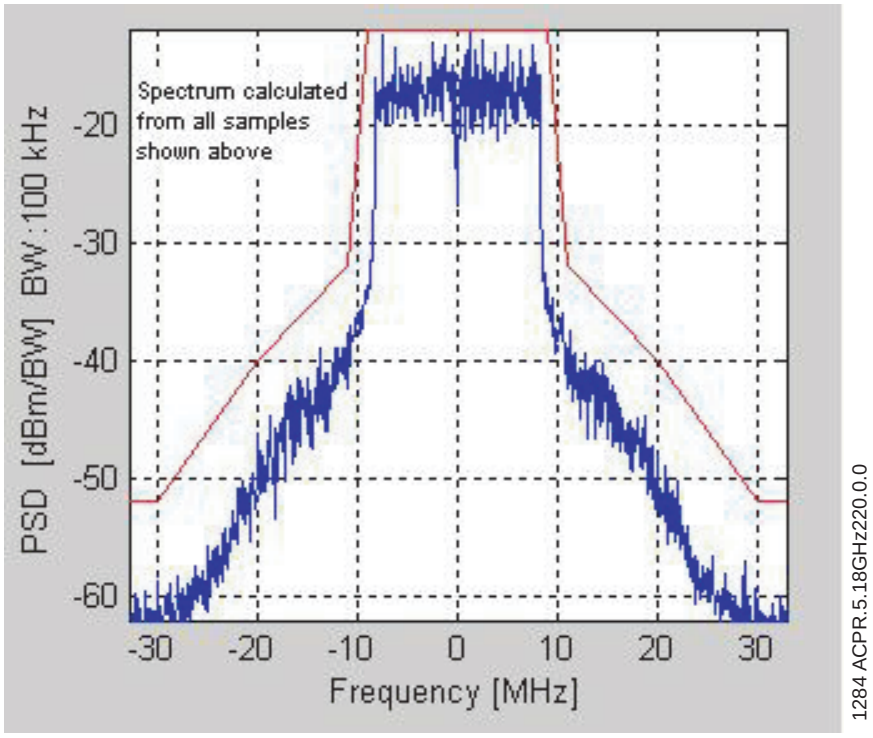


FIGURE 10: SPECTRUM MASK @ POUT = 21 DBM WITH FREQUENCY = 5.32 GHZ AND ICC = 220 MA

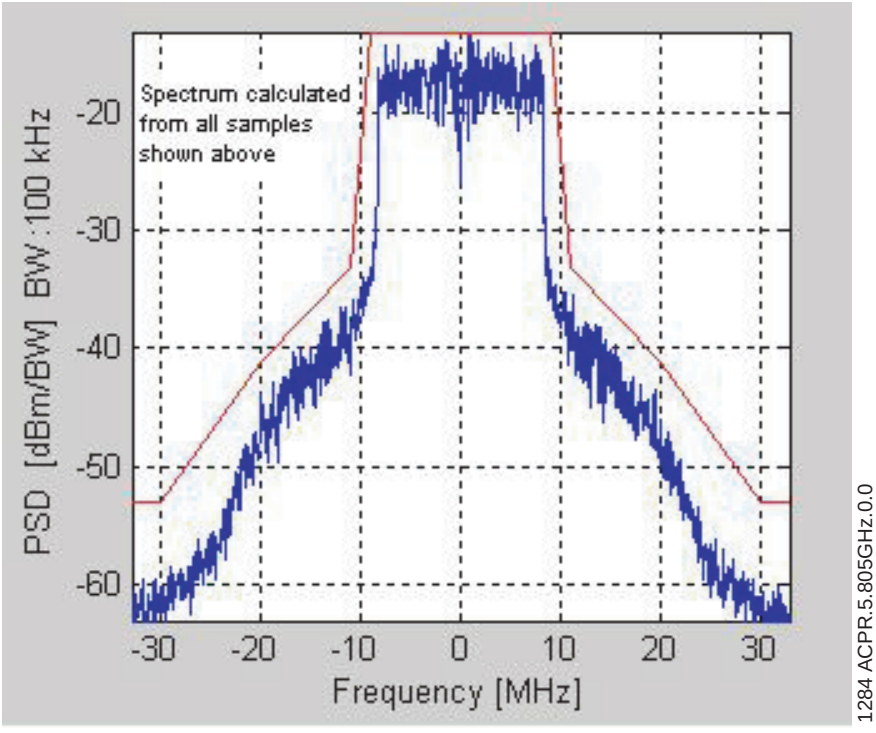


FIGURE 11: SPECTRUM MASK @ POUT = 21 DBM WITH FREQUENCY = 5.805 GHZ AND ICC = 215 MA

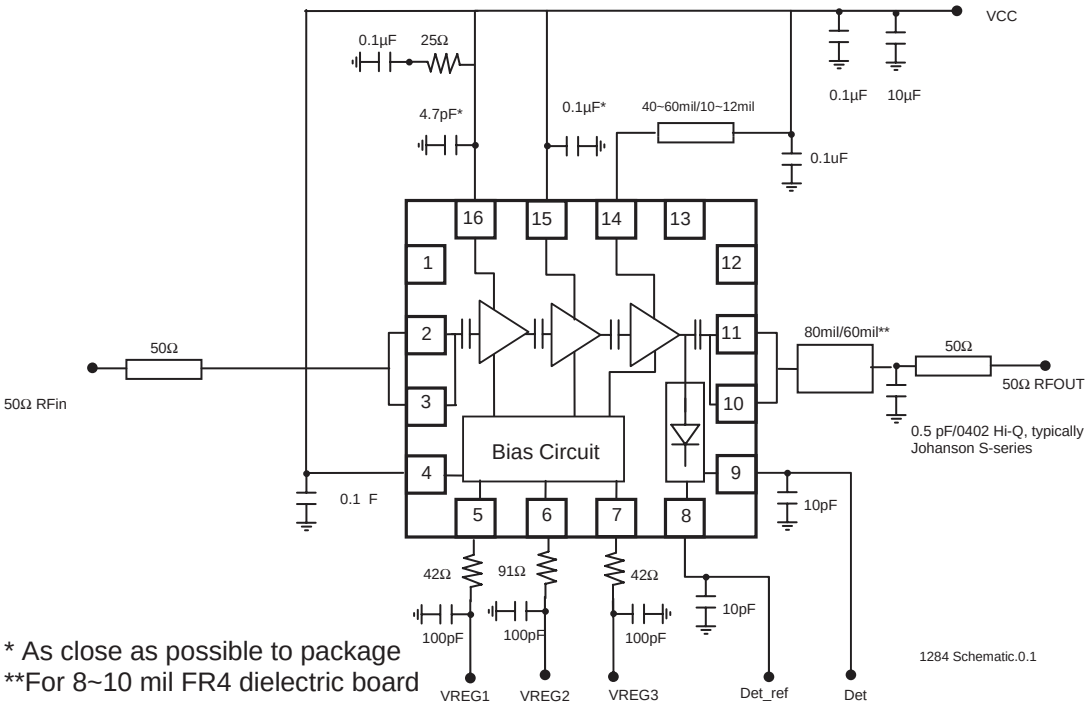
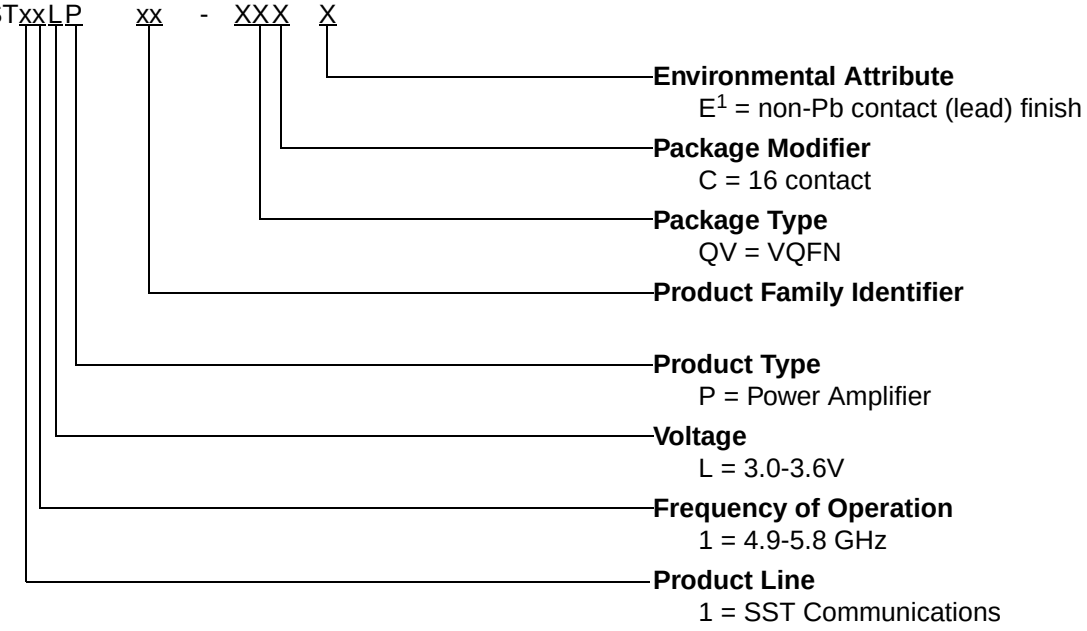


FIGURE 12: TYPICAL SCHEMATIC FOR HIGH-POWER, HIGH-EFFICIENCY 802.11A APPLICATIONS

Preliminary Specifications

PRODUCT ORDERING INFORMATION

SST11LP 11 - QVC E
SSTxxLP xx - XXX X



1. Environmental suffix “E” denotes non-Pb solder.
SST non-Pb solder devices are “RoHS Compliant”.

Valid combinations for SST11LP11

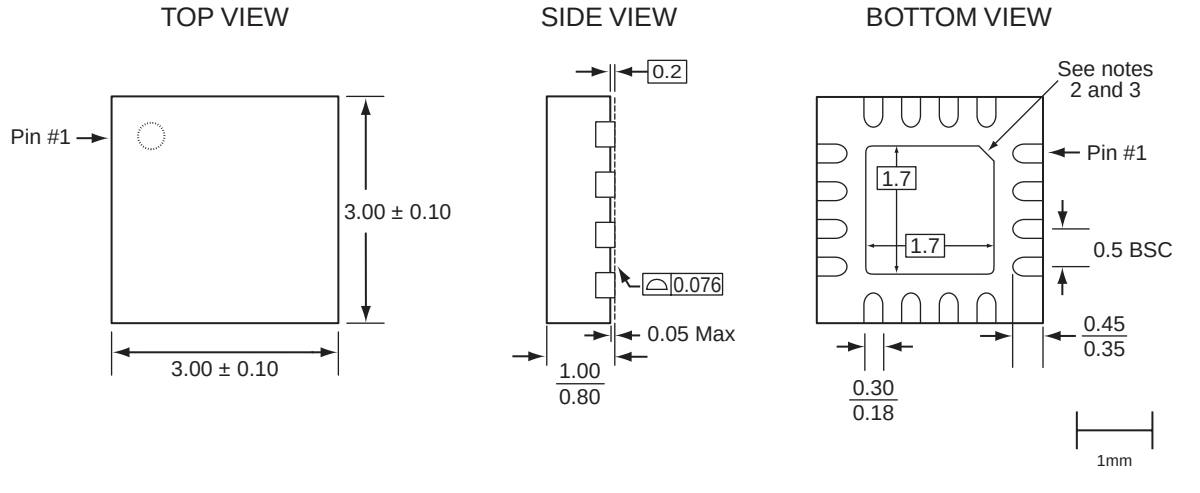
SST11LP11-QVC
SST11LP11-QVCE

SST11LP11 Evaluation Kits

SST11LP11-QVC-K
SST11LP11-QVCE-K

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC JEP95 MO-220I, variant VEED except external paddle nominal dimensions.
2. From the bottom view, the pin #1 indicator may be either a 45-degree chamfer or a half-circle notch.
3. The external paddle is electrically connected to the die back-side and possibly to certain V_{SS} leads. This paddle can be soldered to the PC board; it is suggested to connect this paddle to the V_{SS} of the unit. Connection of this paddle to any other voltage potential can result in shorts and/or electrical malfunction of the device.
4. Untoleranced dimensions are nominal target dimensions.
5. All linear dimensions are in millimeters (max/min).

16-CONTACT VERY-THIN QUAD FLAT NO-LEAD (VQFN)
SST PACKAGE CODE: QVC

TABLE 4: REVISION HISTORY

Revision	Description	Date
00	• S71284: SST conversion of data sheet GP1111	Jan 2005

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