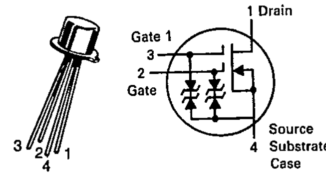
3N201
3N202
3N203

CASE 20-03, STYLE 9
TO-72 (TO-206AF)



DUAL-GATE MOSFET
VHF AMPLIFIER

N-CHANNEL — DEPLETION

Refer to MPF201 for additional graphs.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG1} V_{DG2}	30 30	Vdc
Drain Current	I_D	50	mAdc
Gate Current	I_{G1} I_{G2}	±10 ±10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	360 2.4	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.2 8.0	Watt mW/°C
Lead Temperature	T_L	300	°C
Junction Temperature Range	T_J	−65 to +175	°C
Storage Channel Temperature Range	T_{stg}	−65 to +175	°C

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (I_D = 10 μAdc, V_S = 0, V_{G1S} = V_{G2S} = −5.0 Vdc)	$V_{(BR)DSX}$	25	—	—	Vdc
Gate 1-Source Breakdown Voltage(1) (I_{G1} = ±10 mAdc, V_{G2S} = V_{DS} = 0)	$V_{(BR)G1SO}$	±6.0	±12	±30	Vdc
Gate 2-Source Breakdown Voltage(1) (I_{G2} = ±10 mAdc, V_{G1S} = V_{DS} = 0)	$V_{(BR)G2SO}$	±6.0	±12	±30	Vdc
Gate 1 Leakage Current (V_{G1S} = ±5.0 Vdc, V_{G2S} = V_{DS} = 0) (V_{G1S} = −5.0 Vdc, V_{G2S} = V_{DS} = 0, T_A = 150°C)	I_{G1SS}	— —	±.040 —	±10 −10	nAdc μAdc
Gate 2 Leakage Current (V_{G2S} = ±5.0 Vdc, V_{G1S} = V_{DS} = 0) (V_{G2S} = −5.0 Vdc, V_{G1S} = V_{DS} = 0, T_A = 150°C)	I_{G2SS}	— —	±.050 —	±10 −10	nAdc μAdc
Gate 1 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 20 μAdc)	$V_{G1S(off)}$	−0.5	−1.5	−5.0	Vdc
Gate 2 to Source Cutoff Voltage (V_{DS} = 15 Vdc, V_{G1S} = 0, I_D = 20 μAdc)	$V_{G2S(off)}$	−0.2	−1.4	−5.0	Vdc
ON CHARACTERISTICS					
Zero-Gate-Voltage Drain Current(2) (V_{DS} = 15 Vdc, V_{G1S} = 0, V_{G2S} = 4.0 Vdc) 3N201,3N202 3N203	I_{DSS}	6.0 3.0	13 11	30 15	mAdc
SMALL-SIGNAL CHARACTERISTICS					
Forward Transfer Admittance(3) (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, V_{G1S} = 0, f = 1.0 kHz) 3N201,3N202 3N203	$\|Y_{fs}\|$	8.0 7.0	12.8 12.5	20 15	mmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, f = 1.0 MHz)	C_{iss}	—	3.3	—	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = 10 mAdc, f = 1.0 MHz)	C_{rss}	0.005	0.014	0.03	pF
Output Capacitance (V_{DS} = 15 Vdc, V_{G2S} = 4.0 Vdc, I_D = I_{DSS}, f = 1.0 MHz)	C_{oss}	—	1.7	—	pF
FUNCTIONAL CHARACTERISTICS					
Noise Figure (V_{DD} = 18 Vdc, V_{GG} = 7.0 Vdc, f = 200 MHz) (Figure 1) 3N201 (V_{DD} = 18 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 3) 3N203	NF	— —	1.8 5.3	4.5 6.0	dB

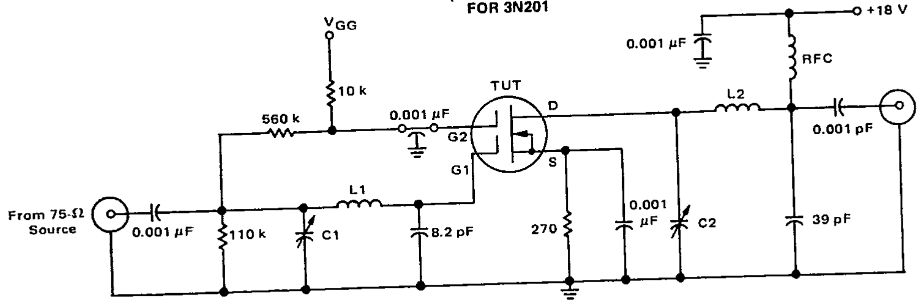
3N201, 3N202, 3N203

ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Common Source Power Gain		G_{ps}				dB
(V_{DD} = 18 Vdc, V_{GG} = 7.0 Vdc, f = 200 MHz) (Figure 1)	3N201		15	20	25	
(V_{DD} = 18 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 3)	3N203		20	25	30	
(V_{DD} = 18 Vdc, f_{LO} = 245 MHz, f_{RF} = 200 MHz) (Figure 2)	3N202	G_c(5)	15	19	25	
Bandwidth		BW				MHz
(V_{DD} = 18 Vdc, V_{GG} = 7.0 Vdc, f = 200 MHz) (Figure 1)	3N201		5.0	—	9.0	
(V_{DD} = 18 Vdc, f_{LO} = 245 MHz, f_{RF} = 200 MHz) (Figure 2)	3N202		4.5	—	7.5	
(V_{DD} = 18 Vdc, V_{GG} = 6.0 Vdc, f = 45 MHz) (Figure 3)	3N203		3.0	—	6.0	
Gain Control Gate-Supply Voltage(4)		$V_{GG(GC)}$				Vdc
(V_{DD} = 18 Vdc, ΔG_{ps} = −30 dB, f = 200 MHz) (Figure 1)	3N201		0	−1.0	−3.0	
(V_{DD} = 18 Vdc, ΔG_{ps} = −30 dB, f = 45 MHz) (Figure 3)	3N203		0	−0.6	−3.0	

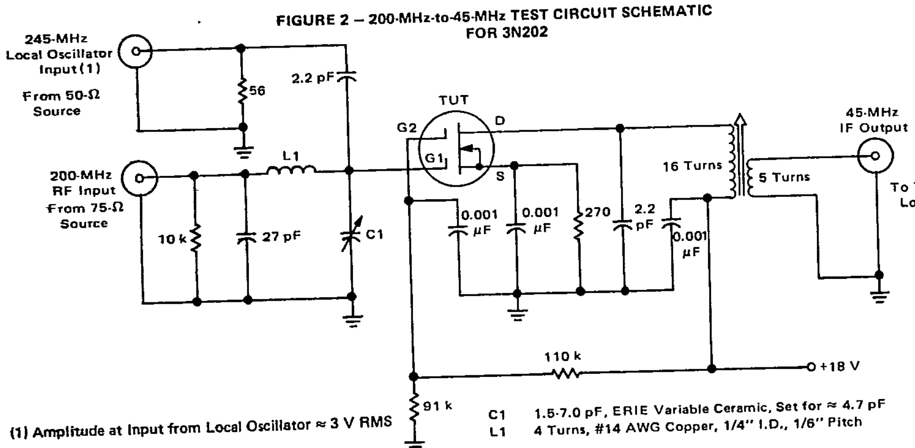
(1) All gate breakdown voltages are measured while the device is conducting rated gate current. This ensures that the gate-voltage limiting network is functioning properly.
(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.
(3) This parameter must be measured with bias voltages applied for less than 5 seconds to avoid overheating.
(4) ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 7.0 volts (3N201) and V_{GG} = 6.0 volts (3N203).
(5) Power Gain Conversion

FIGURE 1 — 200-MHz TEST CIRCUIT SCHEMATIC FOR 3N201



C1 4.0 30 pF, ERIE Variable Ceramic, Set for ≈ 22 pF
C2 4.0 30 pF, ERIE Variable Ceramic, Set for ≈ 10 pF
L1 4 Turns, #14 AWG Cooper, 1/4" I.D., 1/6" Pitch
L2 3 Turns, #14 AWG Cooper, 1/4" I.D., 1/8" Pitch
RFC DELEVAN No. 153712, 1.0 μH

FIGURE 2 — 200-MHz-to-45-MHz TEST CIRCUIT SCHEMATIC FOR 3N202



C1 1.5-7.0 pF, ERIE Variable Ceramic, Set for ≈ 4.7 pF
L1 4 Turns, #14 AWG Copper, 1/4" I.D., 1/6" Pitch

(1) Amplitude at Input from Local Oscillator ≈ 3 V RMS

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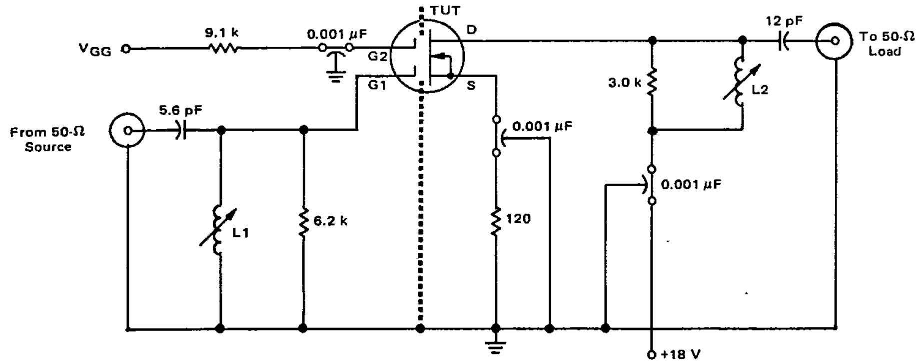
FIGURE 3 — 45-MHz TEST CIRCUIT SCHEMATIC
3N203



L1 14 Turns, #30 AWG Copper, Close-Wound 7/32" OD form with ARNOLD ENGINEERING "J" Tuning Core

L2 10 Turns, #30 AWG Copper, Close-Wound 7/32" OD form with ARNOLD ENGINEERING "J" Tuning Core

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TYPICAL CHARACTERISTICS

FIGURE 4 — DRAIN CURRENT versus DRAIN to SOURCE VOLTAGE

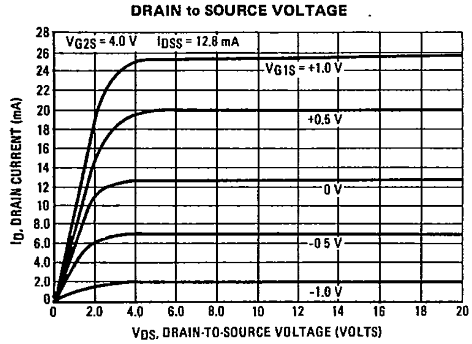

FIGURE 5 — DRAIN CURRENT versus GATE-ONE to SOURCE VOLTAGE

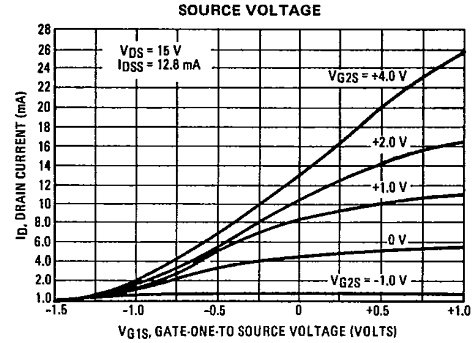

FIGURE 6 — SMALL-SIGNAL COMMON-SOURCE GATE-ONE FORWARD TRANSFER ADMITTANCE versus DRAIN CURRENT

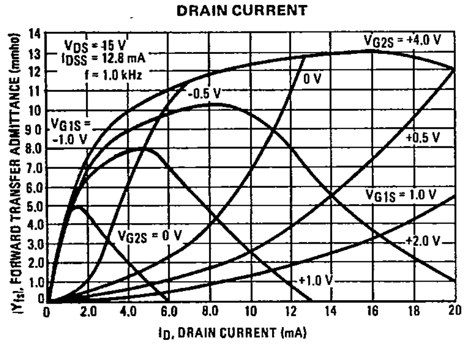

FIGURE 7 — SMALL-SIGNAL COMMON-SOURCE GATE-ONE FORWARD TRANSFER ADMITTANCE versus GATE-ONE to SOURCE VOLTAGE

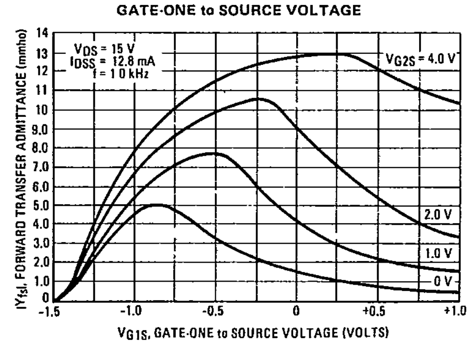

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FIGURE 8 – SMALL-SIGNAL COMMON-SOURCE GATE-ONE FORWARD TRANSFER ADMITTANCE versus GATE-TWO to SOURCE VOLTAGE

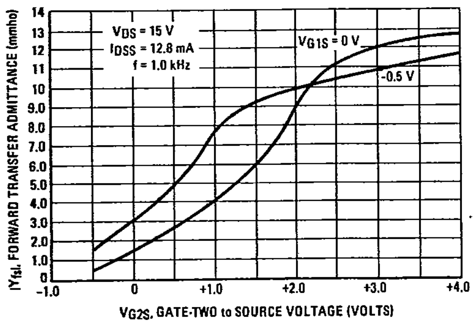
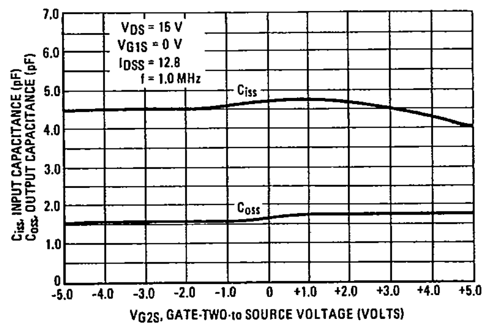


FIGURE 9 – SMALL-SIGNAL COMMON-SOURCE GATE-ONE INPUT AND OUTPUT CAPACITANCE versus GATE-TWO-to-SOURCE VOLTAGE



TYPICAL CHARACTERISTICS

FIGURE 10 – COMMON-SOURCE POWER GAIN AND SPOT NOISE FIGURE versus DRAIN CURRENT

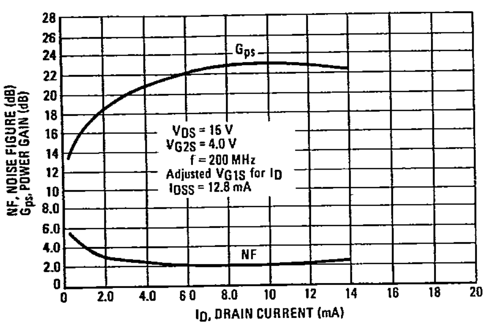


FIGURE 11 – COMMON-SOURCE POWER GAIN AND SPOT NOISE FIGURE versus GAIN CONTROL GATE-SUPPLY VOLTAGE – 3N201

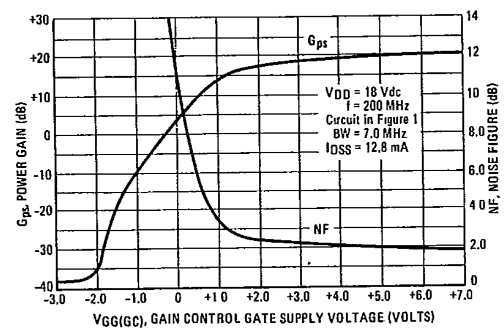


FIGURE 12 – COMMON-SOURCE POWER GAIN versus DRAIN SUPPLY CURRENT – 3N201

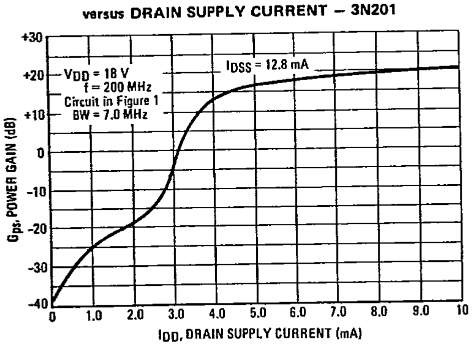


FIGURE 13 – SMALL-SIGNAL COMMON-SOURCE CONVERSION POWER GAIN versus LOCAL OSCILLATOR INPUT VOLTAGE – 3N202

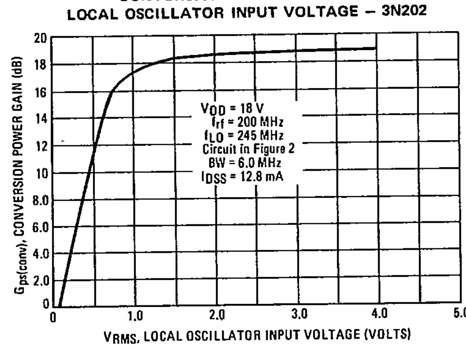


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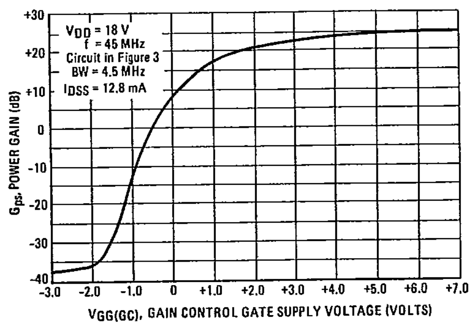
FIGURE 14 – SMALL-SIGNAL COMMON SOURCE INSERTION POWER GAIN versus GAIN CONTROL GATE-SUPPLY VOLTAGE – 3N203



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TYPICAL CHARACTERISTICS

FIGURE 15 – SMALL-SIGNAL GATE ONE FORWARD TRANSFER ADMITTANCE versus FREQUENCY

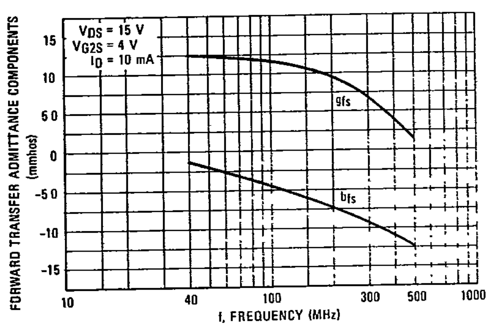

FIGURE 16 – SMALL-SIGNAL GATE ONE INPUT ADMITTANCE versus FREQUENCY

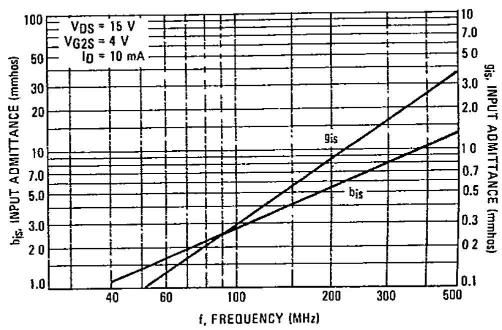

FIGURE 17 – SMALL-SIGNAL GATE ONE OUTPUT ADMITTANCE versus FREQUENCY