## 1.0 Description

AMI Semiconductor's AMIS-720442-A (PI3042A) contact image sensor (CIS) is a 400 dots per inch (dpi) linear array image sensor chip. The sensor chip is processed using a CMOS image sensing technology, belonging to AMIS. Designed for cascading multiple chips in a series, the image sensor chips, using chip-on-board process, are bonded end-to-end on a printed circuit board (PCB). This bonding process allows the manufacturers to produce variable CIS module lengths in increments of chip array lengths. This allows a wide variety of image reading widths which are easily applied to the numerous document scanners found in facsimile, as well as the narrow width scanners, such as, those found in check reader, lotto tickets, entrance gates tickets, etc. Included in this list of scanners are various types of automated office equipment which require a wide variety of scanning widths.

Figure 1 is a block diagram of the imaging sensor chip. Each sensor chip consists of 128 detector elements, their associated multiplexing switches, buffers and a chip selector. The detector's element-to-element spacing is approximately 62.5µm. The size of each chip without scribe lines is 8080µm by 385µm. Each sensor chip has seven bonding pads. The pad symbols and functions are described in Table 1.

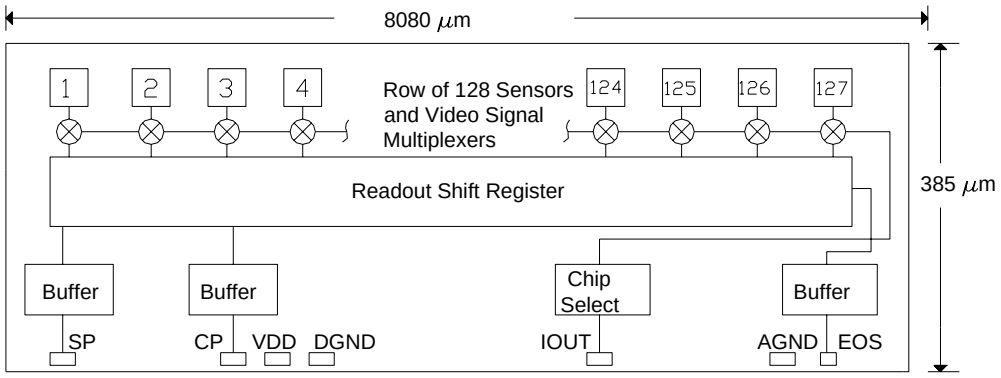


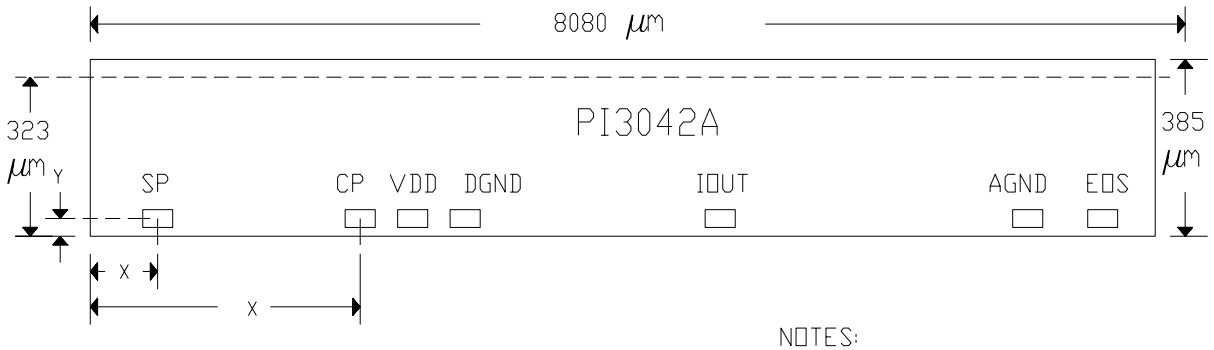

*Figure 1: AMIS-720442-A Block Diagram*

Table 1: Pad Symbols and Functions

| Symbol | Function |
|---|---|
| SP | Start pulse: input clock to start the line scan |
| CP | Clock pulse: input clock to clock of the shift register |
| VDD | Positive supply: +5V supply connected to substrate |
| DGND | Digital ground: connection topside common |
| IOUT | Signal current output: output for video signal current |
| AGND | Analog ground: connection topside common |
| EOS | End-of-scan pulse: output from the shift register at end-of-scan |

## 2.0 Bonding Pad Output Locations and Die Dimensions

Figure 2 shows the die dimensions of the image sensor and the bonding pad locations for the AMIS-720442-A sensor chip. The location is referenced to the lower left corner of the die.




| PAD | FUNCTION | Y | X |
|---|---|---|---|
| SP | START INPUT | 70 | 928 |
| CP | CLOCK INPUT | 70 | 3208 |
| VDD | +5 SUPPLY | 70 | 3505 |
| DGND | GROUND | 70 | 3768 |
| IOUT | VIDEO SIGNAL OUT | 70 | 4922 |
| AGND | ANALOG GROUND | 70 | 6463 |
| EOS | SCAN OUTPUT | 70 | 6742 |

NOTES:
1. THE DRAWING IS NOT TO SCALE.
2. THE DIE LENGTH AND WIDTH ARE GIVEN AS SHOWN.
3. THE PAD LOCATION ARE GIVEN IN THE TABLE
4. THERE ARE TWO EXAMPLES OF THE X AND Y LOCATIONS SHOWN ON THE FIRST TWO PADS. THEY ARE MEASURED TO THE LEFT BOTTOM CORNER OF THE PAD OPENNING ALL PAD OPENNING ARE 140 X 80
5. ALL DIMENSIONS ARE IN µm.
6. SENSOR LINE IS INDICATED BY THE DOTTED LINE.

*Figure 2: Bonding Pad and Chip Layout*

## 3.0 Wafer Scribe Lines Bordering the Die

Figure 3 shows the wafer scribe lines bordering the AMIS-720442-A sensor chip. The wafer thickness is 350µcrons.

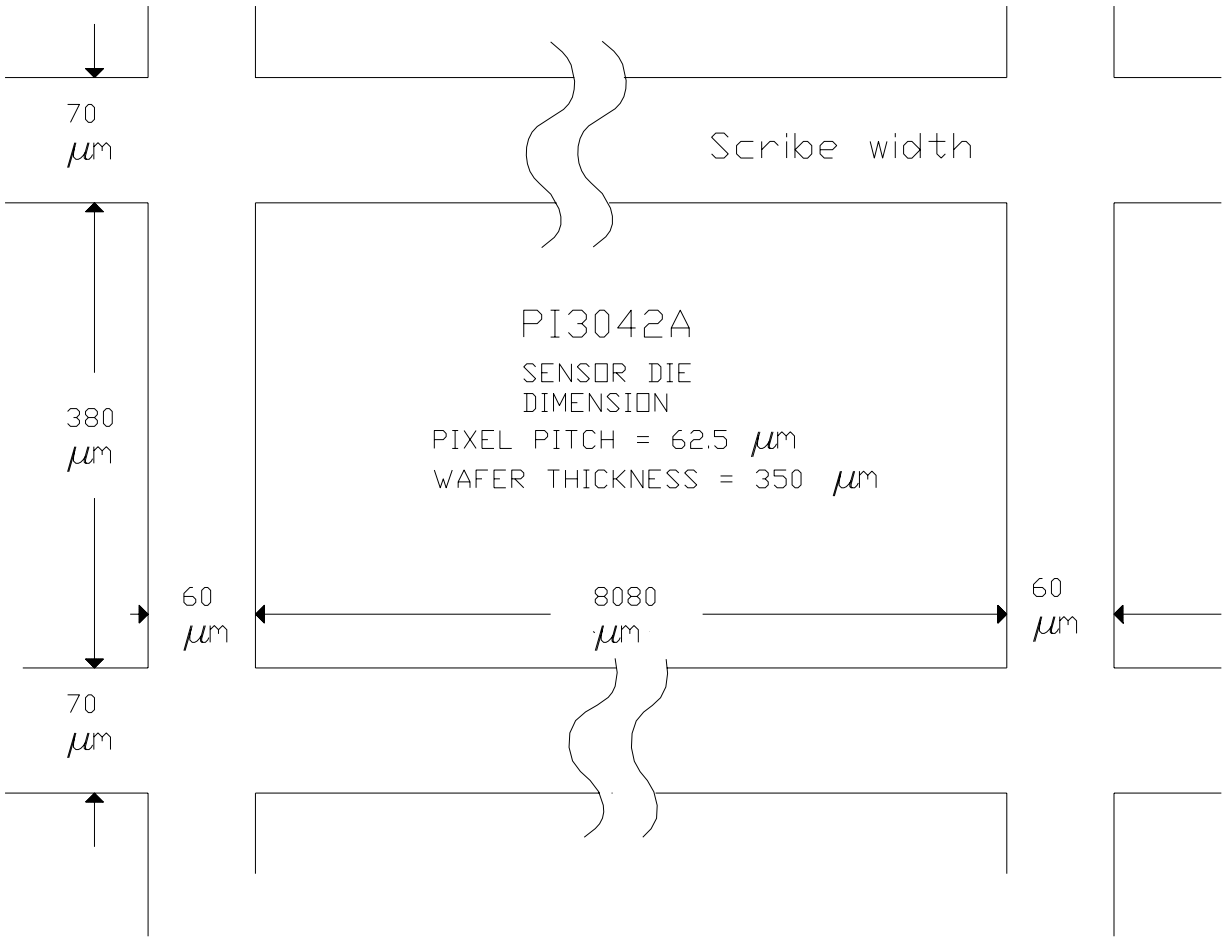



*Figure 3: Wafer Scribe Lines*

## 4.0 Output Circuit of the Image Sensor

The video signal from each photo-site is connected to a common video line on the sensor. Each photo-site is composed of a phototransistor with a series MOS switch connecting its emitter to a common video line. The video line is connected to the pad labeled IOUT. The photo-sites are read out upon the closure of the MOS switch, which is sequentially switched on and off by its internal scanning shift register. See Figure 1. For the clock and timing operation image sensor see Figure 11. The photo-sensing element is the base of the phototransistor where it detects and converts the light energy to proportional charges and stores them in its base and collector capacitance. When the MOS switch is activated, the emitter is connected to the video line and acts as the source follower, producing an impulse current proportional to the stored charges in the base. This current is a discrete-time analog signal output called the video pixel. The charges in the video pixel are proportional to the light energy impinging in the neighborhood of its photo-sites. Figure 4 shows an output structure of four photo-sites out of 128. The multiplexing MOS switch in each photo-site terminates into the output pad, IOUT, through a common video line. As the shift register sequentially accesses each photo-site the charges of the video pixel are sent to the IOUT where they are processed with an external signal conversion circuit (see Section 5.0).

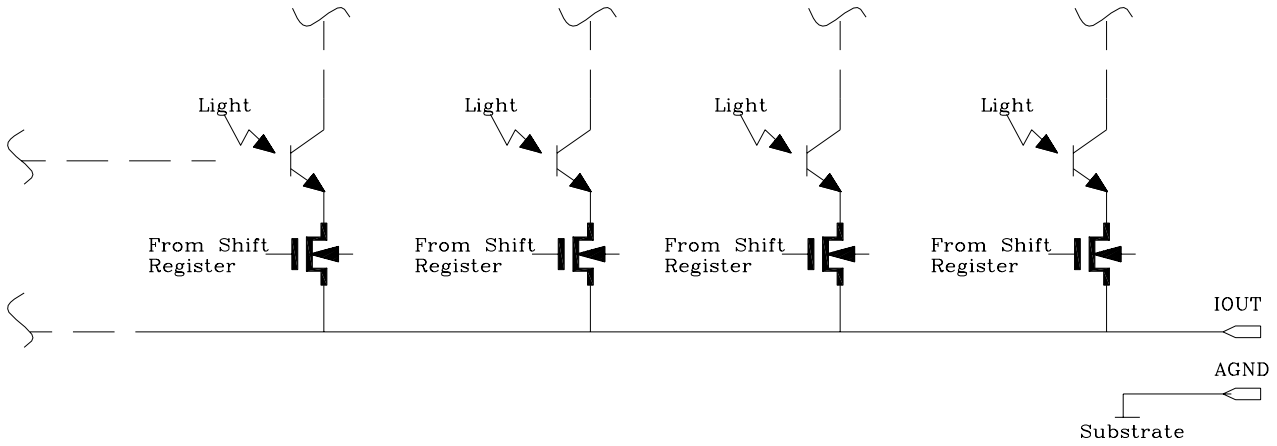



*Figure 4: Video Pixel Output Structures*

## 5.0 Signal Conversion Circuit

Figure 5 is an example of the charge conversion that is used in the CIS modules. It is usually bonded on the same PCB on which the image sensors are bonded. In applications where cost is an important factor, this simple circuit provides the cleanest technique in processing the video output. It integrates all the currents from each pixel element onto a capacitor, CAP. It also sums the energy of the switch edge along with the signal current pulses, minimizing the switching patterns on the video pixels. The summed charges stored on the CAP produce a pixel voltage. This voltage amplitude is proportional to the charge from the current pulse and the value of the CAP.

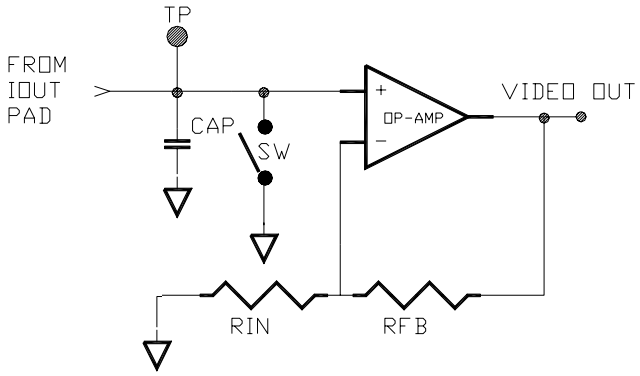



*Figure 5: Video Output Test and Application Circuit*

Since switching energies are components with high frequencies, they tend to integrate to a 0 value and the remainder adds a constant value to off-set the dark level. After the pixel is integrated, the CAP is reset to 0V by activating the shunt switch (SW), that connects the video line to ground prior to accessing the following pixel element. Figure 6, which depicts a typical pixel voltage waveform, shows that the shunt time is controlled with CP. SW activation and the reset to the dark reference level of the pixel element storage occur simultaneously, initializing the pixel for its integration process cycle. The signal pixels Vp(n) is referenced to its dark level as it is seen in Figure 6.

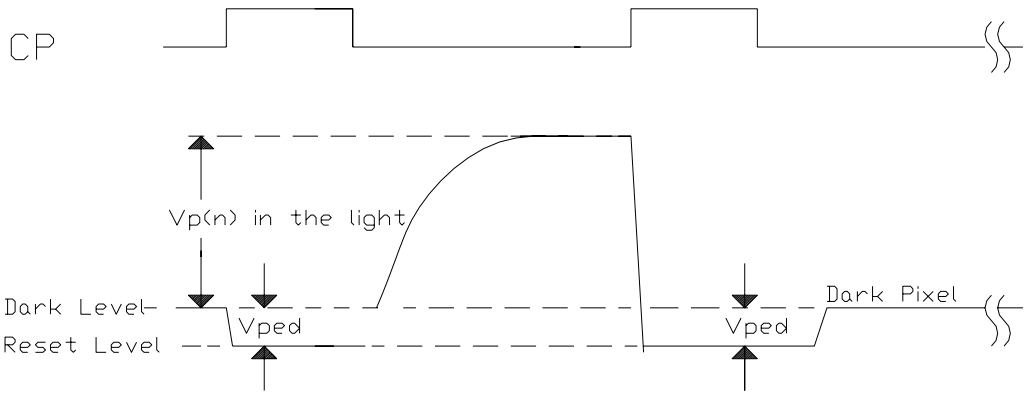



*Figure 6: Single Pixel Video Output*

# 6.0 Two Test Setups for Specifications and Performance

### 6.1 First Setup

The standard specifications are the image sensor tests that are performed on the wafer probe machine where each device on the wafer is tested in production. However, the data in these measurements are measured with a clock frequency at a fixed 500kHz. Since the pixel rate is equal to the clock rate, the pixel rate is also at 500kHz. The specification under Section 7.0 is the wafer probe specifications, Table 2.

### 6.2 Second Setup

The CIS modules made with these devices operate in excess of 5.0MHz. Accordingly the wafer probe specifications are supplemented with high frequency clocking performance using an A6 length modules PCB board.

# 7.0 Electro-Optical Characteristics (25°C)

The electro-optical characteristics of the AMIS-720442-A imaging sensor chip are listed in Table 2. This is the wafer probe specification used to test each die at 25°C.

Table 2: Electro-Optical Characteristics

| Parameters | Symbols | Typical | Units | Notes |
|---|---|---|---|---|
| Number of photo-elements | | 128 | Elements | |
| Pixel-to-pixel spacing | | ~62.5 | µm | |
| Line scanning rate | Tint (1) | 128/Fclk | µs/line | |
| Clock frequency | Fclk (2) | 500 | kHz | See Note 2 for higher clock speed (maximum 5MHz) |
| Output voltage | Vpavg (3) | 1.8 ± 0.35 | V | |
| Output voltage non-uniformity | Up (4) | ± 7.5 | % | |
| Dark output voltage | Vd (5) | <100 | mV | |
| Dark output non-uniformity | Ud (6) | <100 | mV | |
| Adjacent pixel non-uniformity | Upadj (7) | <7.5 | % | |
| Chip-to-chip non-uniformity | Ucc (8) | ± 7.5 | % | |

**Notes:**

(1) Tint stands for the line scanning rate or the integration time. It is determined by the time interval between two start pulses, where the start pulses start the line-scan process, as soon as, CP, module clock, acquires it and shifts it into the internal shift register. To calculate the minimum integration time in a scan it is number of pixels in the scan divided by the clock frequency. In a CIS module it is the number of sensors times the number of pixels in the sensor, all over the clock frequency. This time is especially set for the wafer probes in order to calibrate the Vpavg, see Note (3).

(2) Fclk is the device's clock, CP, frequency and it is, also, equal to the pixel rate. In the wafer test Fclk is set to 500kHz. However, AMIS has been successfully mass-producing high frequency CIS modules, using only the wafer test to qualify them. Hence, the device, which is tested on an A6 size module's PCB board at the standard high speed, meets specifications.

(3) Vpavg = $\sum$Vp(n)/Npixels (average level in one line scan).
Where Vp(n) is the amplitude of $n^{th}$ pixel in the sensor chip and Npixels is the total number of pixels in sensor chip. Vpavg is converted from impulse current video pixel into a voltage output. See Figure 4, in Section 4.0 and Figure 5, in Section 5.0.
Vpavg is calibrated for each image sensor type because of probe card variations, as well as, the interfacing circuits to the wafer probe machine.

(4) Up is the uniformity specification, measured under a uniform exposing light exposure. Up = [Vp(max) - Vpavg] / Vpavg x 100% or [Vpavg - Vp(min)] / Vpavg} x 100%, whichever is greater.
Where Vp(max) is the maximum pixel output voltage in the light.
Vp(min) is the minimum pixel output voltage in the dark.
The pixel Vp(n) is one $n^{th}$ pixel in Npixels in the sensor.

(5) Vd = $\sum$Vp(n)/Npixels. Where Vp(n) is the pixels signal amplitude of the $n^{th}$ pixel of the sensor. Dark is where light is off, leaving the image surface unexposed.

(6) Ud = Vdmax – Vdmin.

(7) Upadj = MAX[ | (Vp(n) - Vp(n+l) | / Vp(n)) x 100%. Upadj is the non-uniformity in percentage. It is the amplitude difference between two neighboring pixels.

(8) Ucc is the uniformity specifications, measured among the good die on the wafer. Under uniform light exposure the sensors are measured and calculated with following algorithm: Vpavg of all the good dies on the wafer are averaged and assigned VGpavg. Then the die with maximum Vpavg is assigned Vpavg(max), and the one with minimum Vpavg is assigned Vpavg(min). Then UCC = {[Vpavg(max)-Vpavg(min)]/VGpavg}x100.

## 8.0 Measuring the High Frequency Performance of the Devices

The AMIS-720442-A devices were tested on an A6 length standard CIS module's PCB. Thirteen sensors were bonded on the PCB board along with its support circuits, such as clock buffer circuits, the shunt switch, SW and its amplifier. The board's video line capacitance, input capacitance of SW and input capacitance of the amplifier become part of the CAP. The A6 PCB was selected because together with the shunt switch, SW, and with its amplifier input, the video line had a typical value of ~100pf, including its stray from its PCB copper traces. Another reason for this selection is that the AMIS-720442-A wafer probe tests of these devices are similarly setup using this method.

By removing RIN, the amplifier gain was set to one. Then with the total value of CAP at ~100pf the video pixels voltage amplitude gives a measure of the approximate pixel charge. Note that the amplifier is a 1:1 buffer amplifier that serves to isolate the video line from the measuring instruments. Further note that when the modules are produced, RIN is in the circuit as variable resistor. Then, in production of the CIS modules, the video output amplitude, Vpavg, can be adjusted to the module's specified level. This factory adjust is required because the exposure is fixed (Exposure = Light Power x Time). For example, the module's light power is fixed and integration's time, tint, is fixed. Note that tint is fixed in accordance to requirements of the user or is specified for the factory adjustment procedure during production. In either case, the light exposure is fixed. Accordingly, to adjust the voltage amplitude to the specified level, RIN is used.

Since the sensor response varies as a function of color, the AMIS-720442-A is measured with a Yellow-Green LED light source, as well as the Red (660nm) LED light source. The light sources were selected because historically, these LED light bars were used in the CIS industry and accepted in the low-cost CIS markets. Today, the users are turning towards the light guides or light pipes as the costs have been reduced and the technology of the image sensor continually improves. Yet, in low-cost applications and especially in mid-size volume production, the light bars and the older image sensors persistently continues to be in demand by the scanning industry.

The high frequency performance specifications are graphical curves showing the video output, Vpavg, response to its applied light exposure. Although four exposure response graphs serve as good design reference for the designer who has prior knowledge of the image power that will be exposing image sensors, this is not always the case, for example, in designing and producing a CIS module. So to this end, the A6 PCB board, used to characterize the light exposure to video response specification, is enclosed in its A6 module housing and measured for its standard CIS parameters. These modules were fabricated exactly as their production counter-part except that the gain of the amplifier is set one. The measurements were conducted with two different LED bars, one Yellow-Green and the other Red.

## 9.0 Video Output Response under Exposure

The four video signal output as a function of light exposure are given in Graphs A, B, C, and D. The measurements are conducted in black box that enclosed the light source, the PCB and the instrument to measure the light power. The LED source mounted at the top radiated its light energy directly on the image sensor of the A6 PCB that was lying flat at the bottom of box. The video output was measured at the amplifier output of the A6 PCB. The PCB setup condition is described Section 8.0. Note that the gain of the amplifier is set to one. Also the clock duty cycle is set to 25 percent for the 2.0MHz clock frequency and set to 50 percent for the 5.0MHz.

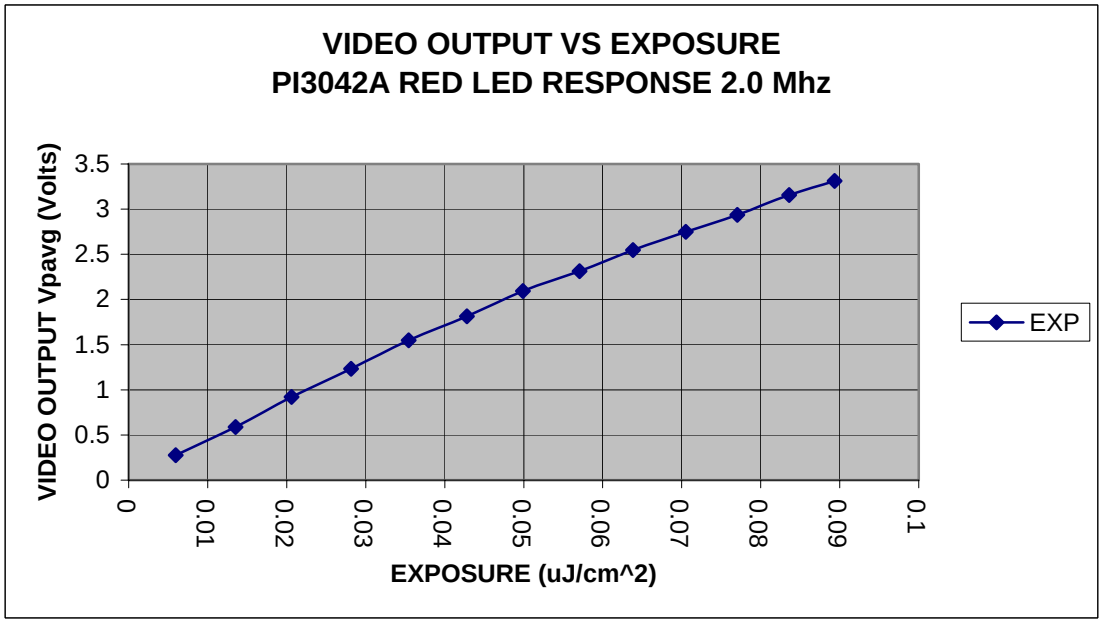



*Figure 7: A Typical Video Output a as Function of Light Exposure*

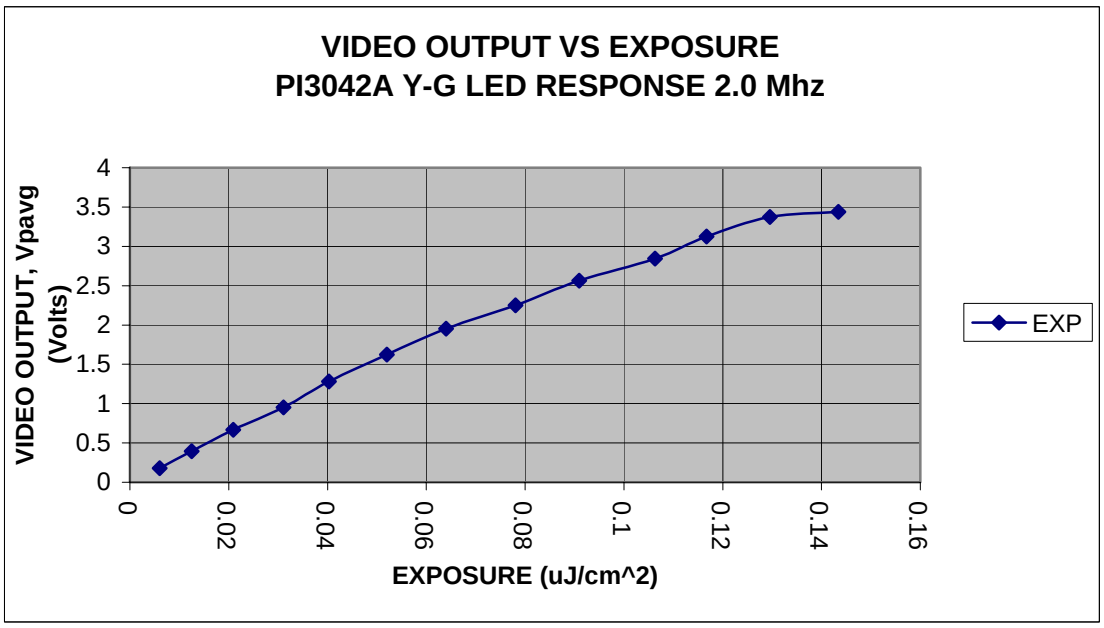



*Figure 8: Graph B. A Typical Video Output a as Function of Light Exposure*

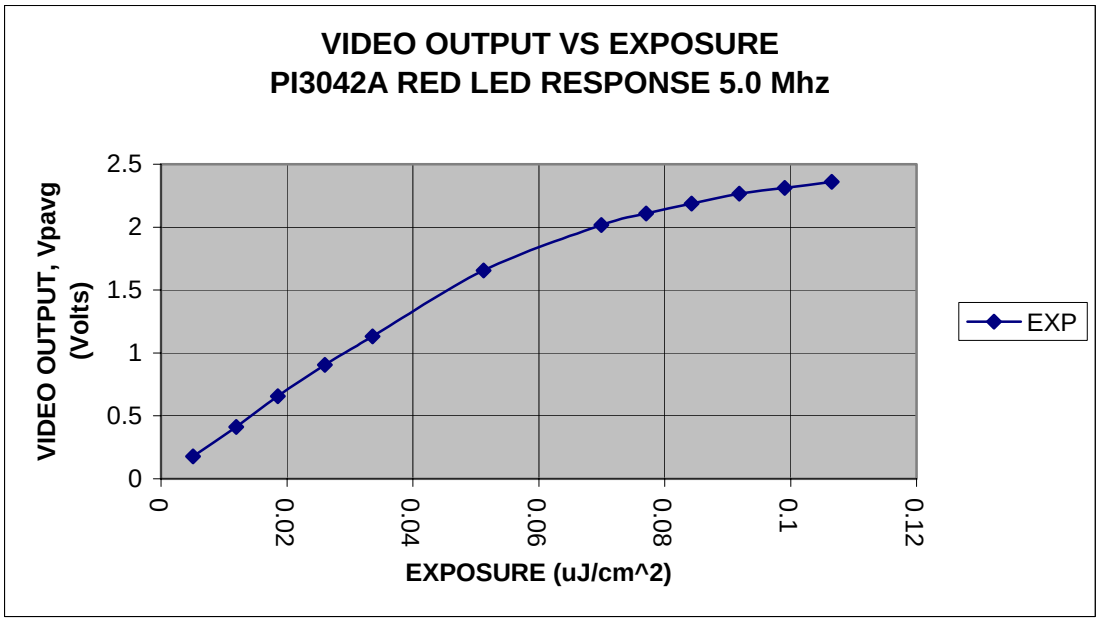



*Figure 9: Graph C. A Typical Video Output a as Function of Light Exposure*

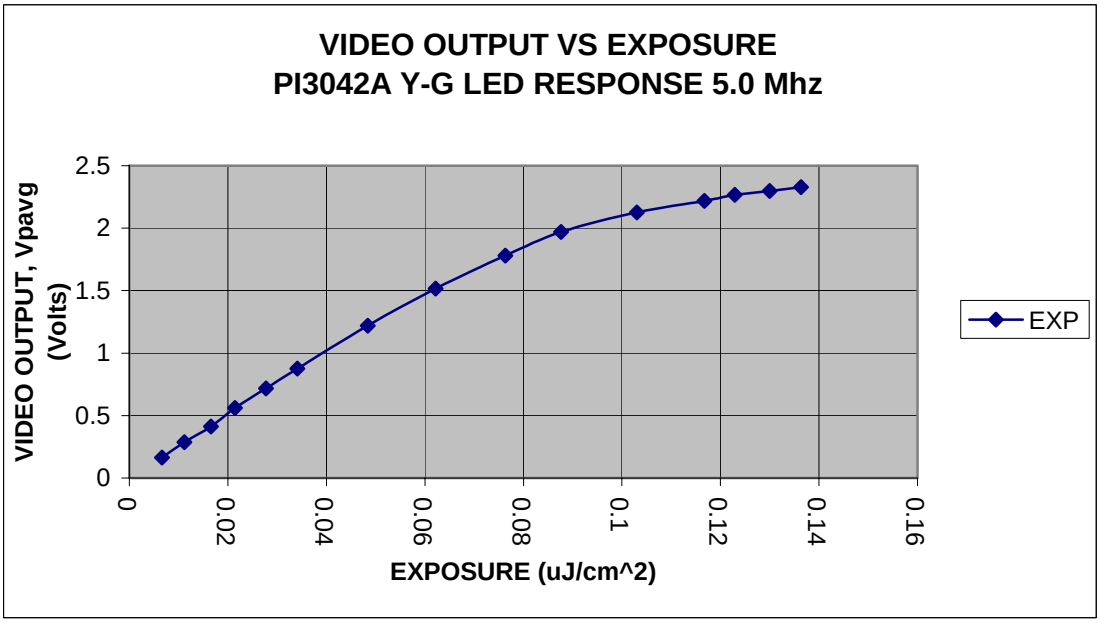



*Figure 10: Graph D. A Typical Video Output a as Function of Light Exposure*

## 10.0 A6 Module with AMIS-720442-A High Frequency Specifications

Table 3: Electro-Optical Characteristics at High Frequency

| Red 660 LED Bar, A6 PCB in A6 Module Housing, at 2.0MHz Clock | | | | |
|---|---|---|---|---|
| **Parameters** | **Symbols** | **Typical** | **Units** | **Remarks** |
| Line scanning rate | Tint (1) | 835 | µs/line | 13 die in the scan, see Note 1 (bottom of Table 6) |
| Clock frequency | Fclk (2) | 2 | MHz | |
| Output voltage | Vpavg (3) | 1.0 | V | Amplifier gain = 1.0, see Note 3 |
| Output voltage non-uniformity | Up (4) | ± 20 | % | LED bar non-uniformity, see Note 4 |
| Dark output voltage | Vd (5) | <15 | mV | |
| Dark output non-uniformity | Ud (6) | <15 | mV | |
| Adjacent pixel non-uniformity | Upadj (7) | <20 | % | |
| LED bar input voltage | VLED (8) | 5.0 | V | LED power varies greatly, see Note 8 |
| LED bar input current | ILED (8) | 90 | mA | LED Power varies greatly, see Note 8 |

Table 4: Electro-Optical Characteristics at High Frequency

| Red 660 LED Bar, A6 PCB in A6 Module Housing, at 5.0MHz Clock | | | | |
|---|---|---|---|---|
| **Parameters** | **Symbols** | **Typical** | **Units** | **Remarks** |
| Line scanning rate | Tint (1) | 334 | µs/line | 13 die in the scan, see Note 1 (bottom of Table 6) |
| Clock frequency | Fclk (2) | 5 | MHz | |
| Output voltage | Vpavg (3) | 0.5 | V | Amplifier gain = 1.0, see Note 3 |
| Output voltage non-uniformity | Up (4) | ± 20 | % | LED bar non-uniformity, see Note 4 |
| Dark output voltage | Vd (5) | <180 | mV | |
| Dark output non-uniformity | Ud (6) | <80 | mV | |
| Adjacent pixel non-uniformity | Upadj (7) | <20 | % | |
| LED bar input voltage | VLED (8) | 5.0 | V | LED power varies greatly, see Note 8 |
| LED bar Input current | ILED (8) | 90 | mA | LED power varies greatly, see Note 8 |

Table 5: Electro-Optical Characteristics at High Frequency

| Y-G LED Bar, A6 PCB in A6 Module Housing, at 2.0MHz Clock | | | | |
|---|---|---|---|---|
| **Parameters** | **Symbols** | **Typical** | **Units** | **Remarks** |
| Line scanning rate | Tint (1) | 835 | µs/line | 13 die in the scan, see Note 1 (bottom of Table 6) |
| Clock frequency | Fclk (2) | 2 | MHz | |
| Output voltage | Vpavg (3) | 0.4 | V | Amplifier gain = 1.0, see Note 3 |
| Output voltage non-uniformity | Up (4) | ± 20 | % | LED bar non-uniformity, see Note 4 |
| Dark output voltage | Vd (5) | <15 | mV | |
| Dark output non-uniformity | Ud (6) | <15 | mV | |
| Adjacent pixel non-uniformity | Upadj (7) | <20 | % | |
| LED bar input voltage | VLED (8) | 5.0 | V | LED power varies greatly, see Note 8 |
| LED bar input current | ILED (8) | 380 | mA | LED power varies greatly, see Note 8 |

Table 6: Electro-Optical Characteristics at High Frequency

| Y-G LED Bar, A6 PCB in A6 Module Housing, at 5.0MHz Clock | | | | |
|---|---|---|---|---|
| **Parameters** | **Symbols** | **Typical** | **Units** | **Remarks** |
| Line scanning rate | Tint (1) | 334 | µs/line | 13 die in the scan, see Note 1 (bottom of Table 6) |
| Clock frequency | Fclk (2) | 5 | MHz | |
| Output voltage | Vpavg (3) | 0.2 | V | Amplifier gain = 1.0, see Note 3 |
| Output voltage non-uniformity | Up (4) | ± 25 | % | LED bar non-uniformity, see Note 4 |
| Dark output voltage | Vd (5) | <160 | mV | |
| Dark output non-uniformity | Ud (6) | <60 | mV | |
| Adjacent pixel non-uniformity | Upadj (7) | <20 | % | |
| LED bar input voltage | VLED (8) | 5.0 | V | LED power varies greatly, see Note 8 |
| LED bar input current | ILED (8) | 380 | mA | LED power varies greatly, see Note 8 |

**Notes:**

(1) Note 1 under Table 2, is a valid definition, except that in the A6 modules has 13 sensors sequentially cascaded, hence, Tint = (13X128)/Fclk for the minimum integration time.

(2) Fclk is the module's clock, CP, frequency and is equal to the pixel rate. Also, the clock duty cycle is set to 25 percent for the 2.0MHz clock frequency and set to 50 percent for the 5.0MHz.

(3) Vpavg = ∑Vp(n)/Npixels (average level in one line scan).
Where Vp(n) is the amplitude of $n^{th}$ pixel in one line scan of the modules. Npixels is the total number of pixels in the module, i.e., 13 die x 128 pixels. The amplitude of Vpavg is adjusted with RIN (which installed in the production module) on all of CIS modules because of variations caused by the LED light sources. The low-cost production LED's light power are known to vary as much as ± 30%.

(4) Up is the uniformity specification, measured under a uniform exposing light exposure. Up = [Vp(max) - Vpavg] / Vpavg x 100% or [Vpavg - Vp(min)] / Vpavg} x 100%, whichever is greater.
Where Vp(max) is the maximum pixel output voltage in the light.
Vp(min) is the minimum pixel output voltage in the dark.
The pixel Vp(n) is one $n^{th}$ pixel in Npixels in the sensor.
In applying the Up definition, Npixels must change. It must include 13 sensors, or 13x128 pixels.
Additionally, because the low-cost LED power variation can be high as ± 30%, the non-uniformities may varies as much as ± 30%. Hence the uniformities are worst because of the LED bar CIS modules.

(5) Vd = ∑Vp(n)/Npixels. Where Vp(n) is the pixels signal amplitude of the $n^{th}$ pixel of the sensor. Dark is where light is off, leaving the image surface unexposed.

(6) Ud = Vdmax – Vdmin.

(7) Upadj = MAX[ | (Vp(n) - Vp(n+l) | / Vp(n)) x 100%. Upadj is the non-uniformity in percentage. It is the amplitude difference between two neighboring pixels.

(8) The low-cost LED light powers are widely specified, worst case as high as ± 30%, hence, the requirement for the Vpavg gain control and the wide Up specifications.

# 11.0 Sensor's Operational Specifications

## 11.1 Absolute Maximum Ratings

Table 7: Absolute Maximum Ratings

| Parameters | Symbol | Maximum Rating | Units |
|---|---|---|---|
| Power supply voltage | VDD | 10 | V |
| Power supply current | IDD | <2.0 | ma |
| Input clock pulse (high level) | Vih | Vdd + 0.5 | V |
| Input clock pulse (low level) | Vil | -0.25 | V |
| Operating temperature | Top | 0 to 50 | °C |
| Operating humidity | Hop | 10 to 85 | RH % |
| Storage temperature | Tstg | -25 to 75 | °C |
| Storage humidity | Hstg | 10 to 90 | RH % |

## 11.2 Recommended Operating Conditions at Room Temperature

Table 8: Recommended Operating Conditions at Room Temperature

| Parameters | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Power supply | VDD | 4.5 | 5.0 | 5.5 | V |
| Input clock pulse high level | Vih (1) | 3.0 | 5.0 | VDD | V |
| Input clock pulse low level | Vil (1) | 0 | 0 | 0.8 | V |
| Operating high level exposed output | IOUT (2) | | See Note 2 | | |
| Clock frequency | Fclk (3) | 0.1 | 2.0 | 5.0 | MHz |
| Clock pulse duty cycle | Duty (4) | | 25 | | % |
| Clock pulse high durations | tw | | 0.125 | | µsec |
| Integration time | Tint | | 0.864 | 10 | ms |
| Operating temperature | Top | | 25 | 50 | °C |

**Notes:**

(1) Applies to both CP and SP

(2) The output is a current that is proportional to the charges, which are integrated on the phototransistor's base via photon-to-electron conversion. For its conversion to voltage pixels see Figure 4, in Section 4.0.

(3) Although the clock frequency, Fclk, will operate the device at less than 100kHz, it is recommended that the device be operated above 500kHz to avoid complication of leakage current build-up. In applications using long CIS module length, such as an array of image sensor > 27, increases the readout time, i.e., increases tint, hence, leakage current build-up occurs.

(4) The clock duty cycle typically is set to 25 percent. However, it can operate with duty cycle as large as 50 percent, which will allow more reset time at the expense of video pixel readout time. At clock frequencies approaching 5.0MHz it is recommended to use 50 percent duty cycle to allow more time for the signal pixel to integrate and settle.

## 12.0 Switching Characteristics at 25°C

The timing relationships of the video output voltage and its two input clocks the start pulse (SP) and the shift register clock, (CP), along with the shift register (EOS) output clock are shown in Figure 11. The switch timing specification for the symbols on the timing diagram is given in Table 9. The digital clocks' levels are +5V CMOS compatible. The video, IOUT, is specified in Figure 4, in Section 4.0.

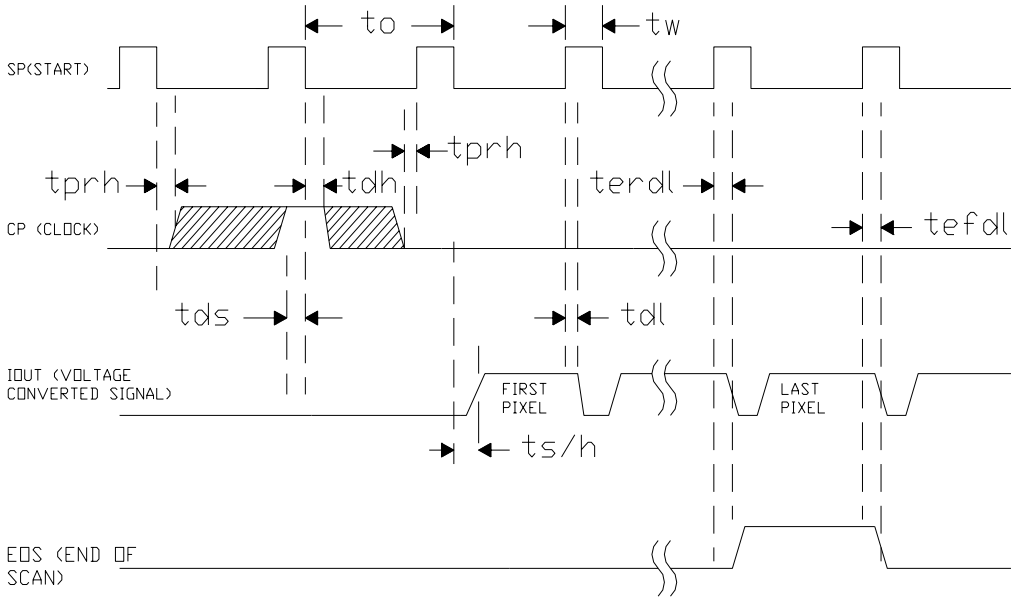



*Figure 11: Timing Diagram of the AMIS-720442-A Sensor*

Table 9: Timing Symbol's Definition

| Item | Symbol | Minimum | Mean | Maximum | Units |
|---|---|---|---|---|---|
| Clock cycle time | to | 200 | | 10000 | ns |
| Clock pulse width(1) | tw | 50 | | | ns |
| Clock duty cycle | | 25 | 50 | 75 | % |
| Data setup time | tds | 20 | | | ns |
| Data hold time | tdh | 20 | | | ns |
| Prohibit crossing time(2) | tprh | | 20 | | ns |
| EOS rise delay | terdl | | 60 | | ns |
| EOS fall delay | tefdl | | 70 | | ns |
| Signal delay time(3) | tdl | | 20 | | ns |
| Signal settling time(3) | ts/h | | 120 | | ns |

**Notes:**

(1) The clock pulse width, tw, varies with frequency, as well as the duty cycle.

(2) Prohibit crossing time is to insure that no two SPs are locked into the shift register for any single scan time. Since the SP is entered into the shift register during its active high level when the CP clock edges falls, the active high of the SP is permitted only during one falling, CP, clock edges for any given scan. Otherwise, multiple SPs will load into the shift register.

(3) Pixel delay times and settling times depend on the employment of the output amplifier. These values, tdl and ts/h, are measured with the amplifier (see Figure 12, using the AMIS-720442-A sensors. Note that the impulse signal current out of the device has pulse width ~ 30ns. Hence, the faster the amplifier with a faster settling time will yield a signal video pulse with faster rise and settle times.

## 13.0 Typical A6 CIS Module Circuit

A typical A6 CIS module circuit, using the AMIS-720442-A sensors, is shown in Figure 12. The circuit is provided as reference to illustrate the interconnection of the AMIS-720442-A for a serially cascaded line of image sensors. It is a typical A6 size CIS module produced by AMIS. It provides the first-time user with additional insight for designing a CIS module and supplements the circuit descriptions given in the Section, Signal Conversion Circuit.

The difference is in the arrangement of the two shunt switches, U3D and U3A. U3D is a counterpart to SW in Figure 5. A DC restoration capacitor, C20, with a value of 500pf, is added between the shunts switch. The first, U3D, clamps the video line to ground to reset the image sensors. Simultaneously, the second, U3A, clamps the node between C15 and the amplifier input to an output reference bias voltage that is on the node between R4 and R9. These resistors are voltage dividers that set the DC operating level of the amplifier's output by applying the same bias voltage to both inputs of the amplifier.

See Figure 12 for the typical A6 CIS module circuit.

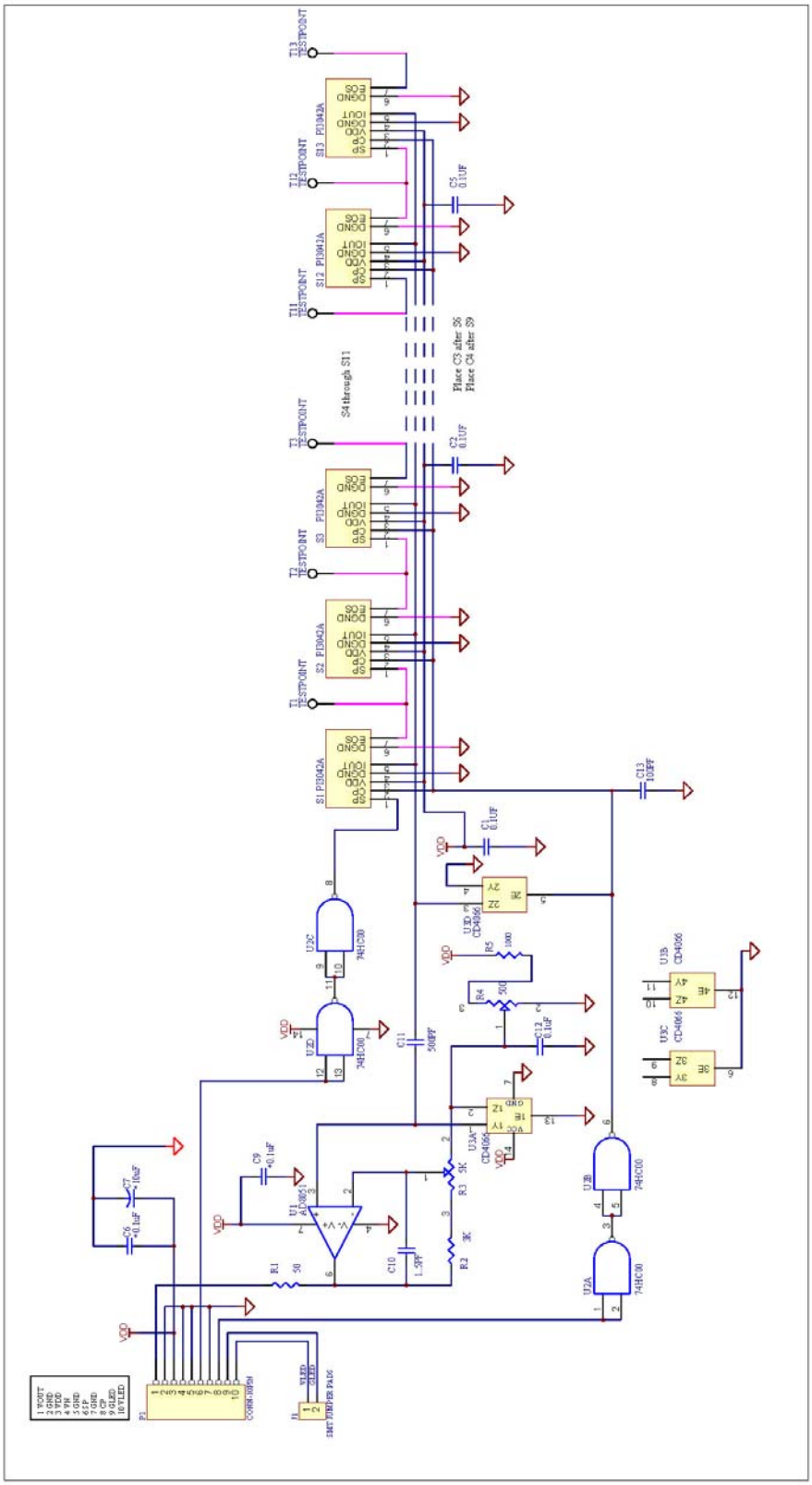


*Figure 12: Typical A6 CIS Module Circuit*

## 14.0 Company or Product Inquiries

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