UNITRODE

Advanced Regulating Pulse Width Modulators

FEATURES

- Fully Interchangeable with Standard UC1524 Family

- Precision Reference Internally Trimmed to ±1%

- High-Performance Current Limit Function

- Under-Voltage Lockout with Hysteretic Turn-on

- Start-Up Supply Current Less Than 4mA

- Output Current to 200mA

- 60V Output Capability

- Wide Common-Mode Input Range for both Error and Current Limit Amplifiers

- PWM Latch Insures Single Pulse per Period

- Double Pulse Suppression Logic

- 200ns Shutdown through PWM Latch

- Guaranteed Frequency Accuracy

- Thermal Shutdown Protection

DESCRIPTION

The UC1524A family of regulating PWM ICs has been designed to retain the same highly versatile architecture of the industry standard UC1524 (SG1524) while offering substantial improvements to many of its limitations. The UC1524A is pin compatible with "non-A" models and in most existing applications can be directly interchanged with no effect on power supply performance. Using the UC1524A, however, frees the designer from many concerns which typically had required additional circuitry to solve.

The UC1524A includes a precise 5V reference trimmed to ±1% accuracy, eliminating the need for potentiometer adjustments; an error amplifier with an input range which includes 5V, eliminating the need for a reference divider; a current sense amplifier useful in either the ground or power supply output lines; and a pair of 60V, 200mA uncommitted transistor switches which greatly enhance output versatility.

An additional feature of the UC1524A is an under-voltage lockout circuit which disables all the internal circuitry, except the reference, until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low power, off-line supplies. The turn-on circuit has approximately 600mV of hysteresis for jitter-free activation.

Other product enhancements included in the UC1524A's design include a PWM latch which insures freedom from multiple pulsing within a period, even in noisy environments, logic to eliminate double pulsing on a single output, a 200ns external shutdown capability, and automatic thermal protection from excessive chip temperature. The oscillator circuit of the UC1524A is usable beyond 500kHz and is now easier to synchronize with an external clock pulse.

The UC1524A is packaged in a hermetic 16-pin DIP and is rated for operation from -55°C to +125°C. The UC2524A and 3524A are available in either ceramic or plastic packages and are rated for operation from -25°C to +85°C and 0°C to 70°C, respectively. Surface mount devices are also available.

BLOCK DIAGRAM

UDG-99178
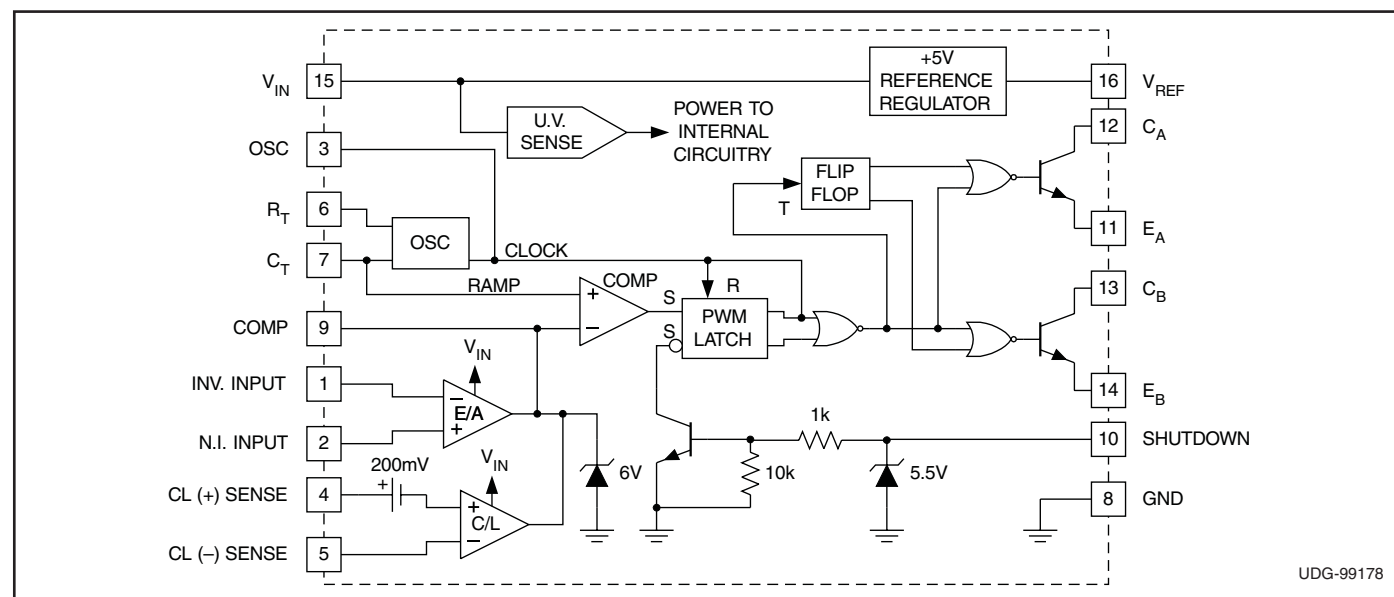
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V$_{IN}$) 40V
Collector Supply Voltage (V$_C$) 60V
Output Current (each Output) 200mA
Maximum Forced Voltage (Pin 9, 10) . . . . -3 to +5V
Maximum Forced Current (Pin 9, 10) . . . . ±10mA
Reference Output Current 50mA
Oscillator Charging Current 5mA
Power Dissipation at T$_A$ = +25°C. 1000mW
Power Dissipation at T$_C$ = +25°C 2000mW
Operating Temperature Range . . . . -55°C to +125°C
Storage Temperature Range. . . . . -65°C to +150°C
Lead Temperature, (Soldering, 10 seconds) . . . . +300°C
*Note: Consult packaging section of Databook for thermal limitations and considerations of package.*

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package

Inv Input	1	16 +5V V$_{REF}$
Non-Inv Input	2	15 +V$_{IN}$
OSC/Sync	3	14 Emitter B
C.L. (+) Sense	4	13 Collector B
C.L. (-) Sense	5	12 Collector A
R$_T$	6	11 Emitter A
C$_T$	7	10 Shutdown
Ground	8	9 Compensation

CONNECTION DIAGRAMS

PLCC-20, LCC-20 (TOP VIEW)
Q or L Package
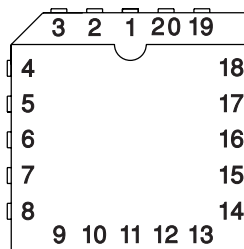
PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Inv. Input	2
Non-Inv. Input	3
OSC/SYNC	4
C.L. (+) sense	5
N/C	6
C.L. (-) sense	7
R$_T$	8
C$_T$	9
Ground	10
N/C	11
Compensation	12
Shutdown	13
Emitter A	14
Collector A	15
N/C	16
Collector B	17
Emitter B	18
+V$_{IN}$	19
+5V V$_{REF}$	20

ELECTRICAL CHARACTERISTICS:
Unless otherwise stated, these specifications apply for T$_A$ = -55°C to +125°C for the UC1524A, -25° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; V$_{IN}$ = V$_C$ = 20V, T$_A$ = T$_J$.

PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Turn-on Characteristics								
Input Voltage	Operating Range after Turn-on	8		40	8		40	V
Turn-on Threshold		6.5	7.5	8.5	6.5	7.5	8.5	V
Turn-on Current	V$_{IN}$ = 6V		2.5	4		2.5	4	mA
Operating Current	V$_{IN}$ = 8 to 40V		5	10		5	10	mA
Turn-on Hysteresis*			0.5			0.5		V
Reference Section								
Output Voltage	T$_J$ = 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
	Over Operating Range	4.9		5.1	4.85		5.15	V
Line Regulation	V$_{IN}$ = 10 to 40V		10	20		10	30	mV
Load Regulation	I$_L$ = 0 to 20 mA		20	25		20	35	mV
Temperature Stability*	Over Operating Range*		20	25		20	35	mV
Short Circuit Current	V$_{REF}$ = 0, 25°C ≤ T$_J$ ≤ 125°C		80	100		80	100	mA
Output Noise Voltage*	10Hz ≤ f ≤ 10kHz, T$_J$ =25°C		40			40		μVrms
Long Term Stability*	T$_J$ =125°C, 1000 Hrs.		20	50		20	50	mV

*   *These parameters are guaranteed by design but not 100% tested in production.*

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1524A, -25° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; V_{IN} = V_C = 20V, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (Unless otherwise specified, R_T = 2700Ω, C_T = 0.01 mfd)								
Initial Accuracy	T_J = 25°C	41	43	45	39	43	47	kHz
	Over Operating Range	40.2		45.9	38.2		47.9	kHz
Temperature Stability*	Over Operating Temperature Range		1	2		1	2	%
Minimum Frequency	R_T = 150kΩ, C_T = 0.1mfd			140			120	Hz
Maximum Frequency	R_T = 2.0kΩ, C_T = 470pF	500			500			kHz
Output Amplitude*		3	3.5		3	3.5		V
Output Pulse Width*		0.29	0.5	1.0	0.3	0.5	1.0	µs
Ramp Peak		3.3	3.5	3.7	3.3	3.5	3.7	V
Ramp Valley	T_J = 25°C	0.7	0.8	0.9	0.7	0.8	0.9	V
Ramp Valley T.C.			-1.0			-1.0		mV/°C
Error Amplifier Section (Unless otherwise specified, V_{CM} = 2.5V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	5		1	10	µA
Input Offset Current			.05	1		0.5	1	µA
Common Mode Rejection Ratio	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
Power Supply Rejection Ratio	V_{IN} = 10 to 40V	70	80		70	80		dB
Output Swing (Note 1)		5.0		0.5	5.0		0.5	V
Open Loop Voltage Gain	ΔV_O= 1 to 4V, $R_L \geq$ 10MΩ	72	80		64	80		dB
Gain-Bandwidth*	T_J = 25°C, A_V = 0dB	1	3		1	3		MHz
DC Transconductance*§	T_J = 25°C, 30kΩ ≤ R_L ≤ 1MΩ	1.7	2.3		1.7	2.3		mS
P.W.M. Comparator (R_T = 2kΩ, C_T = 0.01mfd)								
Minimum Duty Cycle	V_{COMP} = 0.5V			0			0	%
Maximum Duty Cycle	V_{COMP} = 3.8V	45			45			%
Current Limit Amplifier (Unless otherwise specified, Pin 5 = 0V)								
Input Offset Voltage	T_J = 25°C, E/A Set for Maximum Output	190	200	210	180	200	220	mV
	Over Operating Temperature Range	180		220	170		230	mV
Input Bias Current			-1	-10		-1	-10	µA
Common Mode Rejection Ratio	$V_{(pin\,5)}$ = -0.3V to + 5.5V	50	60		50	60		dB
Power Supply Rejection Ratio	V_{IN} = 10 to 40V	50	60		50	60		dB
Output Swing (Note 1)	Minimum Total Range	5.0		0.5	5.0		0.5	V
Open-Loop Voltage Gain	ΔV_O = 1 to 4V, $R_L \geq$ 10MΩ	70	80		70	80		dB
Delay Time*	Pin 4 to Pin 9, ΔV_{IN} = 300mV		300			300		ns
Output Section (Each Output)								
Collector Emitter Voltage	I_C = 100µA	60	80		60	80		V
Collector Leakage Current	V_{CE} = 50V		.1	20		.1	20	µA

* These parameters are guaranteed by design but not 100% tested in production.
§ DC transconductance (g_M) relates to DC open-loop voltage gain according to the following equation: $A_V = g_M R_L$
   where R_L is the resistance from pin 9 to the common mode voltage.
   The minimum g_M specification is used to calculate minimum A_V when the error amplifier output is loaded.
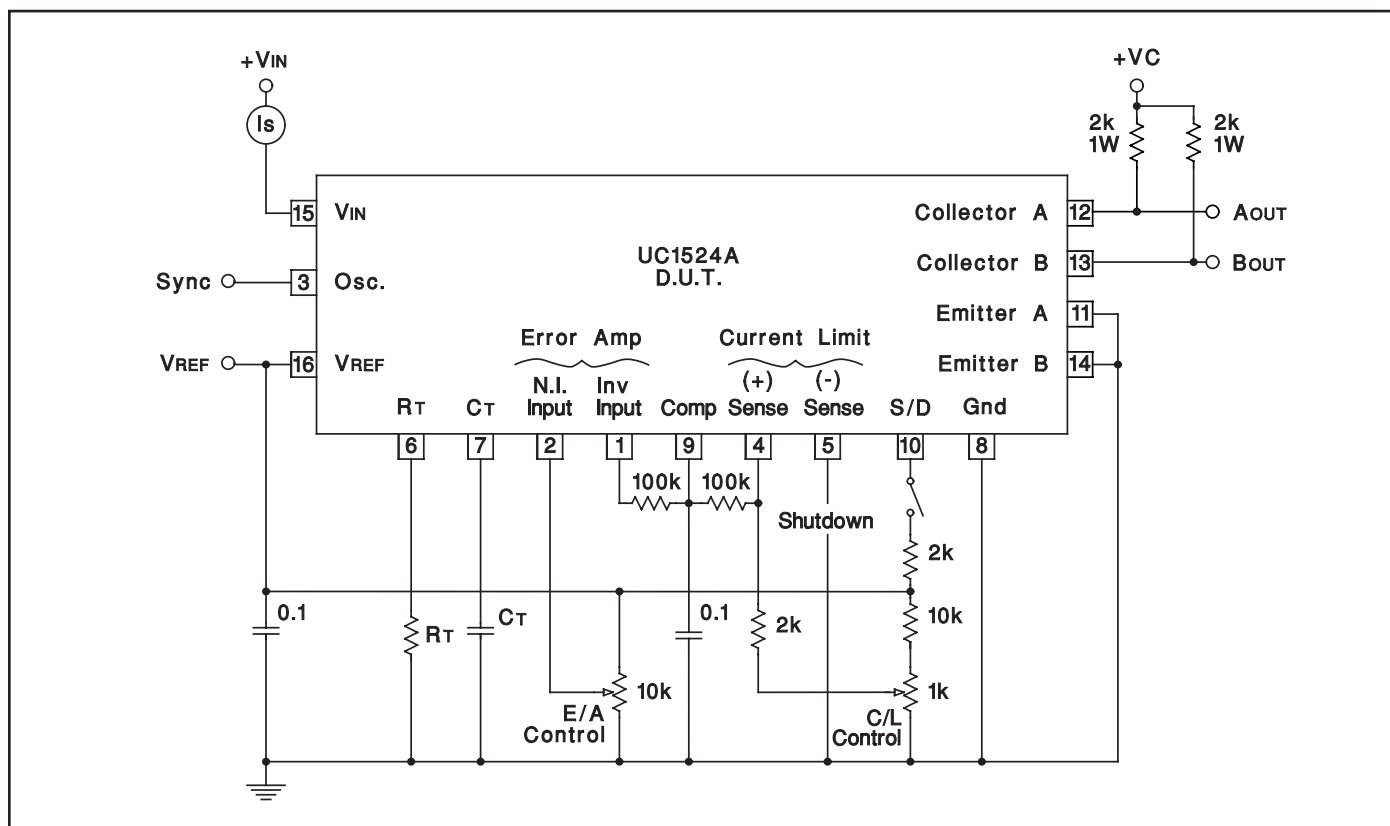Note 1: Min Limit applies to output high level, max limit applies to output low level.

ELECTRICAL CHARACTERISTICS:
Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1524A, -25° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; V_{IN} = V_C = 20V. T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Section (cont.) (Each Output)								
Saturation Voltage	I_C = 20mA		.2	.4		.2	.4	V
	I_C = 200mA		1	2.2		1	2.2	V
Emitter Output Voltage	I_E = 50mA	17	18		17	18		V
Rise Time*	T_J = 25°C, R = 2kΩ		120	400		120	400	ns
Fall Time*	T_J = 25°C, R = 2kΩ		25	200		25	200	ns
Comparator Delay*	T_J = 25°C, Pin 9 to output		300			300		ns
Shutdown Delay*	T_J = 25°C, Pin 10 to output		200			200		ns
Shutdown Threshold	T_J = 25°C, R_C = 2kΩ	0.6	.7	1.0	0.6	.7	1.0	V
S/D Threshold Over Temp.	Over Operating Temperature Range	0.4		1.2	0.4		1.0	V
Thermal Shutdown*			165			165		°C

These parameters are guaranteed by design but not 100% tested in production.
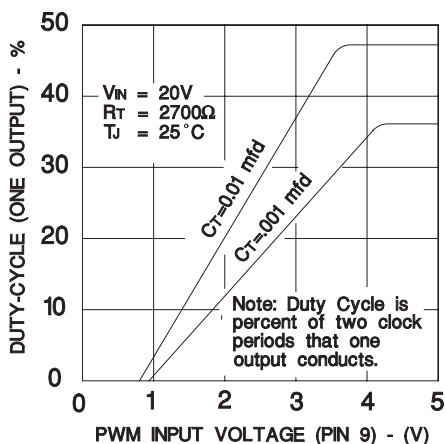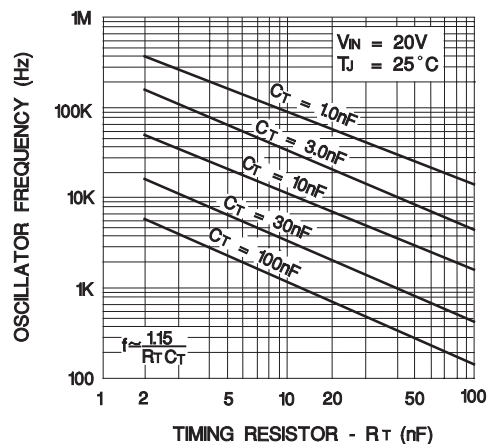
OPEN-LOOP CIRCUIT

Supply Current vs Voltage

QUIESCENT CURRENT (mA)

$T_J = -55°C$
$T_J = 25°C$
$T_J = 125°C$

Note: Outputs Off, $R_T = \infty$

SUPPLY VOLTAGE - V_{IN} (V)
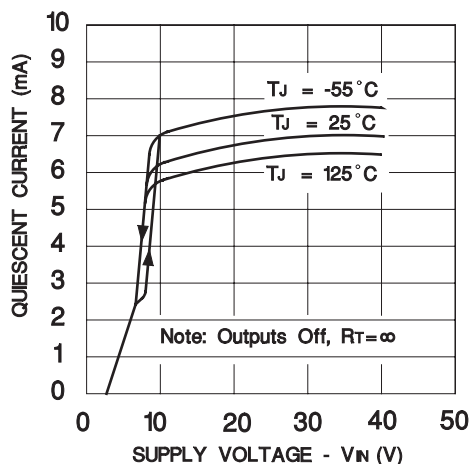
Error Amplifier Voltage Gain and Phase vs Frequency

OPEN-LOOP VOLTAGE GAIN - (dB)
OPEN-LOOP PHASE

$R_L = \infty$
$R_L = 1M\Omega$
$R_L = 300k\Omega$
$R_L = 100k\Omega$
$R_L = 30k\Omega$

$V_{IN} = 20V$
$T_J = 25°C$

VOLTAGE GAIN

R_L is impedance from pin 9 to ground. Values below 30kΩ will begin to limit the maximum duty cycle.

PHASE

-180°
-270°
-360°
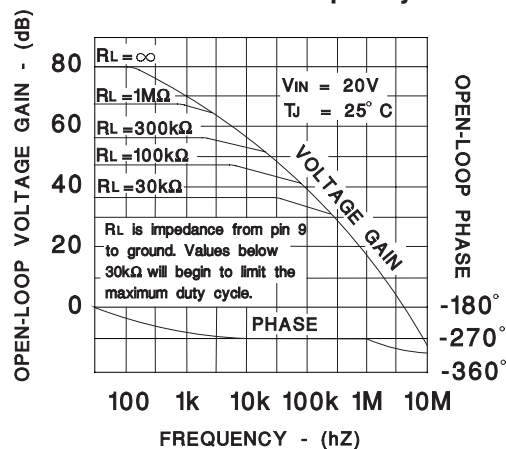
FREQUENCY - (hZ)

Pulse Width Modulator Transfer Function

DUTY-CYCLE (ONE OUTPUT) - %

$V_{IN} = 20V$
$R_T = 2700\Omega$
$T_J = 25°C$

$C_T = 0.01$ mfd
$C_T = .001$ mfd

Note: Duty Cycle is percent of two clock periods that one output conducts.

PWM INPUT VOLTAGE (PIN 9) - (V)

Oscillator Frequency vs Timing Components

OSCILLATOR FREQUENCY (Hz)

$V_{IN} = 20V$
$T_J = 25°C$

$C_T = 1.0nF$
$C_T = 3.0nF$
$C_T = 10nF$
$C_T = 30nF$
$C_T = 100nF$

$f \approx \dfrac{1.15}{R_T C_T}$

TIMING RESISTOR - R_T (nF)

Output Dead Time vs Timing Capacitor Value

OUTPUT DEAD TIME (µs)

$V_{IN} = 20V$
$R_T = 2700\Omega$
$T_J = 25°C$

Note: Dead Time=osc output pulse width plus output delay

TIMING CAPACITOR - C_T (nF)

Output Saturation Voltage

COLLECTOR-TO-EMITTER VOLTAGE (V)

$T_J = 125°C$
$T_J = 25°C$
$T_J = -55°C$

OUTPUT COLLECTOR CURRENT (mA)

Current Limit Amplifier Delay

Output At Pin 9

Overdrive

5%

10%

20%

50%

OUTPUT (V): 6 5 4 3 2 1 0

Input At Pin 4

INPUT (V): 0.2 0.1 0

V_{IN} = 20v, T_J = 25°C
Pin 2 Tied To Pin 16
Pin 5 Grounded

DELAY TIME (µs): 0 1 2 3 4
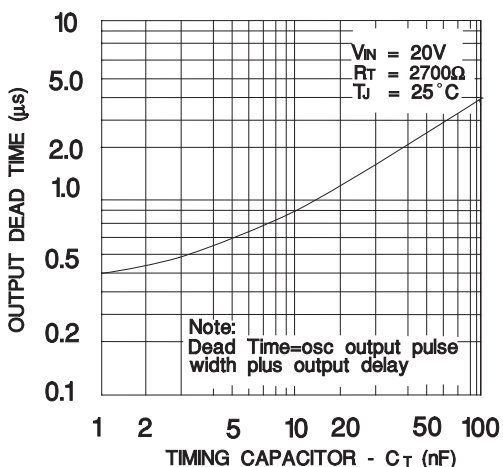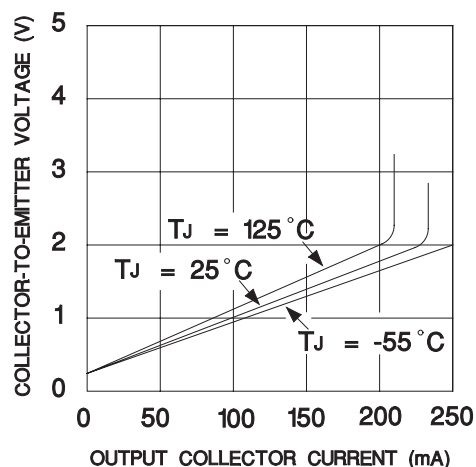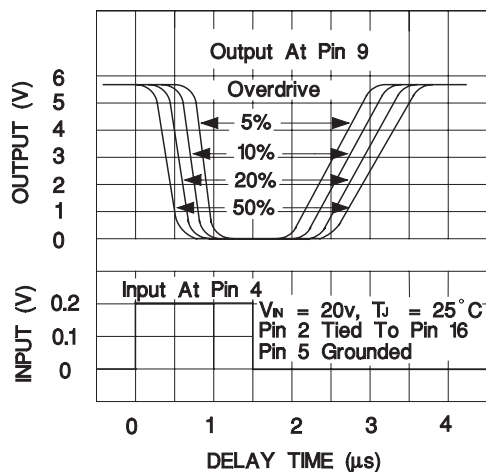
Shutdown Delay From PWM Comparator - Pin 9

OUTPUT (V): 20 15 10 5 0

V_{IN} = 20V
R_L = 2kΩ
T_J = 25°C

Output At
Pin 12 OR 13

INPUT (V): 5 4 3 2 1 0

Input At Pin 9

Note: Minimum input
pulse width to
latch is 200ns

DELAY TIME (µs): 0 1 2 3
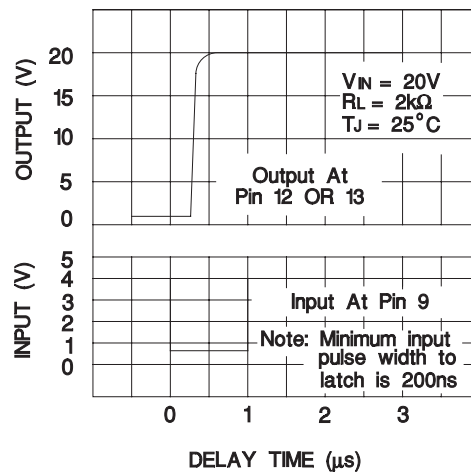
Turn-Off Delay From Shutdown - Pin 10

OUTPUT (V): 20 15 10 5 0

V_{IN} = 20V
R_L = 2kΩ
T_J = 25°C

Output At
Pin 12 or 13

INPUT (V): 1.0 0.5 0

Input at Pin 10

Note: Minimum input pulse width to
latch is 200ns

DELAY TIME (µs): 0 1 2 3
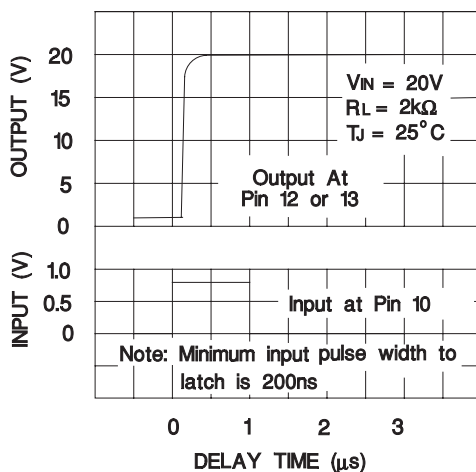
IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.