

# SCSI Termpower Manager

## FEATURES

- Integrated Circuit Breaker Function
- Integrated 0.2Ω Power FET
- SCSI, SCSI-2, SCSI-3 Compliant
- 1μA ICC When Disabled
- Programmable On Time
- Accurate 1.65A Trip Current and 2.0A Max Current
- Fixed 3% Duty Cycle
- Uni-Directional Switch
- Thermal Shutdown

## DESCRIPTION

The UCC3916 SCSI termpower manager provides complete power management, hot swap capability, and circuit breaker functions with minimal external components. For most applications, the only external component required to operate the device, other than supply bypassing, is a timing capacitor which sets the fault time.

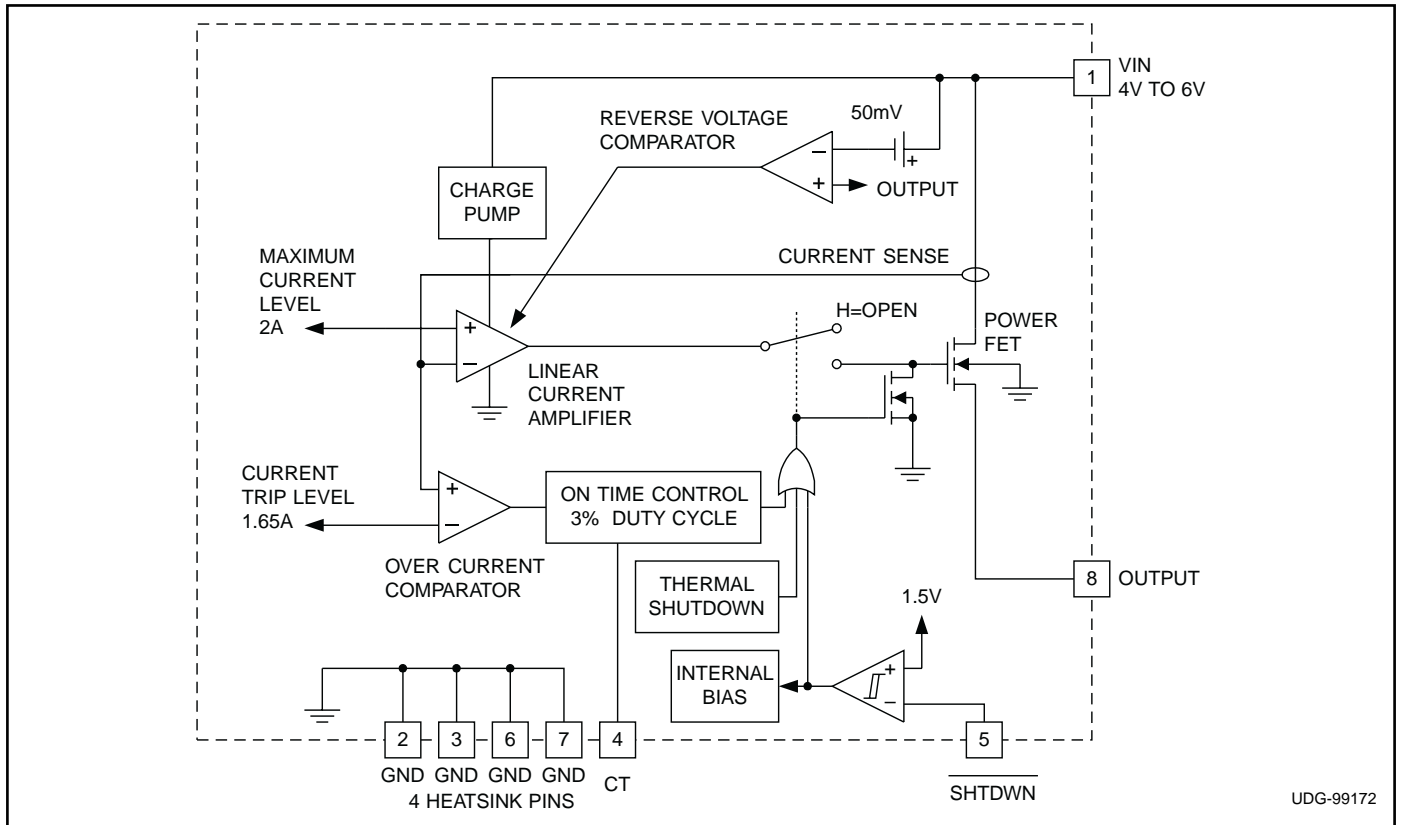
The current trip level is internally set at 1.65A, and the maximum current level is also internally programmed for 2A. While the output current is below the trip level of 1.65A, the internal power MOSFET is switched on at a nominal 220mΩ. When the output current exceeds the trip level but remains less than the maximum current level, the MOSFET remains switched on, but the fault timer starts charging CT. Once the fault time is reached, the circuit will shut off for a time which equates to a 3% duty cycle. Finally, when the output current reaches the maximum current level, the MOSFET transitions from a switch to a constant current source.

The UCC3916 is designed for uni-directional current flow, emulating a diode in series with the power MOSFET.

The UCC3916 can be put in a sleep mode, drawing only 1μA of supply current.

Other features include thermal shutdown and low thermal resistance Small Outline Power package.

## BLOCK DIAGRAM



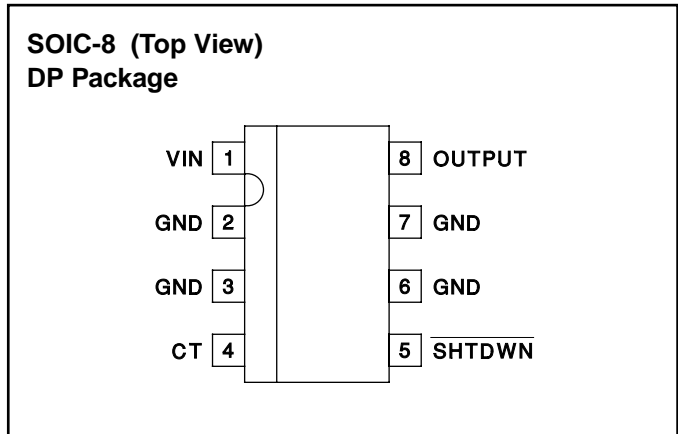
UDG-99172

**ABSOLUTE MAXIMUM RATINGS**

VIN ..... +6V  
 Output Current  
     DC ..... Self Limiting  
     Pulse (Less than 100ns) ..... 20A  
 Storage Temperature ..... -65°C to +150°C  
 Junction Temperature ..... -55°C to +150°C  
 Lead Temperature (Soldering, 10 sec.) ..... +300°C

*Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.*

**CONNECTION DIAGRAM**



**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these parameters apply for TJ = 0°C to +70°C; VIN = 5V, SHTDWN = 2.4V, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Supply Current Section</b>					
ICC			1.00	2.00	mA
ICC - Sleep Mode	SHTDWN = 0.2V		0.50	5	µA
<b>Output Section</b>					
Voltage Drop	IOUT = 1A		0.22	0.33	V
	IOUT = 1.5A		0.33	0.50	V
	IOUT = 1.65A		0.40	0.60	V
Trip Current		-1.8	-1.65	-1.5	A
Max Current		-2.4	-2	-1.65	A
Reverse Leakage	VIN = 4.5V, VOUT = 5V		6	20	µA
	VIN = 0V, VOUT = 5V		0.50	9	µA
Soft Start Time	Initial Startup		50		µs
Short Circuit Response			100		ns
<b>Fault Section</b>					
CT Charge Current	VCT = 1.0V	-45	-36.0	-27	µA
CT Discharge Current	VCT = 1.0V	0.90	1.0	1.50	µA
Output Duty Cycle	VOUT = 0V	2.00	3.00	6.00	%
CT Charge Threshold		0.4	0.5	0.6	V
CT Discharge Threshold		1.2	1.4	1.8	V
Thermal Shutdown			170		°C
Thermal Hysteresis			10		°C
<b>Shutdown Section</b>					
Shutdown Threshold			1.5	3.0	V
Shutdown Hysteresis			150	300	mV
Shutdown Bias Current	SHTDWN = 1.0V		100	500	nA

Note 1: All voltages are with respect to ground.

**PIN DESCRIPTIONS**

**CT:** A capacitor is applied between this pin and ground to set the maximum fault time. The maximum fault time must be more than the time to charge external capacitance. The maximum fault time is defined as:

$$T_{FAULT} = 28 \cdot 10^3 \cdot CT.$$

Once the fault time is reached the output will shutdown for a time given by:

$$T_{SD} = 1 \cdot 10^6 \cdot CT$$

this results in a 3% duty cycle. 0.1µF is recommended for SCSI applications to achieve the normal maximum capacitance on the Tempwr line.

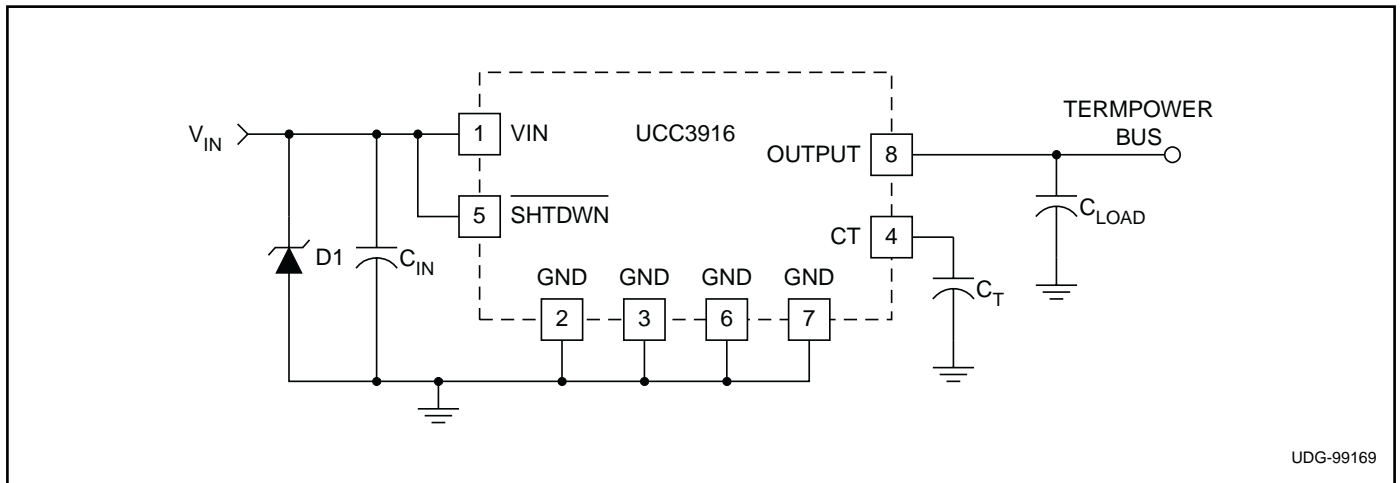
**SHTDWN:** The IC enters a low-power sleep mode when this pin is low and exits the sleep mode when this pin is high.

**VIN:** Input voltage to the circuit breaker, ranging from 4V to 6V.

**VOUT:** Output voltage of the circuit breaker. When switched, the output voltage is approximately:

$$V_{OUT} = V_{IN} - (220m\Omega) \cdot I_{OUT}.$$

**TYPICAL APPLICATION**



UDG-99169

**APPLICATION INFORMATION**

**Protecting The UCC3916 From Voltage Transients**

The parasitic inductance associated with the power distribution can cause a voltage spike at VIN if the load current is suddenly interrupted by the UCC3916. *It is important to limit the peak of this spike to less than 6V to prevent damage to the UCC3916.* This voltage spike can be minimized by:

- Reducing the power distribution inductance (e.g., twist the positive (+) and negative (-) leads of the power supply feeding VIN pin, locate the power supply close to the UCC3916 or use a PCB ground plane).
- Decoupling VIN with a capacitor, CIN, located close to the VIN. This capacitor is typically less than 1µF to limit the inrush current.
- Clamping the voltage at VIN below 6V with a Zener diode, D1, located close to the VIN pin.

**SAFETY RECOMMENDATIONS**

Although the UCC3916 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3916 is intended for use in safety critical applications where UL<sup>®</sup> or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3916 will prevent the fuse from blowing virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.