

TM124MBK36C, TM124MBK36S 1048576 BY 36-BIT  
 TM248NBK36C, TM248NBK36S 2097152 BY 36-BIT  
 DYNAMIC RAM MODULE

SMMS138B – MARCH 1992 – REVISED JUNE 1995

- Organization  
 TM124MBK36C . . . 1048576 × 36  
 TM248NBK36C . . . 2097152 × 36
- Single 5-V Power Supply (±10% Tolerance)
- 72-pin Leadless Single In-Line Memory Module (SIMM)
- TM124MBK36C – Utilizes Eight 4-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages and Two 4-Megabit Quad-CAS DRAMs in Plastic SOJ Packages
- TM248NBK36C – Utilizes Sixteen 4-Megabit DRAMs in Plastic SOJ Packages and Four 4-Megabit Quad-CAS DRAMs in Plastic SOJ Packages
- Long Refresh Period  
 16 ms (1024 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Output
- Common  $\overline{\text{CAS}}$  Control for Nine Common Data-In and Data-Out Lines, in Four Blocks

- Enhanced Page Mode Operation With  $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  (CBR),  $\overline{\text{RAS}}$ -Only, and Hidden Refresh

- Presence Detect

- Performance Ranges:

	ACCESS TIME	ACCESS TIME	ACCESS TIME	READ OR WRITE CYCLE
	t <sub>RAC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>	
	(MAX)	(MAX)	(MAX)	(MIN)
'124MBK36C-60	60 ns	30 ns	15 ns	110 ns
'124MBK36C-70	70 ns	35 ns	18 ns	130 ns
'124MBK36C-80	80 ns	40 ns	20 ns	150 ns
'248NBK36C-60	60 ns	30 ns	15 ns	110 ns
'248NBK36C-70	70 ns	35 ns	18 ns	130 ns
'248NBK36C-80	80 ns	40 ns	20 ns	150 ns

- Low Power Dissipation
- Operating Free-Air-Temperature Range  
 0°C to 70°C
- Gold-Tabbed Versions Available:†
  - TM124MBK36C
  - TM248NBK36C
- Tin-Lead (Solder) Tabbed Versions
  - TM124MBK36S
  - TM248NBK36S

## description

### TM124MBK36C

The TM124MBK36C is a dynamic random-access memory (DRAM) organized as four times 1048576 × 9 (bit 9 is generally used for parity) in a 72-pin leadless single in-line memory module (SIMM). The SIMM is composed of eight TMS44400DJ, 1 048 576 × 4-bit DRAMs, each in 20/26-lead plastic small-outline J-lead packages (SOJs), and two TMS44460DJ, 1 048 576 × 4-bit Quad-CAS DRAMs, in 24/26-lead plastic SOJs mounted on a substrate with decoupling capacitors. Each TMS44400DJ and TMS44460DJ is described in the TMS44400 and TMS44460 data sheets, respectively.

The TM124MBK36C is available in the single-sided BK leadless module for use with sockets.

The TM124MBK36C features  $\overline{\text{RAS}}$  access times of 60 ns, 70 ns, and 80 ns. This device is characterized for operation from 0°C to 70°C.

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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## TM248NBK36C

The TM248NBK36C is a DRAM organized as four times  $2\ 097\ 152 \times 9$  (bit 9 is generally used for parity) in a 72-pin leadless SIMM) The SIMM is composed of sixteen TMS44400DJ,  $1\ 048\ 576 \times 4$ -bit DRAMs, each in 20/26-lead plastic SOJs, and four TMS44460DJ,  $1\ 048\ 576 \times 4$ -bit Quad-CAS DRAMs, in 24/26-lead plastic SOJs mounted on a substrate with decoupling capacitors. Each TMS44400DJ and TMS44460DJ is described in the TMS44400 or TMS44460 data sheet, respectively.

The TM248NBK36C is available in the double-sided BK leadless module for use with sockets.

The TM248NBK36C features  $\overline{\text{RAS}}$  access times of 60 ns, 70 ns, and 80 ns. This device is rated for operation from 0°C to 70°C.

## operation

### TM124MBK36C

The TM124MBK36C operates as eight TMS44400DJs and two TMS44460DJs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

### TM248NBK36C

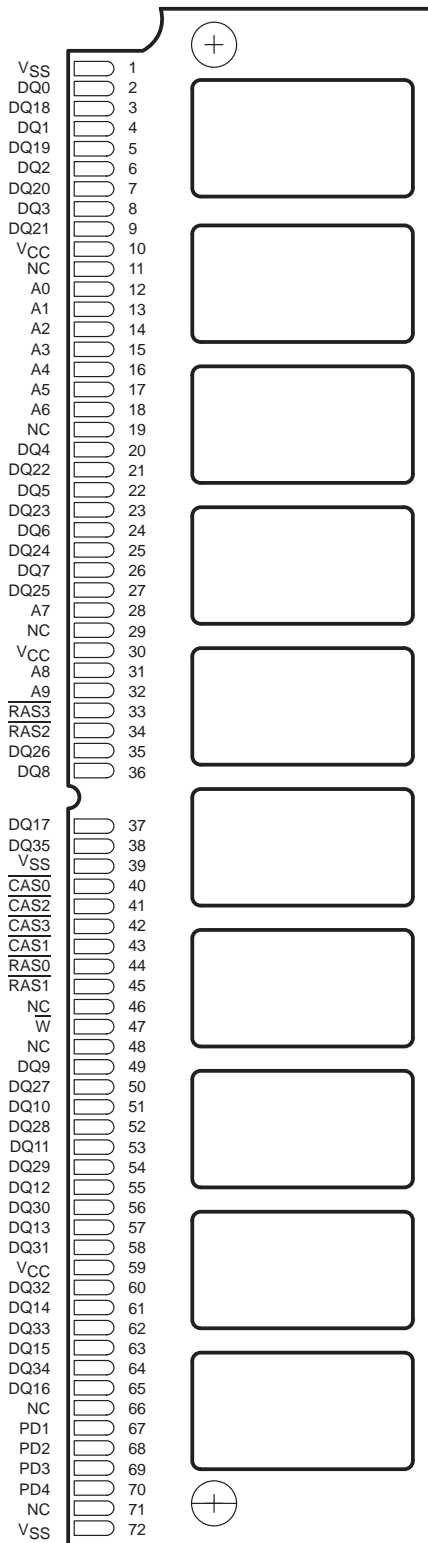
The TM248NBK36C operates as sixteen TMS44400DJs and four TMS44460DJs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.



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BK SINGLE IN-LINE MODULE  
 (TOP VIEW)



TM124MBK36C  
 (SIDE VIEW)



TM248NBK36C  
 (SIDE VIEW)



PIN NOMENCLATURE

A0–A9	Address Inputs
CAS0–CAS3	Column-Address Strobe
DQ0–DQ35	Data In/Data Out
NC	No Connection
PD1–PD4	Presence Detects
RAS0–RAS3	Row-Address Strobe
VCC	5-V Supply
VSS	Ground
W	Write Enable

PRESENCE DETECT

		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124MBK36C	80 ns	VSS	VSS	NC	VSS
	70 ns	VSS	VSS	VSS	NC
	60 ns	VSS	VSS	NC	NC
TM248NBK36C	80 ns	NC	NC	NC	VSS
	70 ns	NC	NC	VSS	NC
	60 ns	NC	NC	NC	NC

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**Table 1. Connection Table**

DATA BLOCK	RASx		CASx
	SIDE 1	SIDE 2†	
DQ0–DQ7 DQ8	RAS0 RAS0	RAS1 RAS1	CAS0 CAS0
DQ9–DQ16 DQ17	RAS0 RAS0	RAS1 RAS1	CAS1 CAS1
DQ18–DQ25 DQ26	RAS2 RAS2	RAS3 RAS3	CAS2 CAS2
DQ27–DQ34 DQ35	RAS2 RAS2	RAS3 RAS3	CAS3 CAS3

† Side 2 applies to the TM248NBK36C only.

**single-in-line memory module and components**

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage

Bypass capacitors: Multilayer ceramic

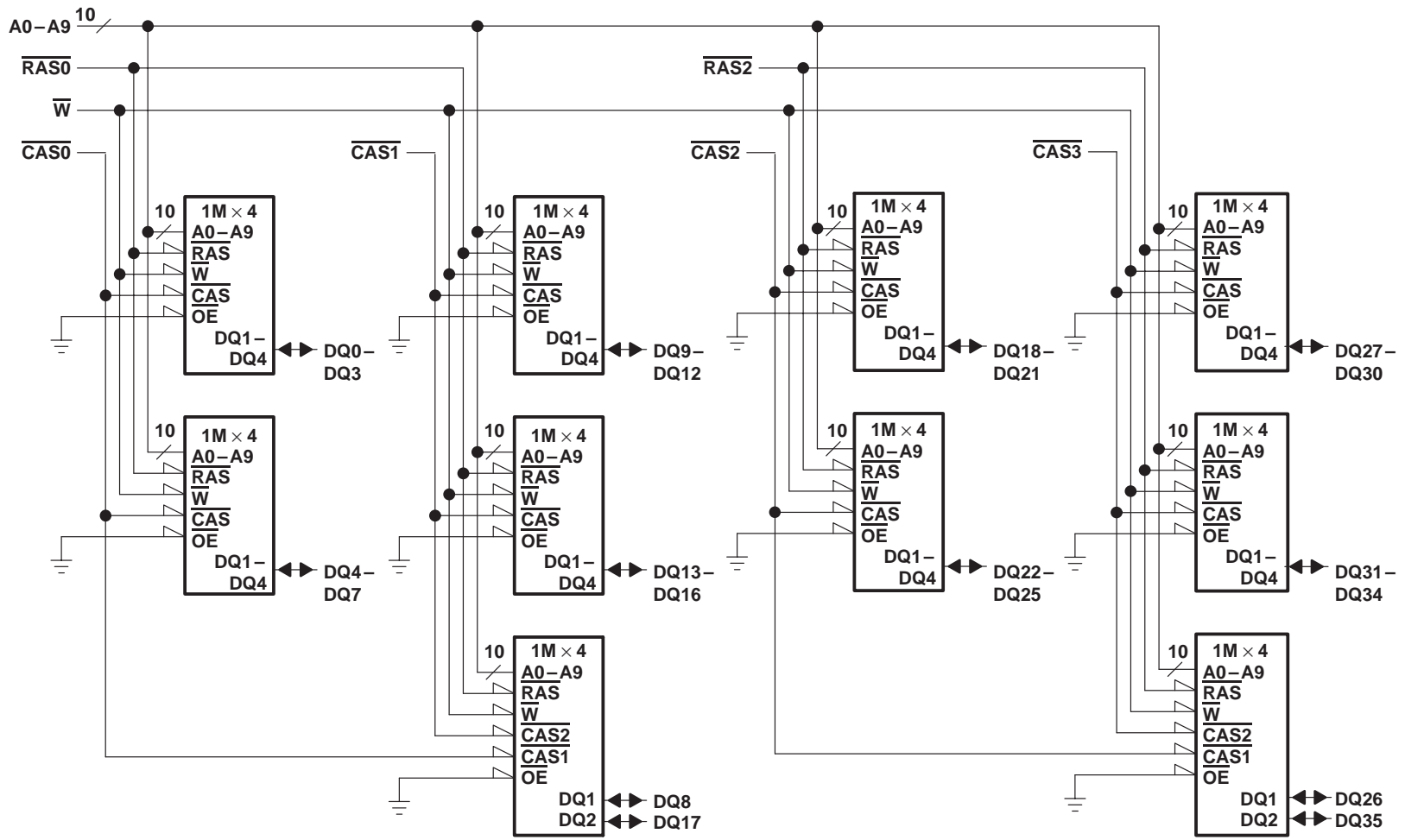
Contact area for TM124MBK36C and TM248NBK36C: Nickel plate and gold plate over copper

Contact area for TM124MBK36S and TM248NBK36S: Nickel plate and tin-lead over copper



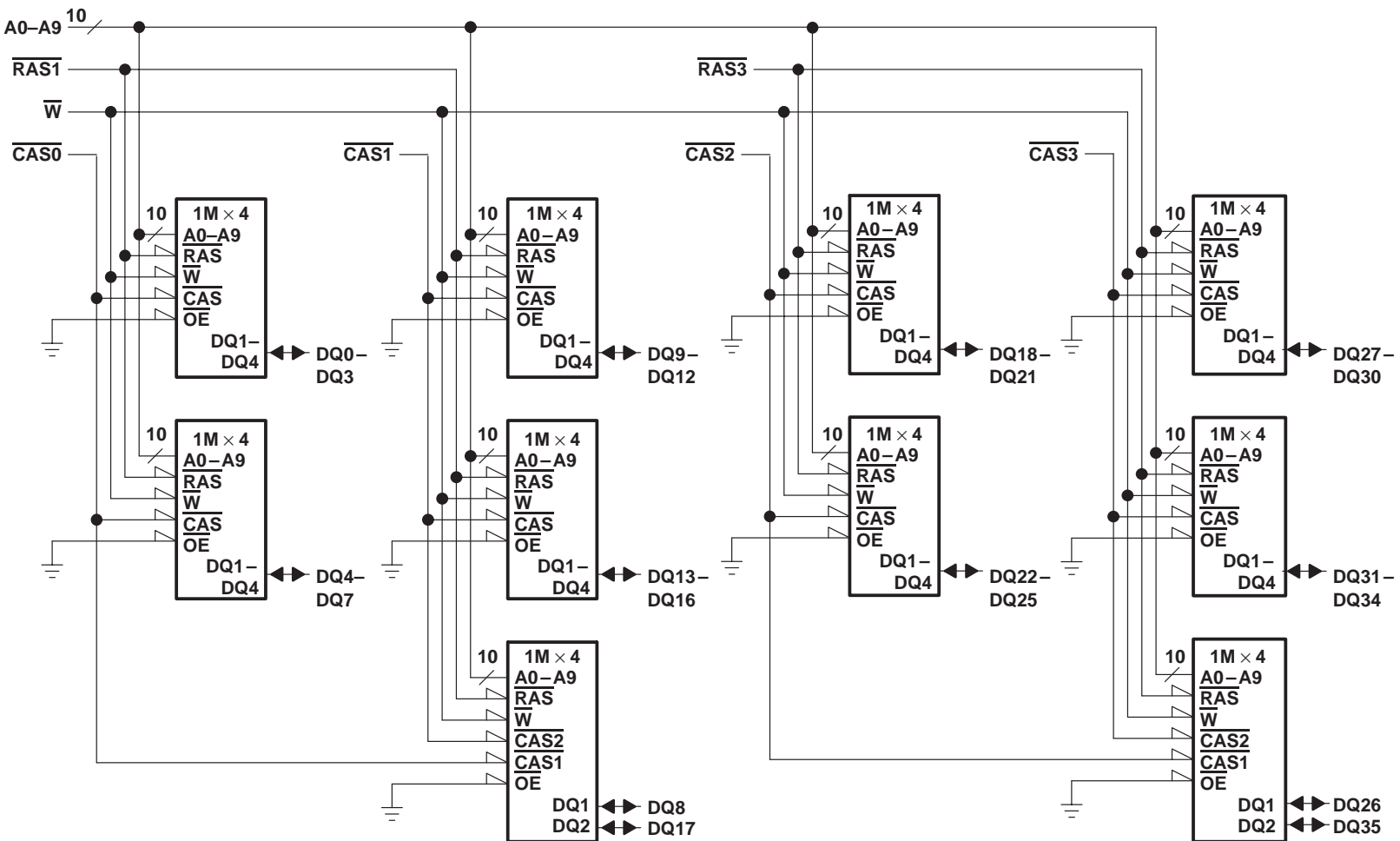
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functional block diagram (for TM124MBK36C and TM248NBK36C, Side 1)



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TM248NBK36C, TM248NBK36S 2097152 BY 36-BIT  
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functional block diagram (for TM248NBK36C, Side 2)



**TM124MBK36C, TM124MBK36S 1048576 BY 36-BIT  
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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range on $V_{CC}$ (see Note 1)	– 1 V to 7 V
Supply voltage range on any pin (see Note 1)	– 1 V to 7 V
Short-circuit output current	50 mA
Power dissipation	10 W
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	– 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to  $V_{SS}$ .

**recommended operating conditions**

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2.4		6.5	V
$V_{IL}$ Low-level input voltage (see Note 2)	– 1		0.8	V
$T_A$ Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	'124MBK36C-60		'124MBK36C-70		'124MBK36C-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$ High-level output voltage	$I_{OH} = -5$ mA	2.4		2.4		2.4		V
$V_{OL}$ Low-level output voltage	$I_{OL} = 4.2$ mA		0.4		0.4		0.4	V
$I_I$ Input current (leakage)	$V_{CC} = 5.5$ V, $V_I = 0$ V to 6.5 V, All other pins = 0 V to $V_{CC}$		± 10		± 10		± 10	µA
$I_O$ Output current (leakage)	$V_{CC} = 5.5$ V, $V_O = 0$ V to $V_{CC}$ , CAS high		± 10		± 10		± 10	µA
$I_{CC1}$ Read- or write-cycle current (see Note 3)	$V_{CC} = 5.5$ V, Minimum cycle		1050		900		800	mA
$I_{CC2}$ Standby current	$V_{IH} = 2.4$ V (TTL), after 1 memory cycle, RAS and CAS high		20		20		20	mA
	$V_{IH} = V_{CC} - 0.2$ V (CMOS), after 1 memory cycle, RAS and CAS high		10		10		10	mA
$I_{CC3}$ Average refresh current (RAS only or CBR) (see Note 3)	$V_{CC} = 5.5$ V, Minimum cycle, RAS cycling, CAS high (RAS only), RAS low after CAS low (CBR)		1050		900		800	mA
$I_{CC4}$ Average page current (see Note 4)	$V_{CC} = 5.5$ V, $t_{PC} =$ Minimum, RAS low, CAS cycling		900		800		700	mA

NOTES: 3. Measured with a maximum of one address change while  $\overline{RAS} = V_{IL}$   
4. Measured with a maximum of one address change while  $CAS = V_{IH}$



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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	'248NBK36C-60		'248NBK36C-70		'248NBK36C-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -5 mA		2.4		2.4		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4.2 mA		0.4		0.4		V
I <sub>I</sub>	Input current (leakage)	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0 V to 6.5 V, All other pins = 0 V to V <sub>CC</sub>		± 20		± 20		µA
I <sub>O</sub>	Output current (leakage)	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V to V <sub>CC</sub> , CAS high		± 20		± 20		µA
I <sub>CC1</sub>	Read or write cycle current (see Note 3)	V <sub>CC</sub> = 5.5 V, Minimum cycle		1070		920		mA
I <sub>CC2</sub>	Standby current	V <sub>IH</sub> = 2.4 V (TTL), after 1 memory cycle, RAS and CAS high		40		40		mA
		V <sub>IH</sub> = V <sub>CC</sub> - 0.2 V (CMOS), after 1 memory cycle, RAS and CAS high		20		20		mA
I <sub>CC3</sub>	Average refresh current (RAS only or CBR) (see Note 3)	V <sub>CC</sub> = 5.5 V, Minimum cycle, RAS cycling, CAS high (RAS only), RAS low after CAS low (CBR)		2100		1800		mA
I <sub>CC4</sub>	Average page current (see Note 4)	V <sub>CC</sub> = 5.5 V, t <sub>PC</sub> = Minimum, RAS low, CAS cycling		920		820		mA

NOTES: 3. Measured with a maximum of one address change while  $\overline{\text{RAS}} = V_{IL}$   
4. Measured with a maximum of one address change while  $\text{CAS} = V_{IH}$

**capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)**

PARAMETER	'124MBK36C		'248NBK36C		UNIT	
	MIN	MAX	MIN	MAX		
C <sub>i(A)</sub>	Input capacitance, A0–A9		50		100	pF
C <sub>i(R)</sub>	Input capacitance, $\overline{\text{RAS}}$ inputs		35		35	pF
C <sub>i(C)</sub>	Input capacitance, $\overline{\text{CAS}}$ inputs		21		42	pF
C <sub>i(W)</sub>	Input capacitance, $\overline{\text{W}}$		70		140	pF
C <sub>o(DQ)</sub>	Output capacitance on DQ pins		7		14	pF

NOTE 5: V<sub>CC</sub> equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.



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**switching characteristics over recommended ranges of supply voltage and operating free-air temperature**

PARAMETER	'124MBK36C-60 '248NBK36C-60		'124MBK36C-70 '248NBK36C-70		'124MBK36C-80 '248NBK36C-80		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>CAC</sub> Access time from $\overline{\text{CAS}}$ low	15		18		20		ns
t <sub>AA</sub> Access time from column-address	30		35		40		ns
t <sub>RAC</sub> Access time from $\overline{\text{RAS}}$ low	60		70		80		ns
t <sub>CPA</sub> Access time from column precharge	35		40		45		ns
t <sub>CLZ</sub> $\overline{\text{CAS}}$ to output in low Z	0		0		0		ns
t <sub>OFF</sub> Output disable time after $\overline{\text{CAS}}$ high (see Note 6)	0 15		0 18		0 20		ns

NOTE 6: t<sub>OFF</sub> is specified when the output is no longer driven.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature**

	'124MBK36C-60 '248NBK36C-60		'124MBK36C-70 '248NBK36C-70		'124MBK36C-80 '248NBK36C-80		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>RC</sub> Cycle time, random read or write (see Note 7)	110		130		150		ns
t <sub>RWC</sub> Cycle time, read-write	130		153		175		ns
t <sub>PC</sub> Cycle time, page-mode read or write (see Note 8)	40		45		50		ns
t <sub>RASP</sub> Pulse duration, page mode, $\overline{\text{RAS}}$ low	60	100 000	70	100 000	80	100 000	ns
t <sub>RAS</sub> Pulse duration, nonpage mode, $\overline{\text{RAS}}$ low	60	10 000	70	10 000	80	10 000	ns
t <sub>CAS</sub> Pulse duration, $\overline{\text{CAS}}$ low	15	10 000	18	10 000	20	10 000	ns
t <sub>CP</sub> Pulse duration, $\overline{\text{CAS}}$ high	10		10		10		ns
t <sub>RP</sub> Pulse duration, $\overline{\text{RAS}}$ high (precharge)	40		50		60		ns
t <sub>WP</sub> Pulse duration, write	15		15		15		ns
t <sub>ASC</sub> Setup time, column address before $\overline{\text{CAS}}$ low	0		0		0		ns
t <sub>ASR</sub> Setup time, row address before $\overline{\text{RAS}}$ low	0		0		0		ns
t <sub>DS</sub> Setup time, data	0		0		0		ns
t <sub>RCS</sub> Setup time, read before $\overline{\text{CAS}}$ low	0		0		0		ns
t <sub>CWL</sub> Setup time, $\overline{\text{W}}$ time before $\overline{\text{CAS}}$ high	15		18		20		ns
t <sub>RWL</sub> Setup time, $\overline{\text{W}}$ low before $\overline{\text{RAS}}$ high	15		18		20		ns
t <sub>WCS</sub> Setup time, $\overline{\text{W}}$ low before $\overline{\text{CAS}}$ low	0		0		0		ns
t <sub>WSR</sub> Setup time, $\overline{\text{W}}$ high (CBR refresh only)	10		10		10		ns
t <sub>CAH</sub> Hold time, column address after $\overline{\text{CAS}}$ low	10		15		15		ns
t <sub>DHR</sub> Hold time, data after $\overline{\text{RAS}}$ low (see Note 9)	50		55		60		ns
t <sub>DH</sub> Hold time, data	10		15		15		ns
t <sub>AR</sub> Hold time, column address after $\overline{\text{RAS}}$ low (see Note 99)	50		55		60		ns
t <sub>CLCH</sub> Hold time, $\overline{\text{CAS}}$ low to $\overline{\text{CAS}}$ high	5		5		5		ns
t <sub>RAH</sub> Hold time, row address after $\overline{\text{RAS}}$ low	10		10		10		ns
t <sub>RCH</sub> Hold time, read after $\overline{\text{CAS}}$ high (see Note 10)	0		0		0		ns
t <sub>RRH</sub> Hold time, read after $\overline{\text{RAS}}$ high (see Note 10)	0		0		0		ns

NOTES: 7. All cycles assume t<sub>T</sub> = 5 ns.

8. To assure t<sub>PC</sub> min, t<sub>ASC</sub> should be ≥ 5 ns.

9. The minimum value is measured when t<sub>RCD</sub> is set to t<sub>RCD</sub> min as a reference.

10. Either t<sub>RRH</sub> or t<sub>RCH</sub> must be satisfied for a read cycle.



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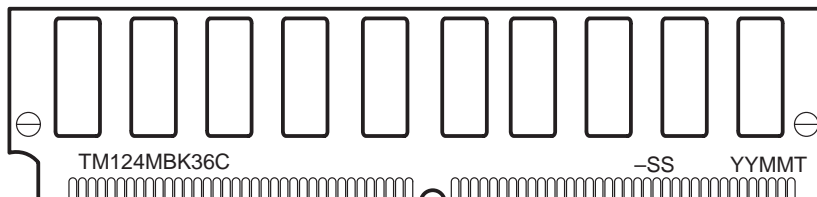
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**timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)**

		'124MBK36C-60 '248NBK36C-60		'124MBK36C-70 '248NBK36C-70		'124MBK36C-80 '248NBK36C-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>WCH</sub>	Hold time, write after $\overline{\text{CAS}}$ low	15		15		15		ns
t <sub>WCR</sub>	Hold time, write after $\overline{\text{RAS}}$ low (see Note 9)	50		55		60		ns
t <sub>WHR</sub>	Hold time, $\overline{\text{W}}$ high (CBR refresh only)	10		10		10		ns
t <sub>CHR</sub>	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high (CBR refresh only)	15		15		20		ns
t <sub>CRP</sub>	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	0		0		0		ns
t <sub>CSH</sub>	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high	60		70		80		ns
t <sub>CSR</sub>	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ low (CBR refresh only)	10		10		10		ns
t <sub>RAD</sub>	Delay time, $\overline{\text{RAS}}$ low to column address (see Note 11)	15	30	15	35	15	40	ns
t <sub>RAL</sub>	Delay time, column address to $\overline{\text{RAS}}$ high	30		35		40		ns
t <sub>CAL</sub>	Delay time, column address to $\overline{\text{CAS}}$ high	30		35		40		ns
t <sub>RCD</sub>	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (see Note 11)	20	45	20	52	20	60	ns
t <sub>RPC</sub>	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low (CBR refresh only)	0		0		0		ns
t <sub>RSH</sub>	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ high	15		18		20		ns
t <sub>REF</sub>	Refresh time interval		16		16		16	ms
t <sub>T</sub>	Transition time	2	50	2	50	2	50	ns

- NOTES: 9. The minimum value is measured when t<sub>RCD</sub> is set to t<sub>RCD</sub> min as a reference.  
 10. Either t<sub>RRH</sub> or t<sub>RCH</sub> must be satisfied for a read cycle.  
 11. The maximum value is specified only to assure access time.

**device symbolization (TM124MBK36C illustrated)**



- YY = Year Code
- MM = Month Code
- T = Assembly Site Code
- SS = Speed Code

NOTE: Location of symbolization may vary.



## IMPORTANT NOTICE

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