

TM124MBK36F, TM124MBK36U 1048576 BY 36-BIT DRAM MODULE TM248NBK36F, TM248NBK36U 2097152 BY 36-BIT DRAM MODULE

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- **Organization**
TM124MBK36F . . . 1 048 576 × 36
TM248NBK36F . . . 2 097 152 × 36
- **Single 5-V Power Supply ($\pm 10\%$ Tolerance)**
- **72-Pin Single-In-Line Memory Module (SIMM) for Use With Socket**
- **TM124MBK36F – Utilizes Two 16-Megabit and One 4-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM248NBK36F – Utilizes Four 16-Megabit and Two 4-Megabit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **Long Refresh Period . . . 16 ms (1024 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{\text{CAS}}$ Control for Nine Common Data-In and Data-Out Lines in Four Blocks**
- **Enhanced Page-Mode Operation With CAS-Before-RAS (CBR), RAS-Only, and Hidden Refresh**

- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	READ OR WRITE CYCLE (MIN)
'124MBK36F-60	60 ns	30 ns	15 ns	110 ns
'124MBK36F-70	70 ns	35 ns	18 ns	130 ns
'124MBK36F-80	80 ns	40 ns	20 ns	150 ns
'248NBK36F-60	60 ns	30 ns	15 ns	110 ns
'248NBK36F-70	70 ns	35 ns	18 ns	130 ns
'248NBK36F-80	80 ns	40 ns	20 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range:**
0°C to 70°C
- **Gold-Tabbed Versions Available:[†]**
 - TM124MBK36F
 - TM248NBK36F
- **Tin-Lead (Solder) Tabbed Versions Available:**
 - TM124MBK36U
 - TM248NBK36U

description

TM124MBK36F

The TM124MBK36F is a 4-MByte dynamic random-access memory (DRAM) organized as four times 1048576 × 9 in a 72-pin single-in-line memory module (SIMM). The SIMM is composed of two TMS418160DZ, 1 048 576 × 16-bit dynamic RAMs, each in a 42-lead plastic small-outline J-lead (SOJ) package and one TMS44460DJ, 1048576 × 4-bit DRAM in a 24/26-lead plastic small-outline J-lead (SOJ) package mounted on a substrate with decoupling capacitors. The TMS418160DZ and TMS44460DJ are described in the TMS418160 and TMS44460 data sheets, respectively. The TM124MBK36F SIMM is available in the single-sided BK leadless module for use with sockets.

TM248NBK36F

The TM248NBK36F is an 8-MByte DRAM organized as four times 2097152 × 9 in a 72-pin single-in-line memory module (SIMM). The SIMM is composed of four TMS418160DZ, 1 048 576 × 16-bit dynamic RAMs, each in a 42-lead plastic small-outline J-lead (SOJ) package and two TMS44460DJ, 1048576 × 4-bit DRAMs, each in a 24/26-lead plastic small-outline (SOJ) package mounted on a substrate with decoupling capacitors. The TMS418160DZ and TMS44460DJ are described in the TMS418160 and TMS44460 data sheets, respectively. The TM248NBK36F SIMM is available in the double-sided BK leadless module for use with sockets.

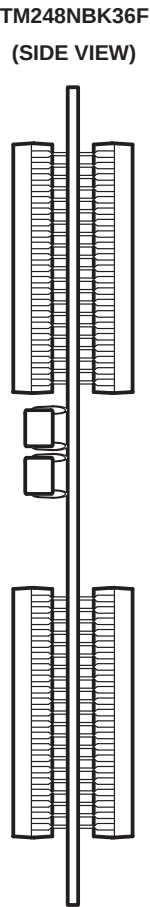
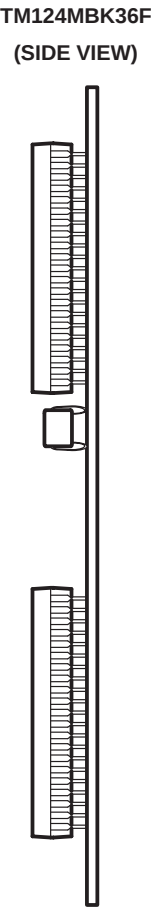
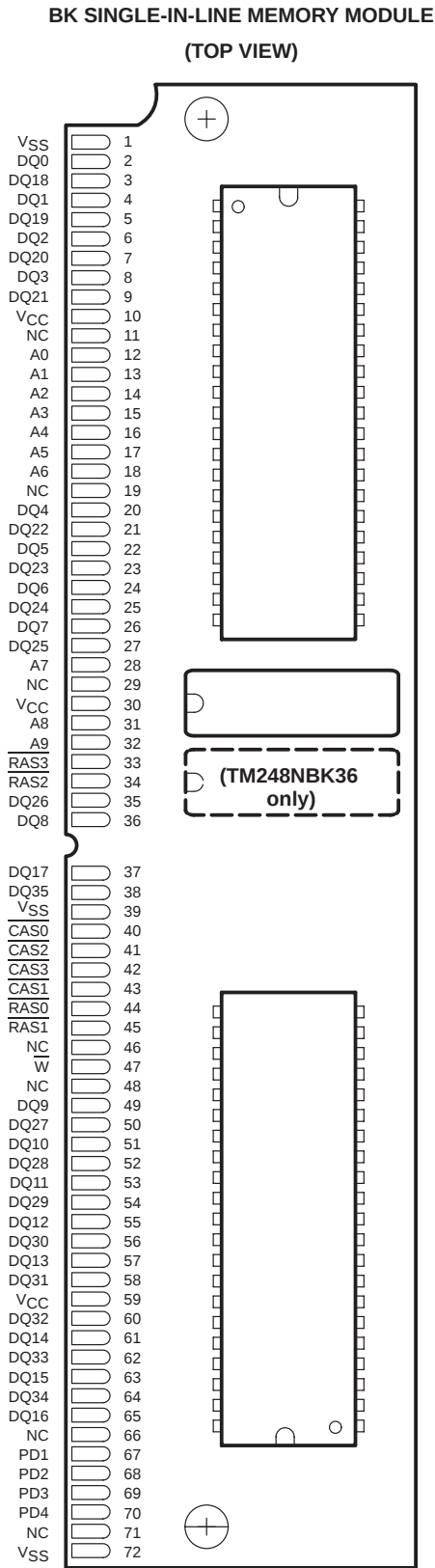
operation

The TM124MBK36F operates as two TMS418160DZs and one TMS44460DJ connected as shown in the functional block diagram and NO TAG. The TM248NBK36F operates as four TMS418160DZs and two TMS44460DJs connected as shown in the functional block diagram and NO TAG. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

[†] Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

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PIN NOMENCLATURE	
A0–A9	Address Inputs
CAS0–CAS3	Column-Address Strobe
DQ0–DQ35	Data In/Data Out
NC	No Connection
PD1–PD4	Presence Detects
RAS0–RAS3	Row-Address Strobe
VCC	5-V Supply
VSS	Ground
W	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124MBK36F	80 ns	VSS	VSS	NC	VSS
	70 ns	VSS	VSS	VSS	NC
	60 ns	VSS	VSS	NC	NC
TM248NBK36F	80 ns	NC	NC	NC	VSS
	70 ns	NC	NC	VSS	NC
	60 ns	NC	NC	NC	NC

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Table 1. Connection Table

DATA BLOCK	RASx		CASx
	SIDE 1	SIDE 2†	
DQ0–DQ7 DQ8	RAS0 RAS2	RAS1 RAS3	CAS0 CAS0
DQ9–DQ16 DQ17	RAS0 RAS2	RAS1 RAS3	CAS1 CAS1
DQ18–DQ25 DQ26	RAS2 RAS2	RAS3 RAS3	CAS2 CAS2
DQ27–DQ34 DQ35	RAS2 RAS2	RAS3 RAS3	CAS3 CAS3

† Side 2 applies to the TM248NBK36F only.

single in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage

Bypass capacitors: Multilayer ceramic

Contact area for TM124MBK36F and TM248NBK36F: Nickel plate and gold plate over copper

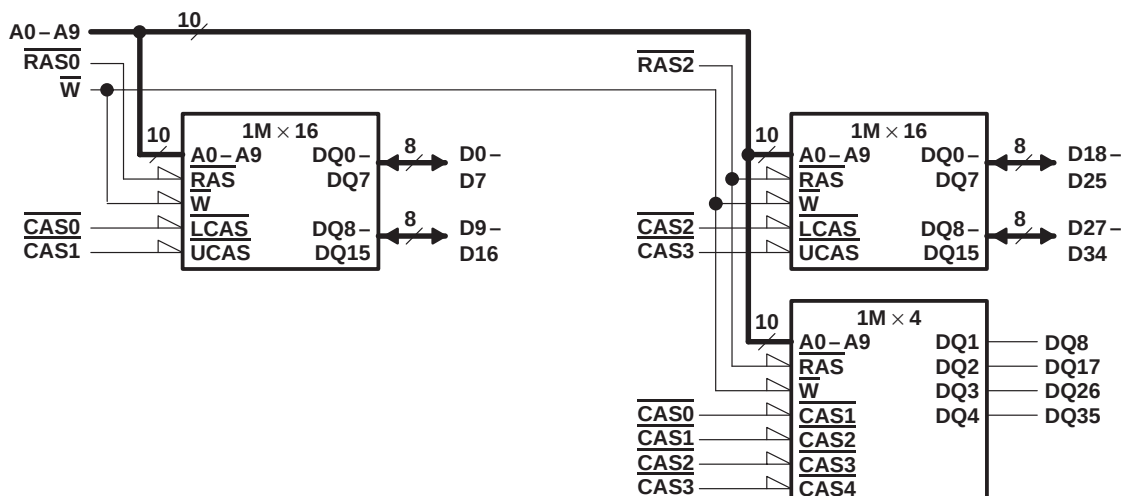
Contact area for TM124MBK36U and TM248NBK36U: Nickel plate and tin/lead over copper



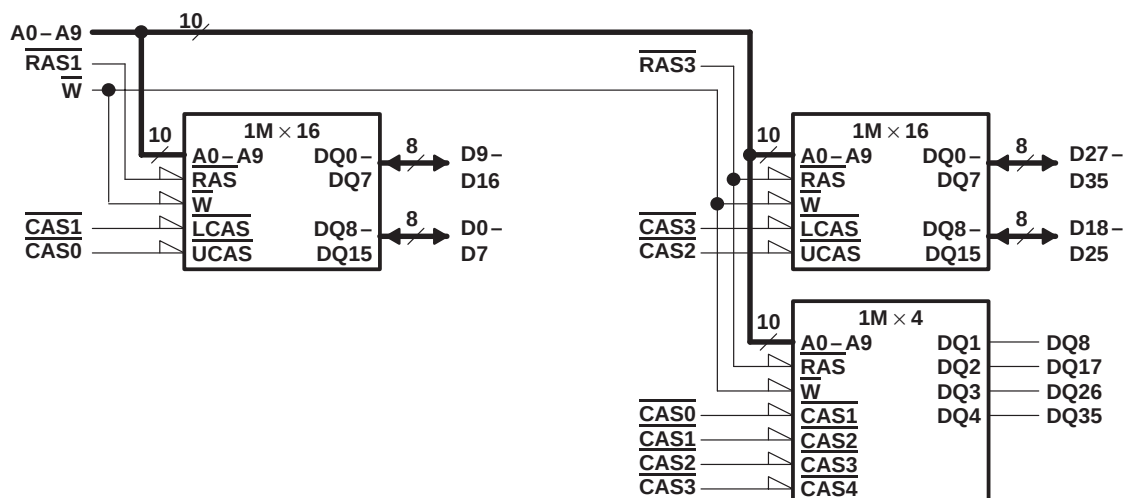
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functional block diagram [TM124MBK36F and TM248NBK36F, side 1]



functional block diagram [TM248NBK36F, side 2]



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	– 1 V to 7 V
Voltage range on any pin (see Note 1)	– 1 V to 7 V
Short-circuit output current	50 mA
Power dissipation TM124MBK36F, TM124MBK36U	3 W
TM248NBK36F, TM248NBK36U	6 W
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	– 55°C to 125°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} .

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2.4		6.5	V
V_{IL} Low-level input voltage (see Note 2)	– 1		0.8	V
T_A Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	'124MBK36F - 60		'124MBK36F - 70		'124MBK36F - 80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH} High-level output voltage	$I_{OH} = -5$ mA	2.4		2.4		2.4		V
V_{OL} Low-level output voltage	$I_{OL} = 4.2$ mA		0.4		0.4		0.4	V
I_I Input current (leakage)	$V_{CC} = 5.5$ V, $V_I = 0$ V to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O Output current (leakage)	$V_{CC} = 5.5$ V, $V_O = 0$ V to V_{CC} , CAS high		± 10		± 10		± 10	µA
I_{CC1} Read- or write-cycle current	$V_{CC} = 5.5$ V, Minimum cycle		285		250		220	mA
I_{CC2} Standby current	$V_{IH} = 2.4$ V (TTL), After 1 memory cycle, RAS and CAS high		6		6		6	mA
	$V_{IH} = V_{CC} - 0.2$ V (CMOS), After 1 memory cycle, RAS and CAS high		3		3		3	mA
I_{CC3} Average refresh current (RAS only or CBR)	$V_{CC} = 5.5$ V, Minimum cycle, RAS cycling, CAS high (RAS only); RAS low after CAS low (CBR)		285		250		220	mA
I_{CC4} Average page current	$V_{CC} = 5.5$ V, $t_{PC} = \text{MIN}$, RAS low, CAS cycling		250		220		190	mA



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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[†]

PARAMETER	TEST CONDITIONS	'248NBK36F - 60		'248NBK36F - 70		'248NBK36F - 80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH} High-level output voltage	I _{OH} = – 5 mA	2.4		2.4		2.4		V
V _{OL} Low-level output voltage	I _{OL} = 4.2 mA		0.4		0.4		0.4	V
I _I Input current (leakage)	V _{CC} = 5.5 V, V _I = 0 V to 6.5 V, All other pins = 0 V to V _{CC}		± 10		± 10		± 10	µA
I _O Output current (leakage)	V _{CC} = 5.5 V, V _O = 0 V to V _{CC} , $\overline{\text{CAS}}$ high		± 20		± 20		± 20	µA
I _{CC1} Read- or write-cycle current (see Note 3)	V _{CC} = 5.5 V, Minimum cycle		391		256		226	mA
I _{CC2} Standby current	V _{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high		12		12		12	mA
	V _{IH} = V _{CC} – 0.2 V (CMOS), After 1 memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high		6		6		6	mA
I _{CC3} Average refresh current ($\overline{\text{RAS}}$ only or CBR) (see Note 3)	V _{CC} = 5.5 V, Minimum cycle, $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ high ($\overline{\text{RAS}}$ only); $\overline{\text{RAS}}$ low after $\overline{\text{CAS}}$ low (CBR)		570		500		440	mA
I _{CC4} Average page current (see Note 4)	V _{CC} = 5.5 V, t _{PC} = MIN, $\overline{\text{RAS}}$ low, $\overline{\text{CAS}}$ cycling		256		226		196	mA

[†] For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Measured with a maximum of one address change while $\overline{\text{RAS}}$ = V_{IL}

4. Measured with a maximum of one address change while $\overline{\text{CAS}}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		'124MBK36F		'248NBK36F		UNIT
		MIN	MAX	MIN	MAX	
C _{i(A)}	Input capacitance, address inputs		15		30	pF
C _{i(R)}	Input capacitance, $\overline{\text{RAS}}$ inputs	$\overline{\text{RAS2}}, \overline{\text{RAS3}}$	14		14	pF
		$\overline{\text{RAS0}}, \overline{\text{RAS1}}$	7		7	
C _{i(C)}	Input capacitance, $\overline{\text{CAS}}$ inputs		14		28	pF
C _{i(W)}	Input capacitance, write-enable input		21		42	pF
C _{o(DQ)}	Output capacitance on DQ pins		7		14	pF

NOTE 5: Bias on pins under test is 0 V.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	'124MBK36F - 60 '248NBK36F - 60		'124MBK36F - 70 '248NBK36F - 70		'124MBK36F - 80 '248NBK36F - 80		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{AA} Access time from column address		30		35		40	ns
t _{CAC} Access time from $\overline{\text{CAS}}$ low		15		18		20	ns
t _{RAC} Access time from $\overline{\text{RAS}}$ low		60		70		80	ns
t _{CPA} Access time from column precharge		35		40		45	ns
t _{CLZ} $\overline{\text{CAS}}$ to output in low-impedance state	0		0		0		ns
t _{OH} Output disable time from start of $\overline{\text{CAS}}$ high	3		3		3		ns
t _{OFF} Output disable time after $\overline{\text{CAS}}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

	'124MBK36F - 60 '248NBK36F - 60		'124MBK36F - 70 '248NBK36F - 70		'124MBK36F - 80 '248NBK36F - 80		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{RC} Cycle time, random read or write (see Note 7)	110		130		150		ns
t _{PC} Cycle time, page-mode read or write (see Notes 7 and 8)	40		45		50		ns
t _{RASP} Pulse duration, page mode, $\overline{\text{RAS}}$ low	60	100 000	70	100 000	80	100 000	ns
t _{RAS} Pulse duration, nonpage mode, $\overline{\text{RAS}}$ low	60	10 000	70	10 000	80	10 000	ns
t _{CAS} Pulse duration, $\overline{\text{CAS}}$ low	15	10 000	18	10 000	20	10 000	ns
t _{CP} Pulse duration, $\overline{\text{CAS}}$ high (precharge)	10		10		10		ns
t _{RP} Pulse duration, $\overline{\text{RAS}}$ high (precharge)	40		50		60		ns
t _{WP} Pulse duration, $\overline{\text{W}}$ low	10		10		10		ns
t _{ASC} Setup time, column address before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{ASR} Setup time, row address before $\overline{\text{RAS}}$ low	0		0		0		ns
t _{DS} Setup time, data before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{RCS} Setup time, $\overline{\text{W}}$ high before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{CWL} Setup time, $\overline{\text{W}}$ low before $\overline{\text{CAS}}$ high	15		18		20		ns
t _{RWL} Setup time, $\overline{\text{W}}$ low before $\overline{\text{RAS}}$ high	15		18		20		ns
t _{WCS} Setup time, $\overline{\text{W}}$ low before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{WRP} Setup time, $\overline{\text{W}}$ high before $\overline{\text{RAS}}$ low (CBR refresh only)	10		10		10		ns
t _{CAH} Hold time, column address after $\overline{\text{CAS}}$ low	10		15		15		ns
t _{RHCP} Hold time, $\overline{\text{RAS}}$ high from $\overline{\text{CAS}}$ precharge	35		40		45		ns
t _{DH} Hold time, data after $\overline{\text{CAS}}$ low	10		15		15		ns
t _{RAH} Hold time, row address after $\overline{\text{RAS}}$ low	10		10		10		ns
t _{RCH} Hold time, $\overline{\text{W}}$ high after $\overline{\text{CAS}}$ high (see Note 9)	0		0		0		ns
t _{RRH} Hold time, $\overline{\text{W}}$ high after $\overline{\text{RAS}}$ high (see Note 9)	0		0		0		ns
t _{WCH} Hold time, $\overline{\text{W}}$ low after $\overline{\text{CAS}}$ low	10		15		15		ns
t _{WRH} Hold time, $\overline{\text{W}}$ high after $\overline{\text{RAS}}$ low (CBR refresh only)	10		10		10		ns

- NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.



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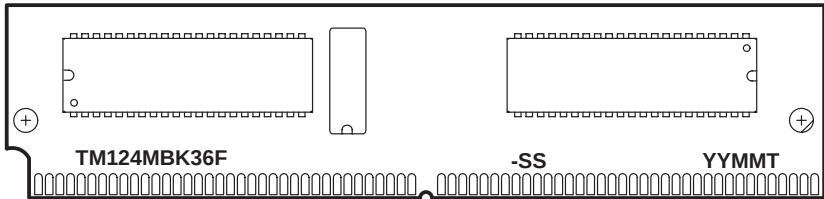
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timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		'124MBK36F-60 '248NBK36F-60		'124MBK36F-70 '248NBK36F-70		'124MBK36F-80 '248NBK36F-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{CHR}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high (CBR refresh only)	10		10		10		ns
t _{CRP}	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	5		5		5		ns
t _{CSH}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high	60		70		80		ns
t _{CSR}	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ low (CBR refresh only)	5		5		5		ns
t _{RAD}	Delay time, $\overline{\text{RAS}}$ low to column address (see Note 10)	15	30	15	35	15	40	ns
t _{RAL}	Delay time, column address to $\overline{\text{RAS}}$ high	30		35		40		ns
t _{CAL}	Delay time, column address to $\overline{\text{CAS}}$ high	30		35		40		ns
t _{RCD}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (see Note 10)	20	45	20	52	20	60	ns
t _{RPC}	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low (CBR only)	0		0		0		ns
t _{RSH}	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ high	15		18		20		ns
t _{REF}	Refresh time interval		16		16		16	ms
t _T	Transition time	3	30	3	30	3	30	ns

NOTE 10: The maximum value is specified only to assure access time.

device symbolization (TM124MBK36F illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE: Location of symbolization may vary.

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