TM124FBK32F, TM124FBK32U 1048576 BY 32-BIT DYNAMIC RAM MODULE
TM248GBK32F, TM248GBK32U 2097152 BY 32-BIT DYNAMIC RAM MODULE

- **Organization**
  TM124FBK32F . . . 1 048 576 × 32
  TM248GBK32F . . . 2 097 152 × 32
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-Pin Single In-Line Memory Module (SIMM) for Use With Socket**
- **TM124FBK32F – Utilizes Two 16M-Bit Dynamic Random-Access Memories (DRAMs) in Plastic Small-Outline J-Lead (SOJ) Package**
- **TM248GBK32F – Utilizes Four 16M-Bit DRAMs in Plastic SOJ Package**
- **Long Refresh Period**
  16 ms (1024 Cycles)
- **All Inputs, Outputs, Clocks Fully TTL-Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines in Four Blocks**
- **Extended Data Out (EDO) Operation With $\overline{CAS}$-Before-$\overline{RAS}$ (CBR), $\overline{RAS}$-Only, Hidden Refresh, and Self Refresh**
- **Presence Detect**
- **JEDEC First Generation 72-Pin SIMM Pinout**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	EDO CYCLE t_{HPC} (MIN)
’124FBK32F-60	60 ns	30 ns	15 ns	25 ns
’124FBK32F-70	70 ns	35 ns	18 ns	30 ns
’124FBK32F-80	80 ns	40 ns	20 ns	35 ns
’248GBK32F-60	60 ns	30 ns	15 ns	25 ns
’248GBK32F-70	70 ns	35 ns	18 ns	30 ns
’248GBK32F-80	80 ns	40 ns	20 ns	35 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range**
  0°C to 70°C
- **Gold-Tabbed Versions Available:† TM124FBK32F TM248GBK32F**
- **Tin-Lead Solder-Tabbed Versions Available: TM124FBK32U TM248GBK32U**

description

TM124FBK32F

The TM124FBK32F is a 4M-byte DRAM organized as four times 1048576 × 8 in a 72-pin SIMM. The SIMM is composed of two TMS418169DZ 1 048 576 × 16-bit DRAMs, each in a 42-lead plastic SOJ package mounted on a substrate with decoupling capacitors. The TMS418169DZ is described in the TMS418169 data sheet (literature number SMKS886). The TM124FBK32F SIMM is available in the single-sided BK-leadless module for use with sockets.

TM248GBK32F

The TM248GBK32F is an 8M-byte DRAM organized as four times 2 097 152 × 8 in a 72-pin SIMM. The SIMM is composed of four TMS418169DZ 1 048 576 × 16-bit DRAMs, each in a 42-lead plastic SOJ package mounted on a substrate with decoupling capacitors. The TMS418169DZ is described in the TMS418169 data sheet (literature number SMKS886). The TM248GBK32F SIMM is available in the double-sided BK-leadless module for use with sockets.

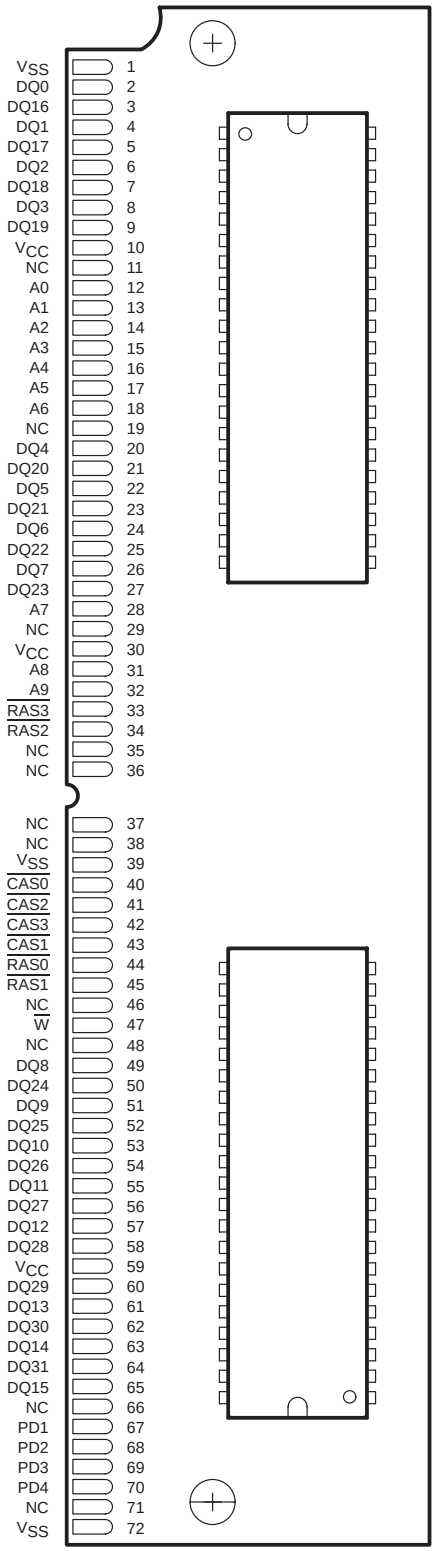
operation

The TM124FBK32F operates as two TMS418169DZs connected as shown in the functional block diagram and in Table 1. The TM248GBK32F operates as four TMS418169DZs connected as shown in the functional block diagram and in Table 1. The common I/O feature dictates the use of early-write cycles to prevent contention on D and Q.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

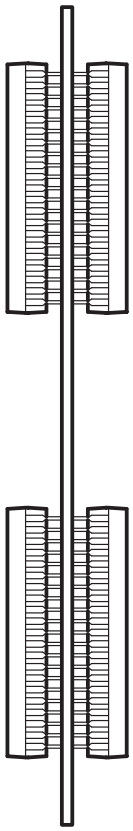
† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

BK SINGLE IN-LINE MEMORY MODULE
(TOP VIEW)



TM124FBK32F
(SIDE VIEW)

TM248GBK32F
(SIDE VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS0}$–$\overline{CAS3}$	Column-Address Strobe
DQ0–DQ31	Data In/Data Out
NC	No Connection
PD1– PD4	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124FBK32F	80 ns	V_{SS}	V_{SS}	NC	V_{SS}
	70 ns	V_{SS}	V_{SS}	V_{SS}	NC
	60 ns	V_{SS}	V_{SS}	NC	NC
TM248GBK32F	80 ns	NC	NC	NC	V_{SS}
	70 ns	NC	NC	V_{SS}	NC
	60 ns	NC	NC	NC	NC

Table 1. Connection Table

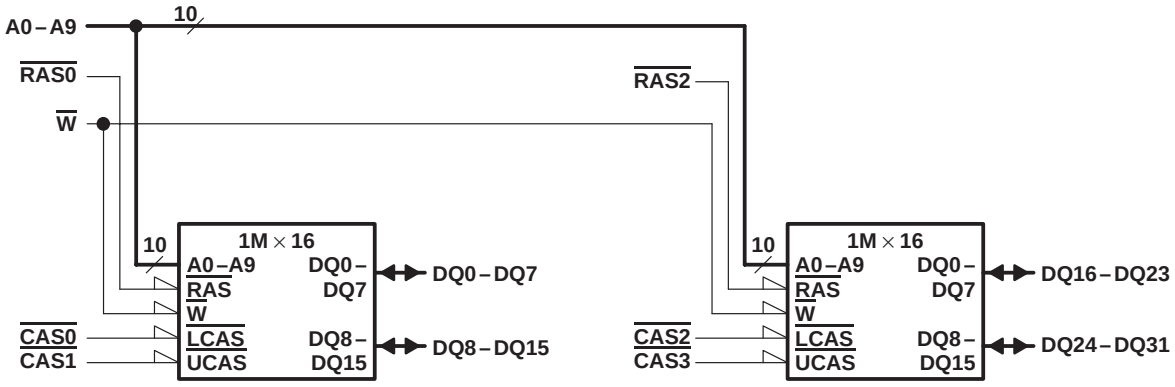
DATA BLOCK	$\overline{RAS}$x		$\overline{CAS}$x
	SIDE 1	SIDE 2†	
DQ0–DQ7	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS0}$
DQ8–DQ15	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{CAS1}$
DQ16–DQ23	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS2}$
DQ24–DQ31	$\overline{RAS2}$	$\overline{RAS3}$	$\overline{CAS3}$

† Side 2 applies to the TM248GBK32F and the TM248GBK32U.

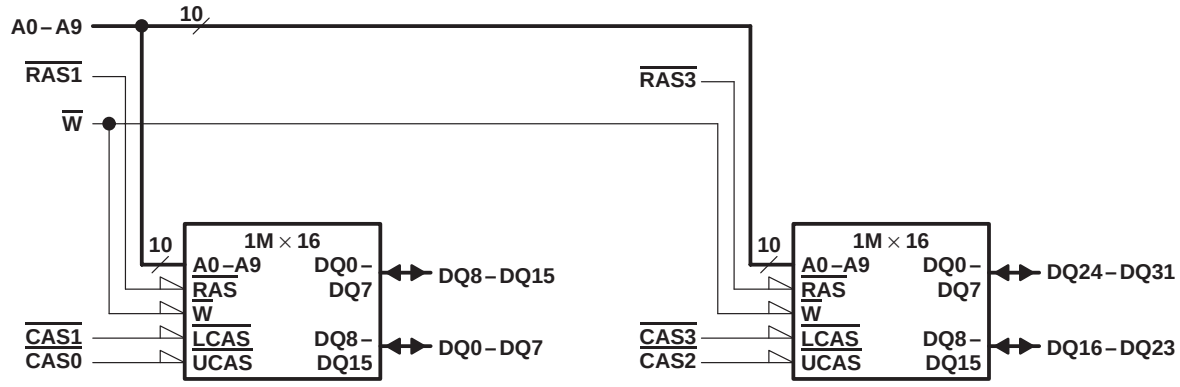
single in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM124FBK32F and TM248GBK32F: Nickel plate and gold plate over copper
Contact area for TM124FBK32U and TM248GBK32U: Nickel plate and tin/lead over copper

functional block diagram (TM124FBK32F and TM248GBK32F, side 1)



functional block diagram (TM248GBK32F, side 2)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . – 1 V to 7 V
Voltage range on any pin (see Note 1) . . . . . – 1 V to 7 V
Short-circuit output current . . . . . 50 mA
Power dissipation: TM124FBK32F, TM124FBK32U . . . . . 2 W
TM248GBK32F, TM248GBK32U . . . . . 4 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	'124FBK32F-60		'124FBK32F-70		'124FBK32F-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		380		360		340	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		4		4		4	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		2		2		2	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		380		360		340	mA
I_{CC4}	Average EDO current (see Note 4)	V_{CC} = 5.5 V, t_{HPC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling		200		180		160	mA

‡ For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS †	'248GBK32F-60		'248GBK32F-70		'248GBK32F-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 20		± 20		± 20	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		384		364		344	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		8		8		8	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		4		4		4	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Notes 3 and 5)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		760		720		680	mA
I_{CC4}	Average EDO current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling		204		184		164	mA

† For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}
5. Measured with both sides in CBR cycle

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		'124FBK32F		'248GBK32F		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, A0 – A9		12		22	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$ inputs		8		8	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$ inputs		8		15	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		16		30	pF
$C_{o(DQ)}$	Output capacitance on DQ0 – DQ31		8		15	pF

NOTE 6: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124FBK32F-60 '248GBK32F-60		'124FBK32F-70 '248GBK32F-70		'124FBK32F-80 '248GBK32F-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	$\overline{CAS}$ to output in low-impedance state	0		0		0		ns
t_{REZ}	Output disable time after $\overline{RAS}$ high (see Note 7)	3	15	3	18	3	20	ns
t_{WEZ}	Output disable time after $\overline{W}$ low (see Note 7)	3	15	3	18	3	20	ns

NOTE 7: t_{REZ} and t_{WEZ} are specified when the output is no longer driven.

EDO timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124FBK32F-60 '248GBK32F-60		'124FBK32F-70 '248GBK32F-70		'124FBK32F-80 '248GBK32F-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{HPC}	Cycle time, EDO page-mode read or write	25		30		35		ns
t_{PRWC}	Cycle time, EDO read-write	80		90		100		ns
t_{CSH}	Hold time, $\overline{CAS}$ from $\overline{RAS}$	50		55		60		ns
t_{DOH}	Hold time, output from $\overline{CAS}$	3		3		3		ns
t_{CAS}	Pulse duration, $\overline{CAS}$	10	10000	12	10000	15	10000	ns
t_{WPE}	Pulse duration, $\overline{W}$ (output disable only)	5		5		5		ns
t_{CP}	Precharge time, $\overline{CAS}$	5		5		5		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124FBK32F-60 '248GBK32F-60		'124FBK32F-70 '248GBK32F-70		'124FBK32F-80 '248GBK32F-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 8)	110		130		150		ns
t_{RWC}	Cycle time, read-write	150		175		200		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{RASS}	Pulse duration, self refresh entry from $\overline{RAS}$ low	100		100		100		µs
t_{RPS}	Pulse duration, $\overline{RAS}$ precharge after self refresh	110		130		150		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{CAS}$ low	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	10		12		15		ns

NOTE 8: The ac parameter assumes t_T = 5 ns.

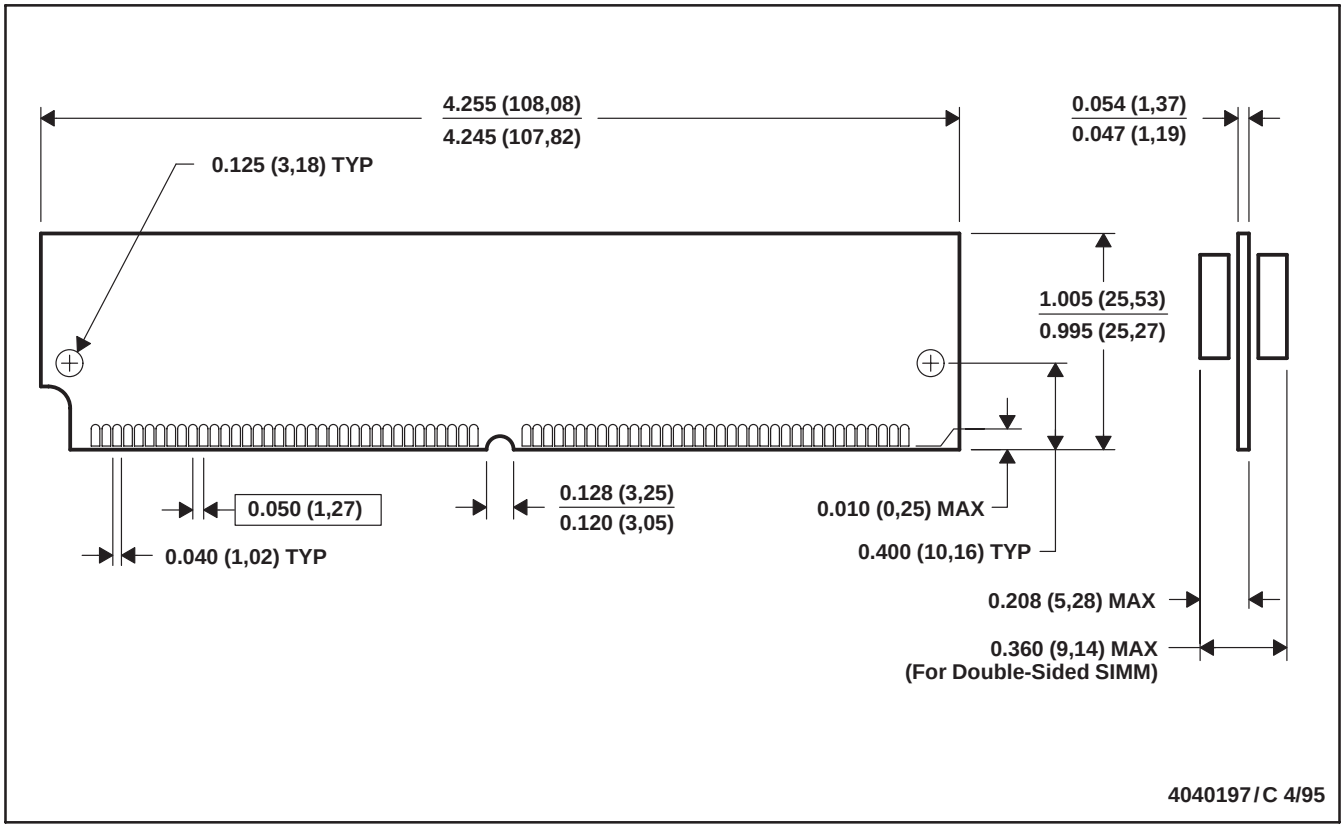
timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		’124FBK32F-60 ’248GBK32F-60		’124FBK32F-70 ’248GBK32F-70		’124FBK32F-80 ’248GBK32F-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	10		12		15		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low	0		0		0		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DH}	Hold time, data after $\overline{CAS}$ low	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 9)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low	10		15		15		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{CAS}$ precharge	35		40		45		ns
t_{CHS}	Hold time, $\overline{CAS}$ low after $\overline{RAS}$ high (self refresh)	– 50		– 50		– 50		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	5		5		5		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 10)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	20		25		30		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (CBR only)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	10		12		15		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	30	2	30	2	30	ns

NOTES: 9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. The maximum value is specified only to assure access time.

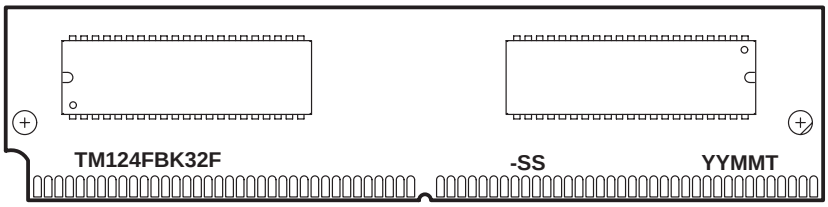
MECHANICAL DATA

BK (R-PSIM-N72) **SINGLE-IN-LINE MEMORY MODULE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

device symbolization (TM124FBK32F illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE: Location of symbolization may vary.

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