TM497FBK32R, TM497FBK32G 4194304 BY 32-BIT
TM893GBK32R, TM893GBK32G 8388608 BY 32-BIT
EXTENDED DATA OUT DYNAMIC RAM MODULES

SMMS672 – FEBRUARY 1997

- **Organization**
  - **TM497FBK32R/G: 4 194 304 x 32**
  - **TM893GBK32R/G: 8 388 608 x 32**
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-Pin Single-In-Line Memory Module (SIMM) for Use With Sockets**
- **TM497FBK32R/G – Uses Eight 16M-Bit Dynamic Random-Access Memories (DRAMs) in Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM893GBK32R/G – Uses Sixteen 16M-Bit DRAMs in Plastic SOJ Packages**
- **Long Refresh Period**
  32 ms (2 048 Cycles)
- **All Inputs, Outputs, Clocks Fully TTL-Compatible**
- **3-State Output**
- **Common $\overline{\text{CAS}}$ Control for Eight Common Data-In and Data-Out Lines in Four Blocks**
- **Extended Data Out (EDO) Operation With $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ (CBR), $\overline{\text{RAS}}$-Only, and Hidden Refresh**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	EDO CYCLE t_{HPC} (MIN)
’497FBK32R/G-50	50 ns	40 ns	20 ns	35 ns
’497FBK32R/G-60	60 ns	30 ns	15 ns	25 ns
’497FBK32R/G-70	70 ns	35 ns	18 ns	30 ns
’893GBK32R/G-50	50 ns	40 ns	20 ns	35 ns
’893GBK32R/G-60	60 ns	30 ns	15 ns	25 ns
’893GBK32R/G-70	70 ns	35 ns	18 ns	30 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range**
  0°C to 70°C
- **Gold-Tabbed Version Available:**[†]
  TM497FBK32G, TM893GBK32G
- **Tin-Lead (Solder-) Tabbed Version Available: TM497FBK32R, TM893GBK32R**

description

The TM497FBK32R/G, designed as 4 × 4 194304 × 8-bits, is a 16M-byte, 72-pin, leadless, single-in-line memory module (SIMM). The SIMM is composed of eight (8) TMS417409DJs, 4194304 × 4-bit DRAMs, each in 24/26-lead, plastic, small-outline J-lead (SOJ) packages mounted on a substrate with decoupling capacitors. See the TMS417409A data sheet (literature number SMKS893) for timing diagrams.

The TM497FBK32R/G SIMM is available in the single-sided BK leadless module for use with sockets. The TM497FBK32R/G features $\overline{\text{RAS}}$ access times of 50, 60, and 70 ns. This device is designed for operation from 0°C to 70°C.

The TM893GBK32R/G, designed as 4 × 8 388608 × 8-bits, is a 32M-byte, 72-pin, leadless SIMM. The SIMM is composed of sixteen TMS417409DJs, 4194304 × 4-bit DRAMs, each in 24/26-lead, plastic, small-outline J-lead (SOJ) packages mounted on a substrate with decoupling capacitors. See the TMS417409A data sheet (literature number SMKS893) for timing diagrams.

The TM893GBK32R/G SIMM is available in the double-sided BK leadless module for use with sockets. The TM893GBK32R/G features $\overline{\text{RAS}}$ access times of 50, 60, and 70 ns. This device is characterized for operation from 0°C to 70°C.

operation

The TM497FBK32R/G operates as eight TMS417409DJs connected as shown in the functional block diagram of TM497RBK32R/G and in Table 1. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

[†] Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

TEXAS INSTRUMENTS

operation (continued)

The TM893GBK32R/G operates as sixteen TMS417409DJs connected as shown in the functional block diagram of TM893GBK32R/G and in Table 2. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

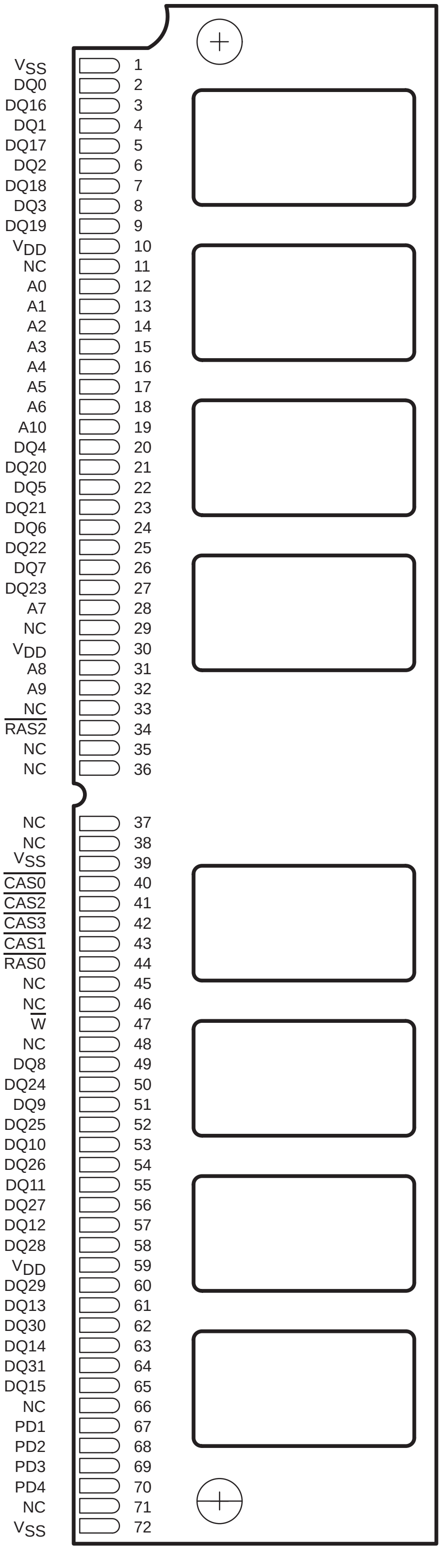
refresh

The refresh period is extended to 32 ms and, during this period, each of the 2 048 rows must be strobed with $\overline{\text{RAS}}$ to retain data. $\overline{\text{CAS}}$ can remain high during the refresh sequence to conserve power.

power up

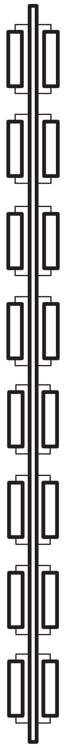
To achieve proper operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{DD} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{\text{RAS}}$-only or CBR) cycle.

BK SINGLE-IN-LINE PACKAGE
(TOP VIEW)



TM497FBK32R/G
(SIDE VIEW)

TM893GBK32R/G
(SIDE VIEW)



PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{\text{CAS0}}$–$\overline{\text{CAS3}}$	Column-Address Strobe
DQ0–DQ31	Data In / Data Out
NC	No Connection
PD1–PD4	Presence Detects
$\overline{\text{RAS0}}$–$\overline{\text{RAS3}}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{\text{W}}$	Write Enable

PRESENCE DETECT

SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM497FBK32R/G	70 ns	V_{SS}	NC	V_{SS}	NC
	60 ns	V_{SS}	NC	NC	NC
	50 ns	V_{SS}	NC	NC	V_{SS}
TM893GBK32R/G	70 ns	NC	V_{SS}	V_{SS}	NC
	60 ns	NC	V_{SS}	NC	NC
	50 ns	NC	V_{SS}	NC	V_{SS}

Table 1. TM497FBK32R/G Connection Table

DATA BLOCK	$\overline{\text{RASx}}$	$\overline{\text{CASx}}$
DQ0–DQ7	$\overline{\text{RAS0}}$	$\overline{\text{CAS0}}$
DQ8–DQ15	$\overline{\text{RAS0}}$	$\overline{\text{CAS1}}$
DQ16–DQ23	$\overline{\text{RAS2}}$	$\overline{\text{CAS2}}$
DQ24–DQ31	$\overline{\text{RAS2}}$	$\overline{\text{CAS3}}$

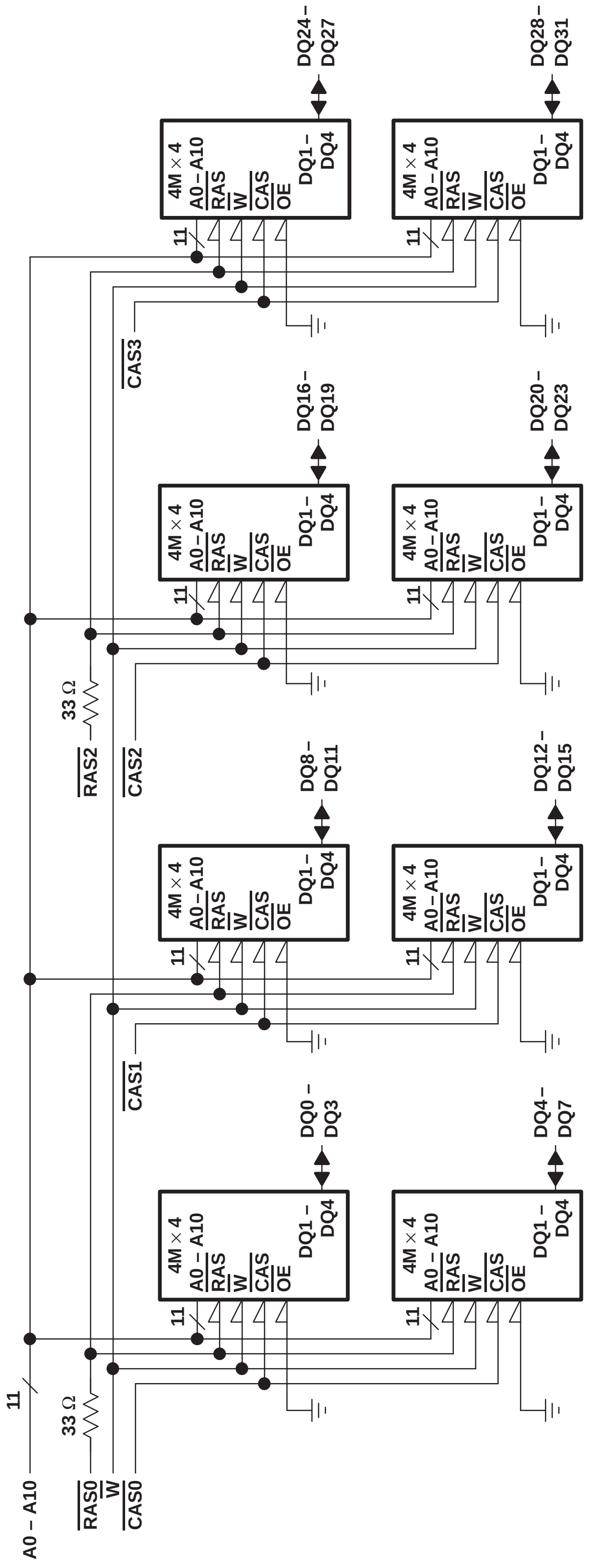
Table 2. TM893GBK32R/G Connection Table

DATA BLOCK	$\overline{\text{RASx}}$		$\overline{\text{CASx}}$
	Side 1	Side 2	
DQ0–DQ7	$\overline{\text{RAS0}}$	$\overline{\text{RAS1}}$	$\overline{\text{CAS0}}$
DQ8–DQ15	$\overline{\text{RAS0}}$	$\overline{\text{RAS1}}$	$\overline{\text{CAS1}}$
DQ16–DQ23	$\overline{\text{RAS2}}$	$\overline{\text{RAS3}}$	$\overline{\text{CAS2}}$
DQ24–DQ31	$\overline{\text{RAS2}}$	$\overline{\text{RAS3}}$	$\overline{\text{CAS3}}$

single-in-line memory module and components

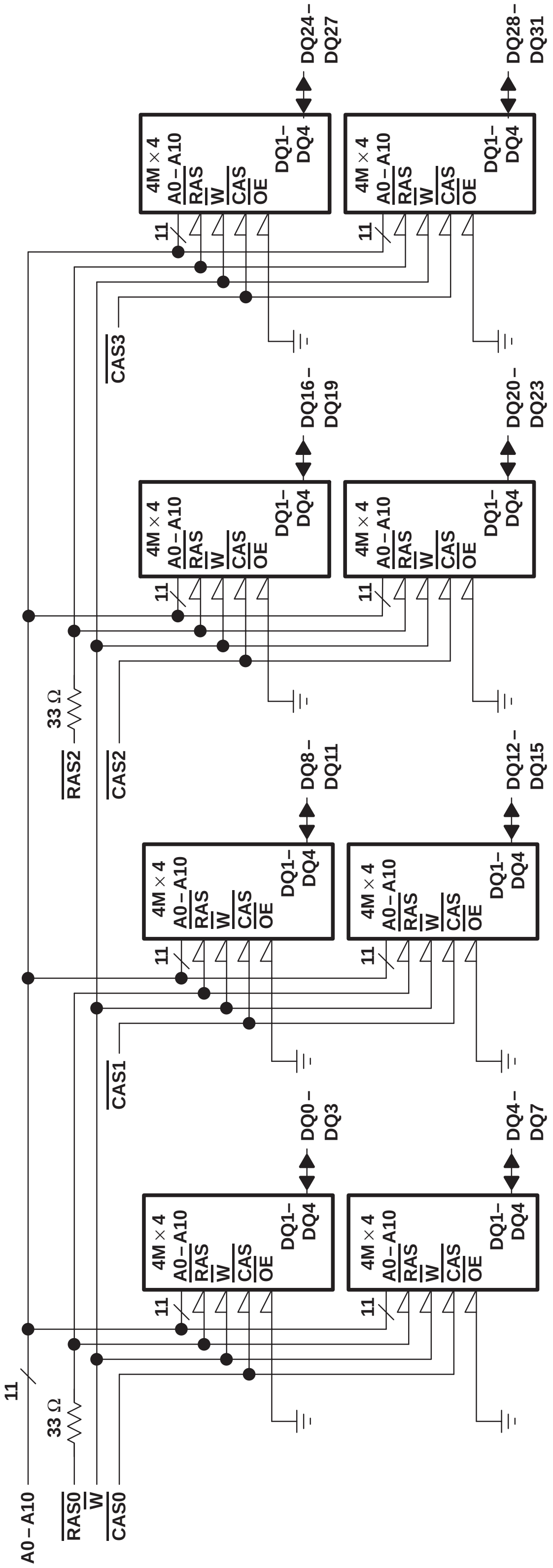
PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM497FBK32G and TM893GBK32G: Nickel plate and gold plate over copper
Contact area for TM497FBK32R and TM893GBK32R: Nickel plate and tin-lead over copper

functional block diagram of TM497RBK32R/G

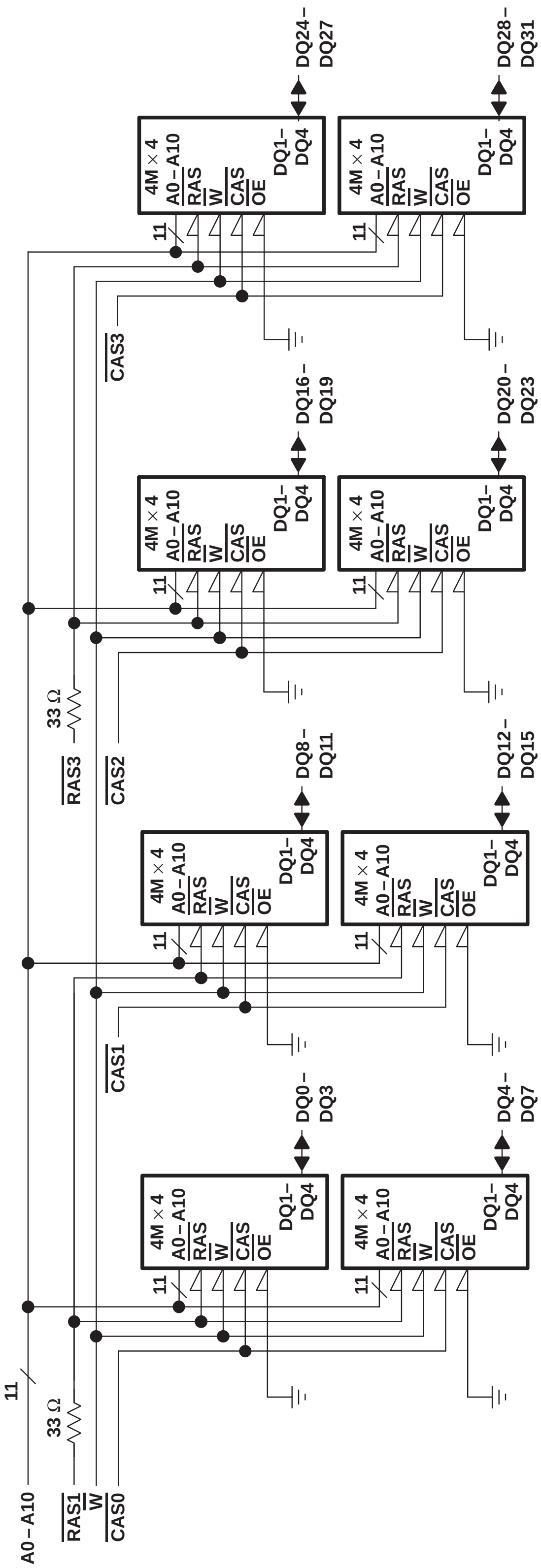


functional block diagrams of TM893GBK32R/G

side 1



side 2



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{DD} (see Note 1)	– 1 V to 7 V
Voltage range on any pin (see Note 1)	– 1 V to 7 V
Short-circuit output current	50 mA
Power dissipation	8 W
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	– 55°C to 125°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS[‡]	’497FBK32-50		’497FBK32-60		’497FBK32-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{DD} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{DD}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{DD} = 5.5 V, V_O = 0 V to V_{DD}, $\overline{\text{CAS}}$ high		± 10		± 10		± 10	µA
I_{CC1}	Average read- or write-cycle current (see Note 3)	V_{DD} = 5.5 V, Minimum cycle		960		880		800	mA
I_{CC2}	Average standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high		16		16		16	mA
		V_{IH} = V_{DD} – 0.2 V (CMOS), After one memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high		8		8		8	mA
I_{CC3}	Average refresh current ($\overline{\text{RAS}}$ only or CBR) (see Note 3)	V_{DD} = 5.5 V, Minimum cycle, $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ high ($\overline{\text{RAS}}$ only); $\overline{\text{RAS}}$ low after $\overline{\text{CAS}}$ low (CBR)		960		880		800	mA
I_{CC4}	Average EDO (see Note 4)	V_{DD} = 5.5 V, t_{PC} = MIN, $\overline{\text{RAS}}$ low, $\overline{\text{CAS}}$ cycling		800		720		640	mA

[‡] For test conditions shown as MIN / MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Measured with a maximum of one address change while $\overline{\text{RAS}}$ = V_{IL}

4. Measured with a maximum of one address change while $\overline{\text{CAS}}$ = V_{IH}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	’893GBK32-50		’893GBK32-60		’893GBK32-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{DD} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{DD}		± 20		± 20		± 20	µA
I_O	Output current (leakage)	V_{DD} = 5.5 V, V_O = 0 V to V_{DD}, $\overline{\mathrm{CAS}}$x high		± 20		± 20		± 20	µA
I_{CC1}	Average read- or write-cycle current (see Note 3)	V_{DD} = 5.5 V, Minimum cycle		976		896		816	mA
I_{CC2}	Average standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{\mathrm{RAS}}$x and $\overline{\mathrm{CAS}}$x high		32		32		32	mA
		V_{IH} = V_{DD} – 0.2 V (CMOS), After one memory cycle, $\overline{\mathrm{RAS}}$x and $\overline{\mathrm{CAS}}$x high		16		16		16	mA
I_{CC3}	Average refresh current ($\overline{\mathrm{RAS}}$ only or CBR) (see Note 3)	V_{DD} = 5.5 V, $\overline{\mathrm{RAS}}$x cycling, ($\overline{\mathrm{RAS}}$x only); Minimum cycle $\overline{\mathrm{CAS}}$x low (CBR) $\overline{\mathrm{CAS}}$x high $\overline{\mathrm{RAS}}$x low after		1920		1760		1600	mA
I_{CC4}	Average EDO (see Note 4)	V_{DD} = 5.5 V, t_{PC} = MIN, $\overline{\mathrm{RAS}}$x low, $\overline{\mathrm{CAS}}$x cycling		1600		1440		1280	mA

† For test conditions shown as MIN / MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Measured with a maximum of one address change while $\overline{\mathrm{RAS}}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{\mathrm{CAS}}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		TM497FBK32R/G		TM893GBK32R/G		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		50		80	pF
$C_{i(R)}$	Input capacitance, $\overline{\mathrm{RAS}}$ inputs		28		33	pF
$C_{i(C)}$	Input capacitance, $\overline{\mathrm{CAS}}$ inputs		17		28	pF
$C_{i(W)}$	Input capacitance, write-enable input		66		112	pF
$C_{o(DQ)}$	Output capacitance on DQ pins		9		14	pF

NOTE 5: V_{DD} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 6)

PARAMETER		’497FBK32-50 ’893GBK32-50		’497FBK32-60 ’893GBK32-60		’497FBK32-70 ’893GBK32-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		25		30		35	ns
t_{CAC}	Access time from $\overline{\text{CAS}}$ low		13		15		18	ns
t_{CPA}	Access time from column precharge		28		35		40	ns
t_{RAC}	Access time from $\overline{\text{RAS}}$ low		50		60		70	ns
t_{CLZ}	$\overline{\text{CAS}}$ to output in low-impedance state	0		0		0		ns
t_{OH}	Output disable time from start of $\overline{\text{CAS}}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{\text{CAS}}$ high (see Note 6)	0	13	0	15	0	18	ns

NOTES: 6. With ac parameters, it is assumed that t_T = 2 ns.
7. t_{OFF} is specified when the output is no longer driven.

EDO timing requirements over recommended ranges of supply voltage and operating free-air temperature

		’497FBK32-50 ’893GBK32-50		’497FBK32-60 ’893GBK32-60		’497FBK32-70 ’893GBK32-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{HPC}	Cycle time, EDO page mode read or write	20		25		30		ns
t_{PRWC}	Cycle time, EDO read-write	57		68		78		ns
t_{CSH}	Hold time, $\overline{\text{CAS}}$ after $\overline{\text{RAS}}$	40		48		58		ns
t_{DOH}	Hold time, output after $\overline{\text{RAS}}$	5		5		5		ns
t_{CAS}	Pulse duration, $\overline{\text{CAS}}$	8	10 000	10	10 000	12	10 000	ns
t_{WPE}	Pulse duration, $\overline{\text{W}}$ (output disable only)	7		7		7		ns
t_{CP}	Precharge time, $\overline{\text{CAS}}$	8		10		10		ns

NOTE 6: With ac parameters, it is assumed that t_T = 2 ns.

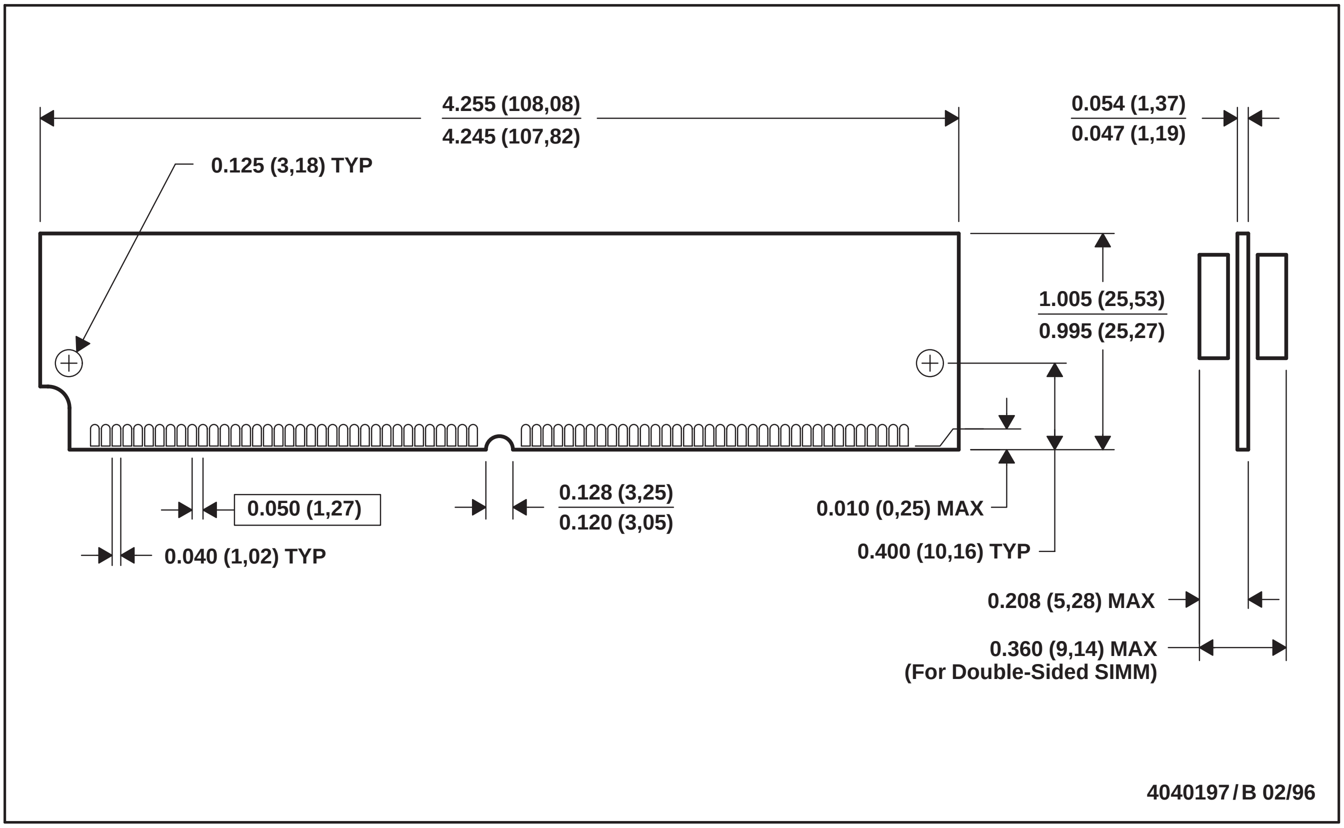
timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 6)

		’497FBK32-50 ’893GBK32-50		’497FBK32-60 ’893GBK32-60		’497FBK32-70 ’893GBK32-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 8)	84		104		124		ns
t_{RASP}	Pulse duration, page-mode, RAS low (see Note 8)	50	100 000	60	100 000	70	100 000	ns
t_{RAS}	Pulse duration, non-page-mode, RAS low (see Note 8)	50	10 000	60	10 000	70	10 000	ns
t_{CAS}	Pulse duration, CAS low	20	10 000	15	10 000	18	10 000	ns
t_{CP}	Pulse duration, CAS high	8		10		10		ns
t_{RP}	Pulse duration, RAS high (precharge)	30		40		50		ns
t_{WP}	Pulse duration, W low	8		10		10		ns
t_{ASC}	Setup time, column address before CAS low	0		0		0		ns
t_{ASR}	Setup time, row address before RAS low	0		0		0		ns
t_{DS}	Setup time, data before CAS low (see Note 9)	0		0		0		ns
t_{RCS}	Setup time, W high before CAS low	0		0		0		ns
t_{CWL}	Setup time, W-low before CAS high	8		10		12		ns
t_{RWL}	Setup time, W-low before RAS high	8		10		12		ns
t_{WCS}	Setup time, W-low before CAS low	0		0		0		ns
t_{WRP}	Setup time, W-high before RAS low (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after CAS low	8		10		12		ns
t_{RHCP}	Hold time, RAS high after CAS precharge	28		35		40		ns
t_{DH}	Hold time, data after CAS low (see Note 9)	8		10		12		ns
t_{RAH}	Hold time, row address after RAS low	8		10		10		ns
t_{RCH}	Hold time, W high after CAS high (see Note 10)	0		0		0		ns
t_{RRH}	Hold time, W high after RAS high (see Note 10)	0		0		0		ns
t_{WCH}	Hold time, W low after CAS low (early-write only)	10		10		12		ns
t_{WRH}	Hold time, W high after RAS low (CBR refresh only)	10		10		10		ns
t_{CHR}	Delay time, RAS low to CAS high (CBR refresh only)	8		10		10		ns
t_{CRP}	Delay time, CAS high to RAS low	5		5		5		ns
t_{CSH}	Delay time, RAS low to CAS high	40		48		58		ns
t_{CSR}	Delay time, CAS low to RAS low (CBR refresh only)	5		5		5		ns
t_{RAD}	Delay time, RAS low to column address (see Note 11)	10	25	12	30	12	35	ns
t_{RAL}	Delay time, column address to RAS high	25		30		35		ns
t_{CAL}	Delay time, column address to CAS high	18		20		25		ns
t_{RCD}	Delay time, RAS low to CAS low (see Note 11)	20	37	20	45	20	52	ns
t_{RPC}	Delay time, RAS high to CAS low (CBR only)	5		5		5		ns
t_{RSH}	Delay time, CAS low to RAS high	8		10		12		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_{T}	Transition time	2	30	2	30	2	30	ns

NOTES:
6. With ac parameters, it is assumed that t_T = 2 ns.
8. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
9. Referenced to the later of CAS or W in write operations.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. The maximum value is specified only to assure access time.

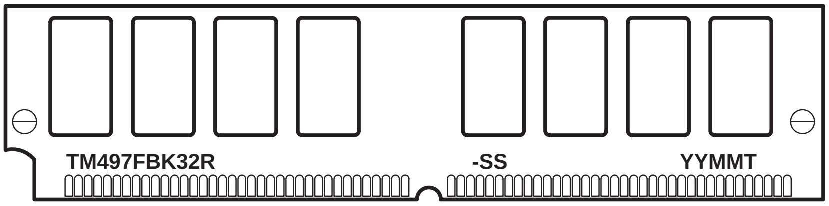
MECHANICAL DATA

BK (R-PSIM-N72) **SINGLE-IN-LINE MEMORY MODULE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE: The location of the part number may vary.

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