TM497FBK32H, TM497FBK32I 4194304 BY 32-BIT
TM893GBK32H, TM893GBK32I 8388608 BY 32-BIT
EXTENDED-DATA-OUT DYNAMIC RAM MODULES

SMMS674A – MARCH 1997 – REVISED SEPTEMBER 1997

- **Organization**
  - **– TM497FBK32H/I: 4 194 304 x 32**
  - **– TM893GBK32H/I: 8 388 608 x 32**
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-Pin Single-In-Line Memory Module (SIMM) for Use With Sockets**
- **TM497FBK32H/I – Uses Eight 16M-Bit Dynamic Random-Access Memories (DRAMs) in Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM893GBK32H/I – Uses Sixteen 16M-Bit DRAMs in Plastic SOJ Packages**
- **Long Refresh Period**
  32 ms (2 048 Cycles)
- **All Inputs, Outputs, Clocks Fully TTL-Compatible**
- **3-State Output**
- **Common $\overline{\text{CAS}}$ Control for Eight Common Data-In and Data-Out Lines in Four Blocks**
- **Extended Data Out (EDO) Operation With $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ (CBR), $\overline{\text{RAS}}$-Only, and Hidden Refresh**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MAX)	EDO CYCLE t_{HPC} (MIN)
’497FBK32H/I-50	50 ns	25 ns	13 ns	20 ns
’497FBK32H/I-60	60 ns	30 ns	15 ns	25 ns
’497FBK32H/I-70	70 ns	35 ns	18 ns	30 ns
’893GBK32H/I-50	50 ns	25 ns	13 ns	20 ns
’893GBK32H/I-60	60 ns	30 ns	15 ns	25 ns
’893GBK32H/I-70	70 ns	35 ns	18 ns	30 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range**
  0°C to 70°C
- **Gold-Tabbed Version Available:**† **TM497FBK32H, TM893GBK32H**
- **Tin-Lead (Solder-) Tabbed Version Available: TM497FBK32I, TM893GBK32I**

description

The TM497FBK32H/I is a 16M-byte dynamic random-access memory (DRAM) module organized as four times 4194304 × 8 bits in a 72-pin leadless single-in-line memory module (SIMM). The SIMM is composed of eight TMS417409ADJ DRAMs, each in 24/26-lead plastic small-outline J-lead (SOJ) packages mounted on a substrate with decoupling capacitors. The TMS417409ADJ is described in the TMS416409A, TMS417409A data sheet (literature number SMKS893).

The TM497FBK32H/I SIMM is available in the single-sided BK leadless module for use with sockets. The TM497FBK32H/I features $\overline{\text{RAS}}$ access times of 50, 60, and 70 ns. This device is characterized for operation from 0°C to 70°C.

The TM893GBK32H/I is a 32M-byte DRAM organized as four times 8388608 × 8 bits in a 72-pin leadless SIMM. The SIMM is composed of sixteen TMS417409ADJ DRAMs.

The TM893GBK32H/I SIMM is available in the double-sided BK leadless module for use with sockets. The TM893GBK32H/I features $\overline{\text{RAS}}$ access times of 50, 60, and 70 ns. This device is characterized for operation from 0°C to 70°C.

operation

The TM497FBK32H/I operates as eight TMS417409ADJs connected as shown in Figure 1 and in Table 1. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

The TM893GBK32H/I operates as sixteen TMS417409ADJs connected as shown in Figure 2 and in Table 2. The common I/O feature dictates the use of early write cycles to prevent contention on D and Q.

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† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

TEXAS INSTRUMENTS

Table 1. TM497FBK32H/I Connection Table

DATA BLOCK	$\overline{\text{RASx}}$	$\overline{\text{CASx}}$
DQ0 – DQ7	$\overline{\text{RAS0}}$	$\overline{\text{CAS0}}$
DQ8 – DQ15	$\overline{\text{RAS0}}$	$\overline{\text{CAS1}}$
DQ16 – DQ23	$\overline{\text{RAS2}}$	$\overline{\text{CAS2}}$
DQ24 – DQ31	$\overline{\text{RAS2}}$	$\overline{\text{CAS3}}$

Table 2. TM893GBK32H/I Connection Table

DATA BLOCK	$\overline{\text{RASx}}$		$\overline{\text{CASx}}$
	Side 1	Side 2	
DQ0 – DQ7	$\overline{\text{RAS0}}$	$\overline{\text{RAS1}}$	$\overline{\text{CAS0}}$
DQ8 – DQ15	$\overline{\text{RAS0}}$	$\overline{\text{RAS1}}$	$\overline{\text{CAS1}}$
DQ16 – DQ23	$\overline{\text{RAS2}}$	$\overline{\text{RAS3}}$	$\overline{\text{CAS2}}$
DQ24 – DQ31	$\overline{\text{RAS2}}$	$\overline{\text{RAS3}}$	$\overline{\text{CAS3}}$

refresh

The refresh period is extended to 32 ms and, during this period, each of the 2048 rows must be strobed with $\overline{\text{RAS}}$ to retain data. $\overline{\text{CAS}}$ can remain high during the refresh sequence to conserve power.

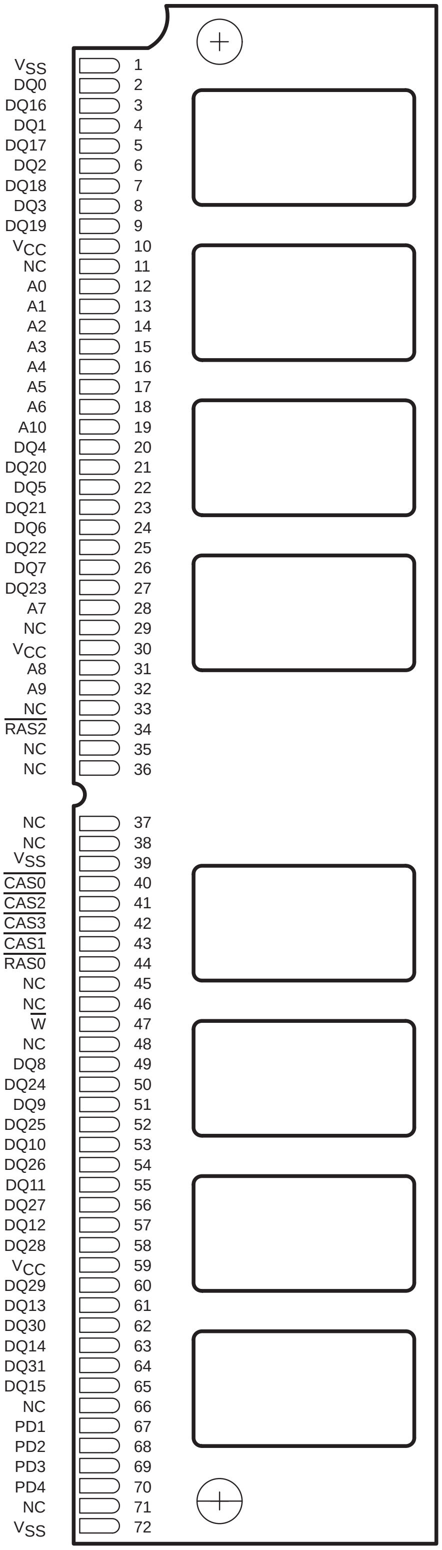
power up

To achieve proper operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{\text{RAS}}$-only or CBR) cycle.

single-in-line memory module and components

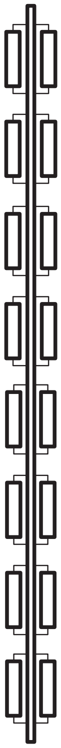
PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM497FBK32H and TM893GBK32H: Nickel plate and gold plate over copper
Contact area for TM497FBK32I and TM893GBK32I: Nickel plate and tin-lead over copper

BK SINGLE-IN-LINE PACKAGE
(TOP VIEW)



TM497FBK32H/I
(SIDE VIEW)

TM893GBK32H/I
(SIDE VIEW)



PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{\text{CAS0}}$–$\overline{\text{CAS3}}$	Column-Address Strobe
DQ0–DQ31	Data In / Data Out
NC	No Connection
PD1–PD4	Presence Detects
$\overline{\text{RAS0}}$–$\overline{\text{RAS3}}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{\text{W}}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		**PD1 (67)**	**PD2 (68)**	**PD3 (69)**	**PD4 (70)**
TM497FBK32H/I	50 ns	V_{SS}	NC	V_{SS}	V_{SS}
	60 ns	V_{SS}	NC	NC	NC
	70 ns	V_{SS}	NC	V_{SS}	NC
TM893GBK32H/I	50 ns	NC	V_{SS}	V_{SS}	V_{SS}
	60 ns	NC	V_{SS}	NC	NC
	70 ns	NC	V_{SS}	V_{SS}	NC

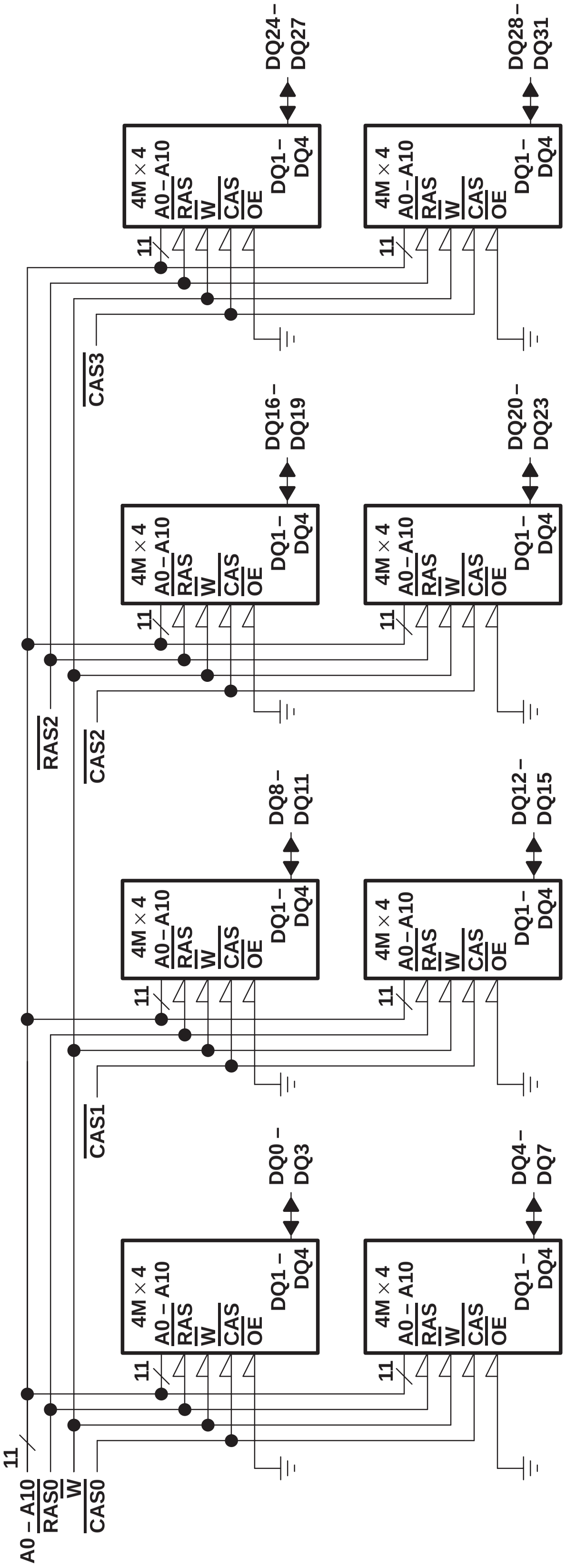


Figure 1. Functional Block Diagram of TM497FBK32H/I

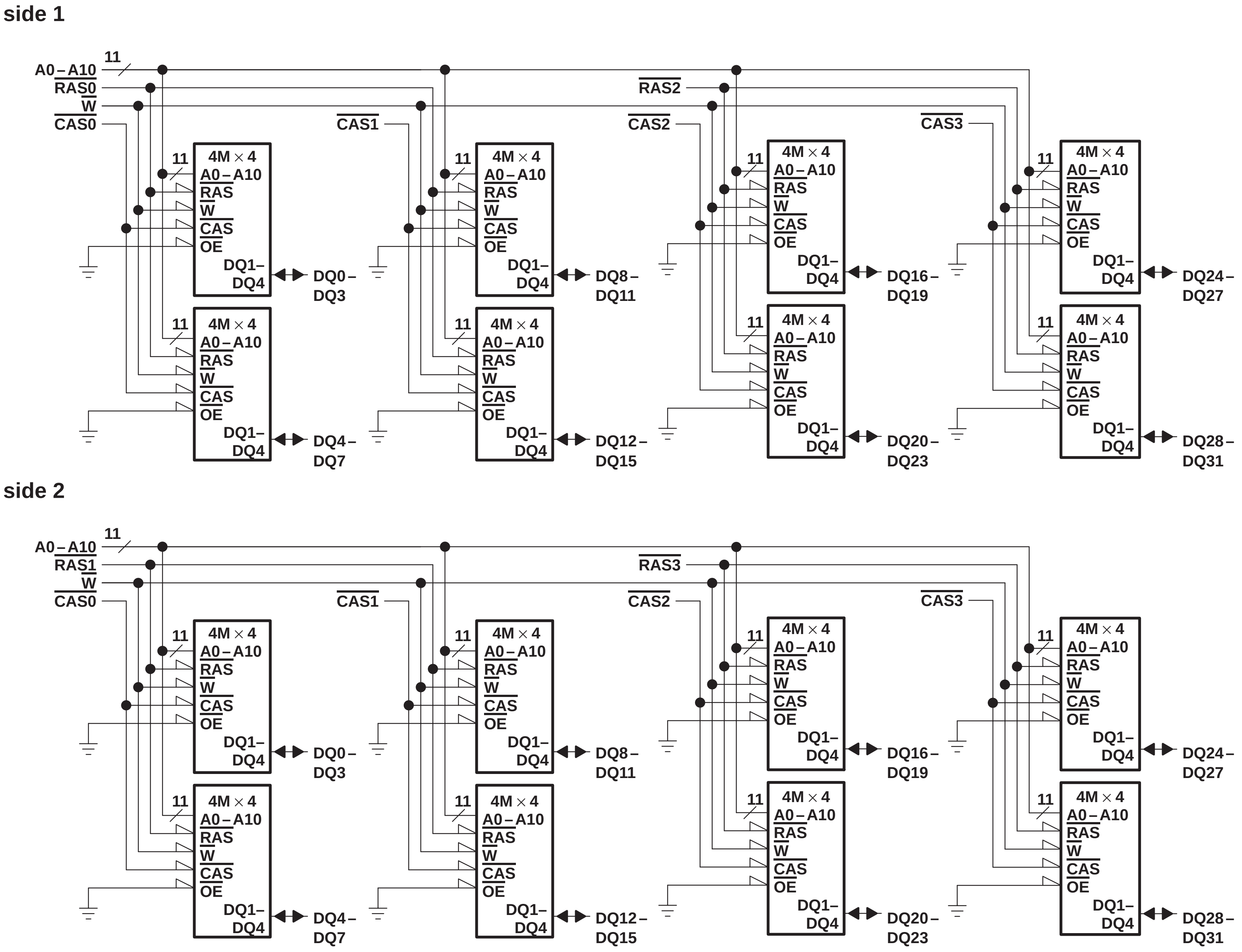


Figure 2. Functional Block Diagram of TM893GBK32H/I

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	– 1 V to 7 V
Voltage range on any pin (see Note 1)	– 1 V to 7 V
Short-circuit output current	50 mA
Power dissipation	8 W
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	– 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS‡	'497FBK32H/I-50		'497FBK32H/I-60		'497FBK32H/I-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{\text{CAS}}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		1040		880		800	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high		16		16		16	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After one memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high		8		8		8	mA
I_{CC3}	Average refresh current ($\overline{\text{RAS}}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ high ($\overline{\text{RAS}}$ only); $\overline{\text{RAS}}$ low after $\overline{\text{CAS}}$ low (CBR)		1040		880		800	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{\text{RAS}}$ low, $\overline{\text{CAS}}$ cycling		880		720		640	mA

‡ For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Measured with a maximum of one address change while $\overline{\text{RAS}}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{\text{CAS}}$ = V_{IH}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	’893GBK32H/I-50		’893GBK32H/I-60		’893GBK32H/I-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 20		± 20		± 20	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{\text{CAS}}$x high		± 20		± 20		± 20	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle		1056		896		816	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{\text{RAS}}$x and $\overline{\text{CAS}}$x high		32		32		32	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After one memory cycle, $\overline{\text{RAS}}$x and $\overline{\text{CAS}}$x high		16		16		16	mA
I_{CC3}	Average refresh current ($\overline{\text{RAS}}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, $\overline{\text{RAS}}$x cycling, ($\overline{\text{RAS}}$x only); Minimum cycle $\overline{\text{CAS}}$x low (CBR) $\overline{\text{CAS}}$x high $\overline{\text{RAS}}$x low after		2080		1760		1600	mA
I_{CC4}	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{\text{RAS}}$x low, $\overline{\text{CAS}}$x cycling		1760		1440		1280	mA

† For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 3. Measured with a maximum of one address change while $\overline{\text{RAS}}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{\text{CAS}}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		TM497FBK32H/I		TM893GBK32H/I		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		50		80	pF
$C_{i(R)}$	Input capacitance, $\overline{\text{RAS}}$ inputs		28		33	pF
$C_{i(C)}$	Input capacitance, $\overline{\text{CAS}}$ inputs		17		28	pF
$C_{i(W)}$	Input capacitance, write-enable input		66		112	pF
$C_{o(DQ)}$	Output capacitance on DQ pins		9		14	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER		’497FBK32H/I-50 ’893GBK32H/I-50		’497FBK32H/I-60 ’893GBK32H/I-60		’497FBK32H/I-70 ’893GBK32H/I-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		25		30		35	ns
t_{CAC}	Access time from $\overline{\text{CAS}}$ low		13		15		18	ns
t_{CPA}	Access time from column precharge		28		35		40	ns
t_{RAC}	Access time from $\overline{\text{RAS}}$ low		50		60		70	ns
t_{CLZ}	$\overline{\text{CAS}}$ to output in low-impedance state	0		0		0		ns
t_{REZ}	Output buffer turn off delay from $\overline{\text{RAS}}$ (see Note 6)	3	13	3	15	3	18	ns
t_{CEZ}	Output buffer turn off delay from $\overline{\text{CAS}}$ (see Note 6)	3	13	3	15	3	18	ns
t_{WEZ}	Output buffer turn off delay from $\overline{\text{W}}$ (see Note 6)	3	13	3	15	3	18	ns

NOTES: 6. The maximum values of t_{REZ}, t_{CEZ}, and t_{WEZ} are specified when the output is no longer driven. Data in should not be driven until one of the applicable maximum specifications is satisfied.

7. All cycles assume t_{T} = 2 ns.

EDO timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

		’497FBK32H/I-50 ’893GBK32H/I-50		’497FBK32H/I-60 ’893GBK32H/I-60		’497FBK32H/I-70 ’893GBK32H/I-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{HPC}	Cycle time, EDO page mode read or write	20		25		30		ns
t_{PRWC}	Cycle time, EDO read-write	57		68		78		ns
t_{CSH}	Hold time, $\overline{\text{CAS}}$ after $\overline{\text{RAS}}$	40		48		58		ns
t_{DOH}	Hold time, output after $\overline{\text{RAS}}$	5		5		5		ns
t_{CAS}	Pulse duration, $\overline{\text{CAS}}$	8	10 000	10	10 000	12	10 000	ns
t_{WPE}	Pulse duration, $\overline{\text{W}}$ (output disable only)	7		7		7		ns
t_{CP}	Precharge time, $\overline{\text{CAS}}$	8		10		10		ns

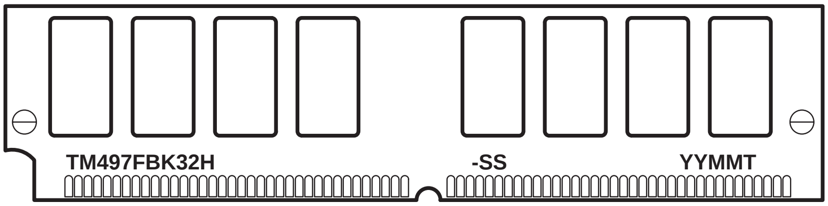
NOTE 7. All cycles assume t_{T} = 2 ns.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

		’497FBK32H / I-50 ’893GBK32H / I-50		’497FBK32H / I-60 ’893GBK32H / I-60		’497FBK32H / I-70 ’893GBK32H / I-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	84		104		124		ns
t_{RWC}	Cycle time, read-write	111		135		160		ns
t_{RASP}	Pulse duration, page-mode, $\overline{\text{RAS}}$ low (see Note 8)	50	100 000	60	100 000	70	100 000	ns
t_{RAS}	Pulse duration, non-page-mode, $\overline{\text{RAS}}$ low (see Note 8)	50	10 000	60	10 000	70	10 000	ns
t_{CAS}	Pulse duration, $\overline{\text{CAS}}$ low	8	10 000	10	10 000	12	10 000	ns
t_{CP}	Pulse duration, $\overline{\text{CAS}}$ high	8		10		10		ns
t_{RP}	Pulse duration, $\overline{\text{RAS}}$ high (precharge)	30		40		50		ns
t_{WP}	Pulse duration, $\overline{\text{W}}$ low	8		10		10		ns
t_{ASC}	Setup time, column address before $\overline{\text{CAS}}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{\text{RAS}}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{\text{CAS}}$ low (see Note 11)	0		0		0		ns
t_{RCS}	Setup time, $\overline{\text{W}}$ high before $\overline{\text{CAS}}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{\text{W}}$-low before $\overline{\text{CAS}}$ high	8		10		12		ns
t_{RWL}	Setup time, $\overline{\text{W}}$-low before $\overline{\text{RAS}}$ high	8		10		12		ns
t_{WCS}	Setup time, $\overline{\text{W}}$-low before $\overline{\text{CAS}}$ low	0		0		0		ns
t_{WRP}	Setup time, $\overline{\text{W}}$-high before $\overline{\text{RAS}}$ low (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{\text{CAS}}$ low	8		10		12		ns
t_{RHCP}	Hold time, $\overline{\text{RAS}}$ high after $\overline{\text{CAS}}$ precharge	28		35		40		ns
t_{DH}	Hold time, data after $\overline{\text{CAS}}$ low (see Note 11)	8		10		12		ns
t_{RAH}	Hold time, row address after $\overline{\text{RAS}}$ low	8		10		10		ns
t_{RCH}	Hold time, $\overline{\text{W}}$ high after $\overline{\text{CAS}}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, $\overline{\text{W}}$ high after $\overline{\text{RAS}}$ high (see Note 9)	0		0		0		ns
t_{WCH}	Hold time, $\overline{\text{W}}$ low after $\overline{\text{CAS}}$ low	8		10		12		ns
t_{WRH}	Hold time, $\overline{\text{W}}$ high after $\overline{\text{RAS}}$ low (CBR refresh only)	10		10		10		ns
t_{CHR}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high (CBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high	40		48		58		ns
t_{CSR}	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ low (CBR refresh only)	5		5		5		ns
t_{RAD}	Delay time, $\overline{\text{RAS}}$ low to column address (see Note 10)	10	25	12	30	12	35	ns
t_{RAL}	Delay time, column address to $\overline{\text{RAS}}$ high	25		30		35		ns
t_{CAL}	Delay time, column address to $\overline{\text{CAS}}$ high	18		20		25		ns
t_{RCD}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (see Note 11)	12	37	14	45	14	52	ns
t_{RPC}	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low (CBR only)	5		5		5		ns
t_{RSH}	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ high	8		10		12		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_{T}	Transition time	2	30	2	30	2	30	ns

NOTES:
7. All cycles assume t_T = 2 ns.
8. In a read-write cycle, t_{RWD} and t_{WRL} must be observed.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. The maximum value is specified only to assure access time.
11. Referenced to the later of $\overline{\text{CAS}}$ or $\overline{\text{W}}$ in write operations.

device symbolization

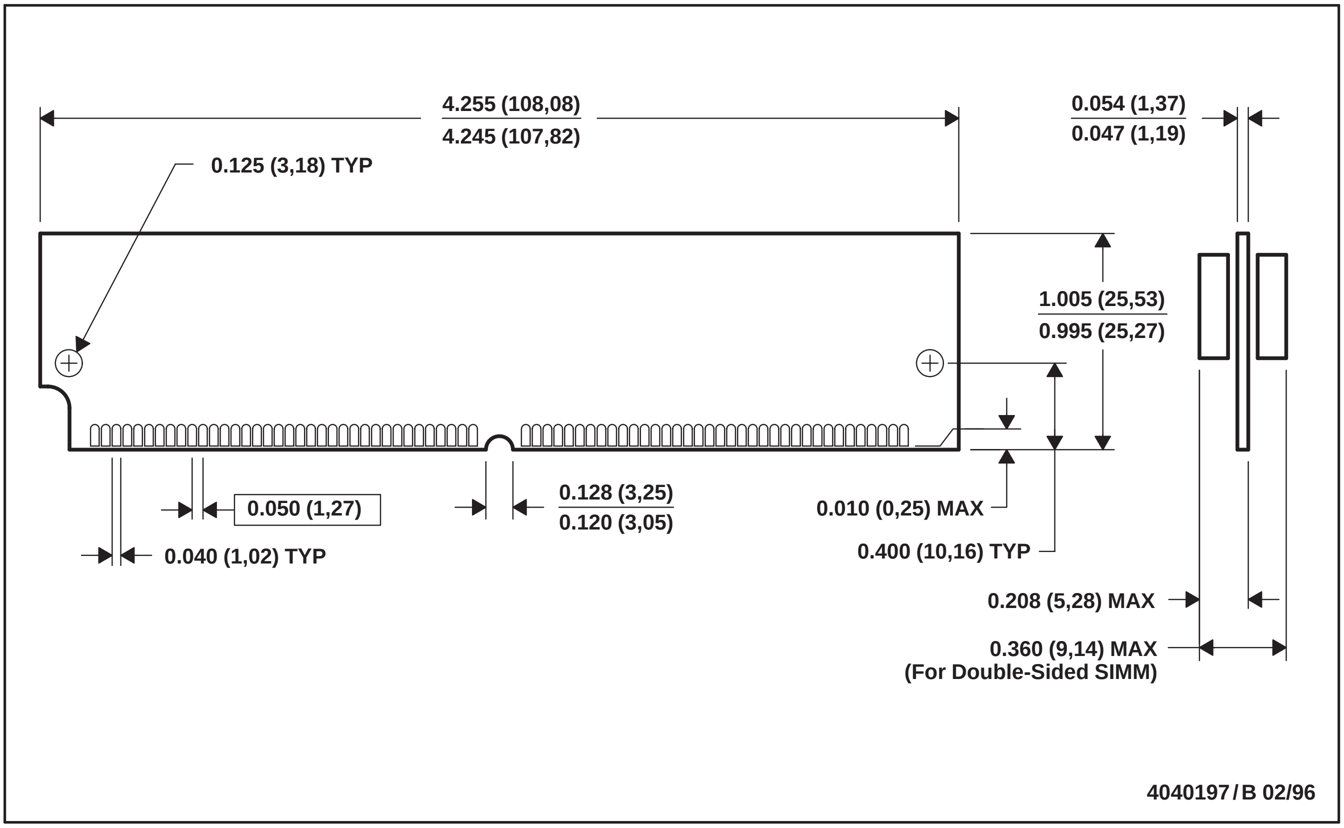


YY = **Year Code**
MM = **Month Code**
T = **Assembly Site Code**
-SS = **Speed Code**

NOTE A: The location of the part number may vary.

MECHANICAL DATA

BK (R-PSIM-N72) **SINGLE-IN-LINE MEMORY MODULE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

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