SPSS028A – MAY 2000 – REVISED JUNE 2000

- **Advanced, Integrated Speech Synthesizer for High-Quality Sound**
- **Operates up to 12.32 MHz (Performs up to 12 MIPS)**
- **Very Low-Power Operation, Ideal for Hand-Held Devices**
- **Low-Voltage Operation, Sustainable by Three (3) Batteries**
- **Reduced Power Standby Modes, Less Than 10 μA in Deep-Sleep Mode**
- **Supports High-Quality Synthesis Algorithms such as MELP, CELP, LPC, FM and ADPCM**
- **Slave Mode Enables Hours of Speech Using an External Processor and Memory**
- **Master Mode Allows 6.8 Mins of Speech Onboard**
- **16 General-Purpose I/O Pins (in Master Mode) or 4 General-Purpose I/O Pins (in Slave Mode)**
- **Resistor-Trimmed Oscillator or 32.768-kHz Crystal Reference Oscillator**
- **Slave Interface Logic**
- **Contains 32K-Words On-Board ROM (2K Words Reserved)**
- **640-Word RAM**
- **Direct Speaker Drive (32 Ω) (PDM)**
- **One-Bit Comparator with Edge Detection Interrupt Service**
- **Serial Scan Port for In-Circuit Emulation, Monitor, and Test**
- **Available in Die Form or 64-Pin PM Package**
- **An Emulator Board (EPC50C604) is Available for Code Development in Slave Mode**

description

The MSP50C604 ('C604) is a low-cost, mixed-signal processor that combines a speech synthesizer with a dedicated slave interface logic, general-purpose I/O, on-board ROM, and direct speaker-drive in a single package. The computational unit uses a powerful new DSP that gives the 'C604 unprecedented speed and computational flexibility compared with previous devices of its type. The 'C604 supports a variety of speech and audio coding algorithms, providing a range of options with respect to speech duration and sound quality.

The device consists of a micro-DSP core, embedded program and data memory, and a self-contained clock generation system. General-purpose periphery is comprised of 16 bits of partially configurable I/O.

The core processor is a general-purpose 16-bit microcontroller with DSP capability. The basic core block includes a computational unit (CU), data address unit, program address unit, two timers, eight-level interrupt processor, and several system and control registers. The core processor gives the 'C604 break-point capability in emulation.

The processor is a Harvard type for efficient DSP algorithm execution, separating program and data memory blocks to permit simultaneous access. The ROM has a protection scheme to prevent third-party pirating. It is configured in 32K 17-bit words.

The total ROM space is divided into two areas: 1) The lower 2K words are reserved by Texas Instruments for a built-in self-test 2) The upper 30K is for user program and data space.

The data memory is internal static RAM. The RAM is configured in 640 17-bit words. All memories are designed to consume minimum power at a given system clock and algorithm acquisition frequency.

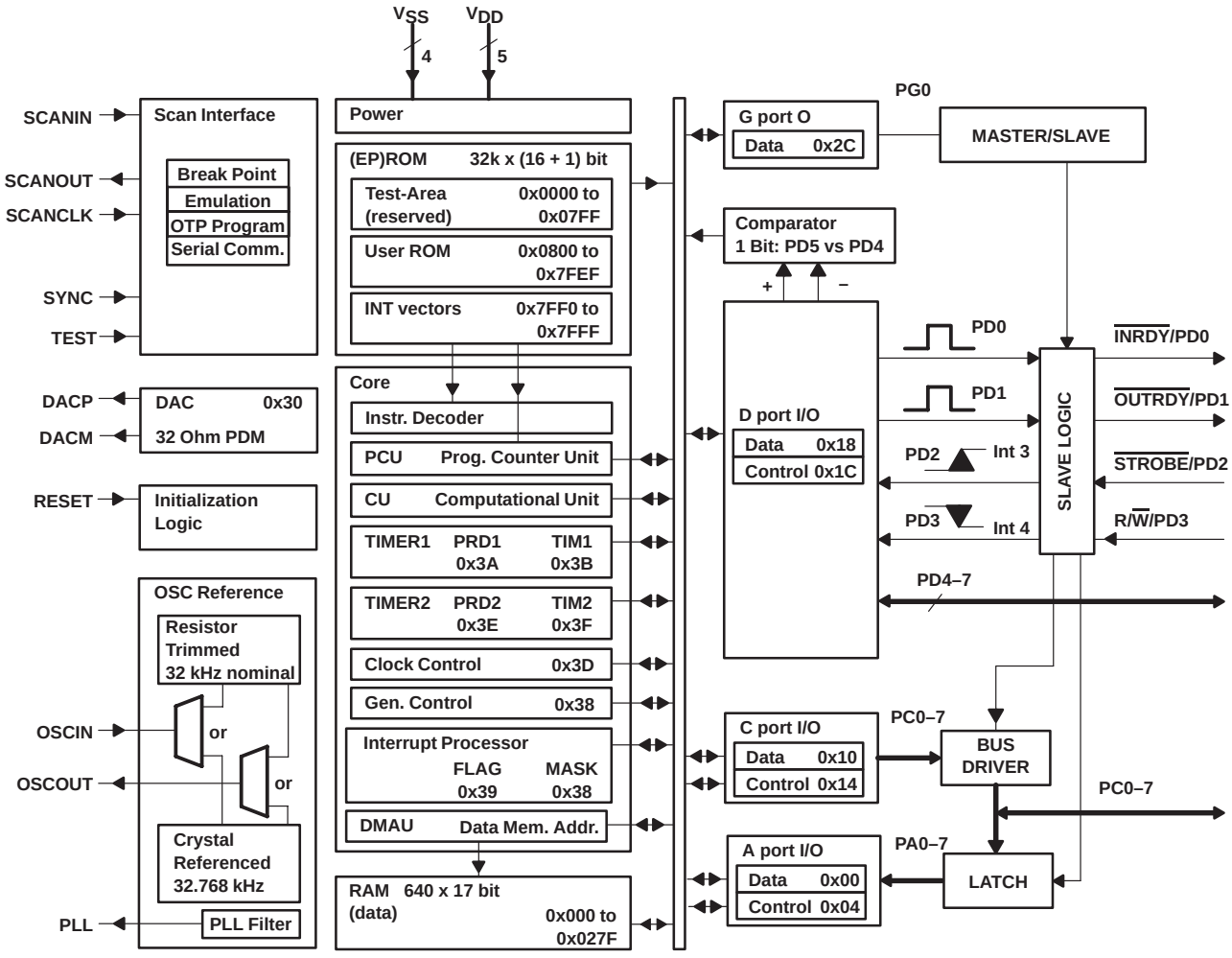
A flexible clock generation system enables the software to control the clock over a wide frequency range. The implementation uses a phase-locked loop (PLL) circuit that drives the processor clock at a selectable frequency between the minimum and maximum achievable. Selectable frequencies for the processor clock are spaced apart in 65.536-kHz steps. The PLL clock-reference is also selectable; either a resistor-trimmed oscillator or a crystal-referenced oscillator may be used. Internal and external clock sources are controlled separately to provide different levels of power management.

description (continued)

The periphery consists of two 8-bit-wide general-purpose I/O ports when operating in master mode, or four general-purpose I/O pins in slave mode. In the master mode, the bidirectional I/O can be configured under software control as either high-impedance inputs or as totem-pole output. They are controlled via addressable I/O registers. These features make the input port especially useful as a key-scan interface. Slave mode consists of four general-purpose I/O, four control pins, and eight bidirectional data pins.

A simple one-bit comparator is also included in the periphery. The comparator is enabled by a control register, and its access is shared with two pins in one general-purpose I/O port. Rounding out the ’C604 periphery is a built-in pulse-density-modulated DAC (digital-to-analog converter) with direct speaker-drive capability. The following block diagram gives an overview of the ’C604 functionality.

functional block diagram



functional description

The ’C604 is a member of the MSP50C6xx family, which is based on the MSP50C614 core. For specific details about the core operations, instruction sets, register definitions, port configuration, etc., please consult the MSP50C614 user’s guide (SPSU014).

The ’C604 can be used as a slave synthesizer in slave mode or can operate stand-alone in master mode. The slave mode activates logic circuitry internal to the device that gives the device a dedicated slave interface. The slave or master mode is controlled by the bit 0 of the Port G (PG0). By default the device initially starts in slave mode. To change to master mode write a 0x01 to G port 0 (0x2C). To change back to slave mode write a 0x00 to port G bit 0 (0x2C).

master mode

In master mode, the slave logic circuitry is disabled and ’C604 has 16 general-purpose I/Os. These 16 input/output pins are organized as 2-byte-wide ports (C and D), initialized as inputs. Each of the pins can be configured as a totem-pole output or as a high-impedance input by setting or clearing the appropriate bit in the appropriate control register (0x14, 0x1C). When configured as an output, the data driven by the output pin can be controlled by setting or clearing the appropriate bit in the appropriate data register (0x10, 0x18). Whether configured as input or as output, reading the data port reads the actual state of the pin.

External interrupts can be caused by transitions on pins PD2, PD3, PD4, and PD5 in the master mode. These interrupts are supported whether the pins are programmed as inputs or outputs.

slave mode

In slave mode, the slave logic circuitry is enabled allowing the device to have a dedicated slave interface. In this mode, only four pins of port D (PD4–PD7) are available as general-purpose I/O while the remaining pins (PD0–PD3) are redefined as $\overline{\text{INRDY}}$, $\overline{\text{OUTRDY}}$, $\overline{\text{STROBE}}$ and R/$\overline{\text{W}}$. These pins are used to operate the slave interface. The ’C604 controls the $\overline{\text{INRDY}}$ and $\overline{\text{OUTRDY}}$ pins to let the external microcontroller know when the slave is ready to accept or transmit data. The external microcontroller controls the R/$\overline{\text{W}}$ and $\overline{\text{STROBE}}$ pins of ’C604 to sequence the read/write data flow. Each read or write sequence generates an interrupt that needs to be serviced by an interrupt service routine. These interrupt service routines need to be written by the code developer. The INT3 interrupt service routine indicates that the host has completed the write sequence, and the slave should read the data from port A. The INT4 interrupt service routine indicates the host has completed the read sequence. An interrupt is not generated when a read/write is done on port G bit 0 (PG0).

The slave interface consists of:

- 8-bit bidirectional data bus (PC0 – PC7)
- 2 status outputs: $\overline{\text{INRDY}}$/PD0, and $\overline{\text{OUTRDY}}$/PD1
- 2 control inputs: $\overline{\text{STROBE}}$/PD2, and R/$\overline{\text{W}}$/PD3
- 4 general-purpose I/Os (PD4–PD7)

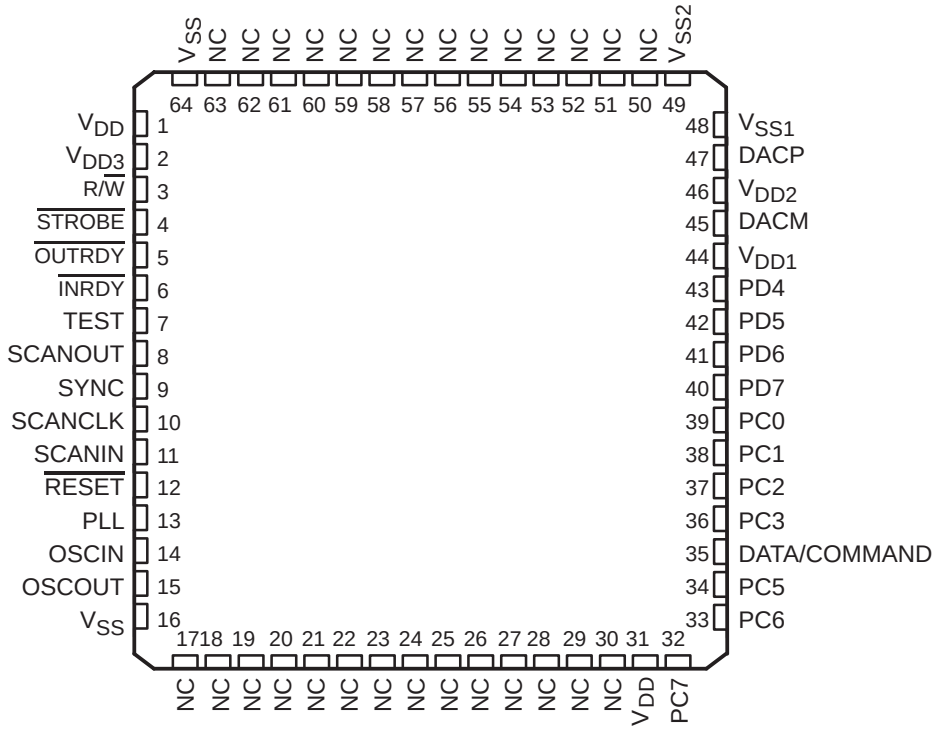
Port C is used as an 8-bit bidirectional data bus. When data is to be sent to the host, it needs to be written to port C data register (0x10). When data is read from the host, it needs to be read from port A data register (0x00). Port A pins are not physically brought outside the device but are internally connected with the pins of port C.

pin assignments

SIGNAL	PIN NUMBER	PAD NUMBER	I/O	DESCRIPTION
Input/Output Ports				
PC0 – PC7	39 → 32	25 → 18	I/O	Port C general-purpose I/O (1 Byte)
PD4– PD7	43 → 40	29 → 26	I/O	Port D general-purpose I/O (1 Nibble)
PD0/$\overline{\text{INRDY}}$	6	6	I/O	(Master) Port D general-purpose I/O
			O	(Slave) $\overline{\text{INRDY}}$ output to host
PD1/$\overline{\text{OUTRDY}}$	5	5	I/O	(Master) Port D general-purpose I/O
			O	(Slave) $\overline{\text{OUTRDY}}$ output to host
PD2/$\overline{\text{STROBE}}$	4	4	I/O	(Master) Port D general-purpose I/O
			I	(Slave) $\overline{\text{STROBE}}$ input from host
PD3/R/$\overline{\text{W}}$	3	3	I/O	(Master) Port D general-purpose I/O
			I	(Slave) Read/$\overline{\text{write}}$ input from host
Pins PD4 and PD5 may be dedicated to the comparator function, if the comparator enable bit is set. Please refer to Section 3.3, *Comparator*, in the MSP50C614 User's Guide (SPSU014) for details.				
Scan Port Control Signals				
SCANIN	11	11	I	Scan port data input
SCANOUT	8	8	O	Scan port data output
SCANCLK	10	10	I	Scan port clock
SYNC	9	9	I	Scan port synchronization
TEST	7	7	I	'C604 test modes
The Scan Port pins must be bonded out on any 'C604 production board. Please consult the *Important Note regarding Scan Port Bond Out*, see Chapter 7 in the MSP50C614 User's Guide (SPSU014).				
Oscillator Reference Signals				
OSCOUT	15	15	O	Resistor/crystal reference out
OSCIN	14	14	I	Resistor/crystal reference in
PLL	13	13	O	Phase-lock-loop filter
DAC Sound Output				
DACP	47	33	O	Digital-to-analog output 1 (+)
DACM	45	31	O	Digital-to-analog output 2 (–)
Initialization				
$\overline{\text{RESET}}$	12	12	I	Initialization
Power Signals†				
V_{SS}	16, 48, 49†, 64	16, 34†, 35, 36		Ground
V_{DD}	1, 2, 31, 44, 46†	1, 2, 17, 30, 32†		Processor power (+)
† V_{SS} and V_{DD} connections service the DAC circuitry. Their pins tend to sustain a higher current draw. A dedicated decoupling capacitor across these pins is therefore required.				

pin assignments

PM PACKAGE
(TOP VIEW)



system initialization sequence in the slave mode

- Initialize the host processor first.
- The host must hold the slave $\overline{\text{RESET}}$ pin low until the slave $\overline{\text{STROBE}}$ pin can be held high by the host throughout the slave initialization process.

The $\overline{\text{INRDY}}$ and $\overline{\text{OUTRDY}}$ pins are set high by the slave on the rising edge of the slave $\overline{\text{RESET}}$ pin.

slave mode software initialization

- Write 0x00 to port A (0x00), port C (0x10), port D (0x18) data registers.
- Configure the port C (PC0–PC7), port D0, and port D1 as output ports. (Write 0xFF to port C (0x14) and 0x03 to port D (0x1C) control registers)
- Configure port A (PA0–PA7), PORT D2, and port D3 as input ports (default at reset). Write 0x00 to port A (0x04) and 0x03 to port D (0x1C) control registers.
- After the slave completes its initialization, the slave needs to inform the host that it is ready to read or write data.

NOTE:
The default mode for the MSP50C604 is the slave mode. The ’C604 can be set to master mode by writing a 1 to port G bit 0. This is an internal bit that is not available on the ’C604 external pins.

NOTE:
The initialization sequence given previously is a specific requirement for setting up the ’C604 in slave mode. For the basic initialization requirements of the device, please refer to the MSP50C614 user’s guide (SPSU014).

write to slave in the slave mode

- The slave indicates it is ready to receive data from the host by dropping $\overline{\text{INRDY}}$ low. This is done by writing low-high-low to port D (0x18) bit 0 (PD0).
- On the falling edge of the internal PD0 pulse, $\overline{\text{INRDY}}$ toggles low, notifying the host that the slave is ready to receive data.
- The host writes data to the slave by setting R/$\overline{\text{W}}$ low and then pulsing the $\overline{\text{STROBE}}$ high-low-high.
- The slave latches the data on the rising edge of the $\overline{\text{STROBE}}$ pulse and sets $\overline{\text{INRDY}}$ high.
- An INT3 interrupt is generated as $\overline{\text{INRDY}}$ goes high completing the write cycle.
- The latched data is read by the slave through port A (0x00) data register.

read from slave in the slave mode

- When the slave has data for the host, it places the data in port C (0x10).
- The slave then indicates that the data is ready by dropping $\overline{\text{OUTRDY}}$ low. This is done by writing low-high-low to port D (0x18) bit 1 (PD1).
- On the falling edge of the internal PD1 pulse, $\overline{\text{OUTRDY}}$ toggles low notifying the host that the slave is ready to send data.
- The host responds by setting R/$\overline{\text{W}}$ high and then pulsing $\overline{\text{STROBE}}$ high-low-high.
- The host should latch the data before raising $\overline{\text{STROBE}}$ high.
- This informs the slave that the data has been written to the host. The $\overline{\text{OUTRDY}}$ is pulled high by the slave at the rising edge of $\overline{\text{STROBE}}$.
- An INT4 interrupt is generated as $\overline{\text{OUTRDY}}$ goes high completing the read cycle.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . –0.3 to 7 V
Supply current, I_{DD} (see Note 2) . . . . . 35 mA
Input voltage range, V_I (see Note 1) . . . . . –0.3 to V_{DD} + 0.3 V
Output voltage range, V_O (see Note 1) . . . . . –0.3 to V_{DD} + 0.3 V
Storage temperature range, T_A . . . . . –30°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Unless otherwise noted, all voltages are measured with respect to V_{SS} .
2. The total supply current includes the current out of all the I/O pins as well as the operating current of the device.

recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{DD}	Supply voltage (with respect to V_{SS})		3.0	5.2	V
V_{IH}	High-level input voltage	V_{DD} = 3 V	2	3.3	V
		V_{DD} = 4.5 V	3	4.8	
		V_{DD} = 5.2 V	3.5	5.2	
V_{IL}	Low-level input voltage	V_{DD} = 3 V	0	1	V
		V_{DD} = 4.5 V	0	1.5	
		V_{DD} = 5.2 V	0	1.7	
I_{OH}‡	High-level output current (per pin of I/O port)	V_{DD} = 4.5 V, V_{OH} = 4 V		–2	mA
I_{OL}‡	Low-level output current (per pin of I/O port)	V_{DD} = 4.5 V, V_{OL} = 0.5 V		5	mA
$I_{OH(DAC)}$	High-level output DAC current	V_{DD} = 4.5 V, V_{OH} = 4 V		–10	mA
$I_{OL(DAC)}$	Low-level output DAC current	V_{DD} = 4.5 V, V_{OL} = 0.5 V		20	mA
$f_{(CPU)}$	CPU clock rate (as programmed)		64	12,320	kHz
$R_{(DAC)}$	Resistance between DACP and DACM		32		Ω
T_A	Operating free-air temperature	Device functionality	0	70	°C

‡ This parameter cannot exceed 15 mA total per internal V_{DD} pin. Port C and port D share 1 internal V_{DD}. Ports A and G0 are used internally.

dc electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
RESET	Threshold changes	V_{DD} = 3 V	Positive going threshold		2.4		V
			Negative going threshold		1.8		
			Hysteresis		0.6		
		V_{DD} = 5.2 V	Positive going threshold		3.3		V
			Negative going threshold		2.9		
			Hysteresis		0.4		
I_{lkg}	Input leakage current	Excludes OSC_{IN}				1	µA
$I_{(STANDBY)}$	Standby current	RESET is low			0.05	10	µA
I_{DD}†	Operating current	V_{DD} = 4.5 V,	F_{CLOCK} = 12.32 MHz		15		mA
$I_{(SLEEP–deep)}$	Supply current	V_{DD} = 4.5 V,	DAC off, ARM set, OSC disabled		0.05	10	µA
$I_{(SLEEP–mid)}$		V_{DD} = 4.5 V,	DAC off, ARM set, OSC enabled		40	60	
$I_{(SLEEP–light)}$		V_{DD} = 4.5 V,	DAC off, ARM clear, OSC enabled		60	100	
V_{IO}	Input offset voltage	V_{DD} = 4.5 V,	Vref = 1 to 4.25 V		25	50	mV
$R_{(PULLUP)}$	F port pullup resistance	V_{DD} = 5 V		70	150		kΩ
$\Delta f_{(RTO–trim)}$	Trim deviation	R_{RTO} = 470 kΩ, V_{DD} = 4.5 V, T_A = 25°C, f_{RTO} = 8.192 MHz (PLL setting = 7 Ch)‡			±2	±3	%
$\Delta f_{(RTO–volt)}$	Voltage deviation	R_{RTO} = 470 kΩ, V_{DD} = 3.5 to 5.2 V, T_A = 25°C, f_{RTO} = 8.192 MHz (PLL setting = 7 Ch)‡				±1.5	%/V
$\Delta f_{(RTO–temp)}$	Temperature deviation	R_{RTO} = 470 kΩ, V_{DD} = 4.5 V, T_A = 0 to 70°C, f_{RTO} = 8.192 MHz (PLL setting = 7 Ch)‡		–0.1		0.1	%/°C
$\Delta f_{(RTO–res)}$	Resistance deviation	V_{DD} = 4.5 V,	T_A = 25°C, R_{OSC} = 470 kΩ @ ±1%, f_{RTO} = 8.192 MHz (PLL setting = 7 Ch)‡		±1		%/R

† Operating current assumes all inputs are tied to either V_{SS} or V_{DD} with no input currents due to programmed pullup resistors. The DAC output and other outputs are open circuited.

‡ The best trim value is selected at nominal temperature and voltage but the deviation due to the trim error is ignored.

external component absolute values

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$R_{(RTO)}$	RTO external resistance	T_A = 25°C,	1% tolerance		470	kΩ
$C_{(PLL)}$	PLL external capacitance	T_A = 25°C,	10% tolerance		3300	pF

timing requirements

PARAMETER		MIN	MAX	UNIT
$t_{(RESET)}$	Reset pulsed low, while 'C604 has power applied	100		ns
$t1_{(WIDTH)}$	Pulse width required prior to a negative transition at pin (PD3, PD5, or PF0...PF7 interrupt)	2		$1/F_{CPU}$
$t2_{(WIDTH)}$	Pulse width required prior to a positive transition at pin (PD2 or PD4 interrupt)	2		$1/F_{CPU}$

Figure 1. Initialization Timing Diagram

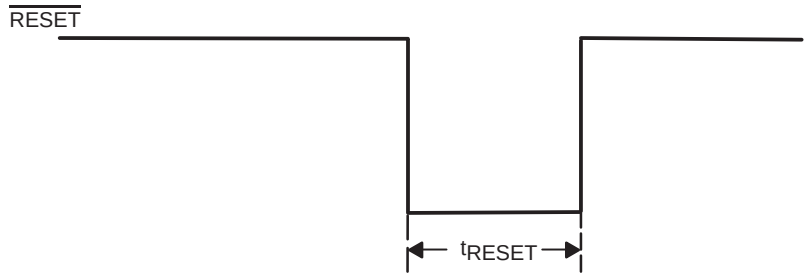
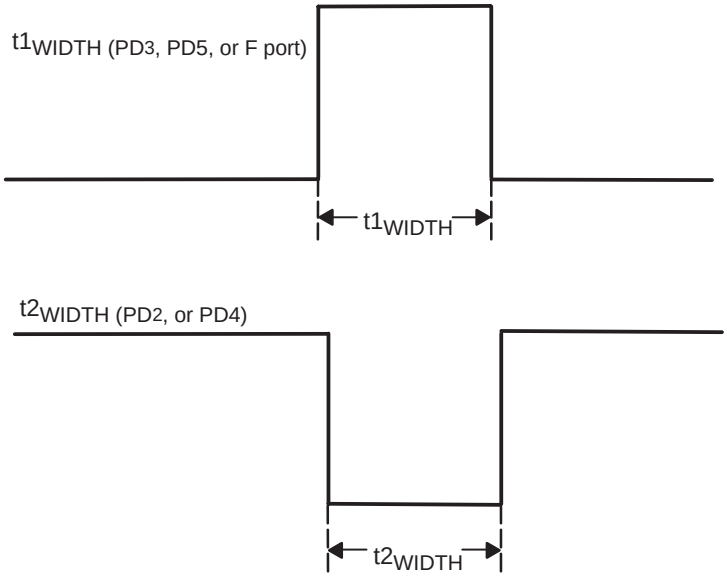
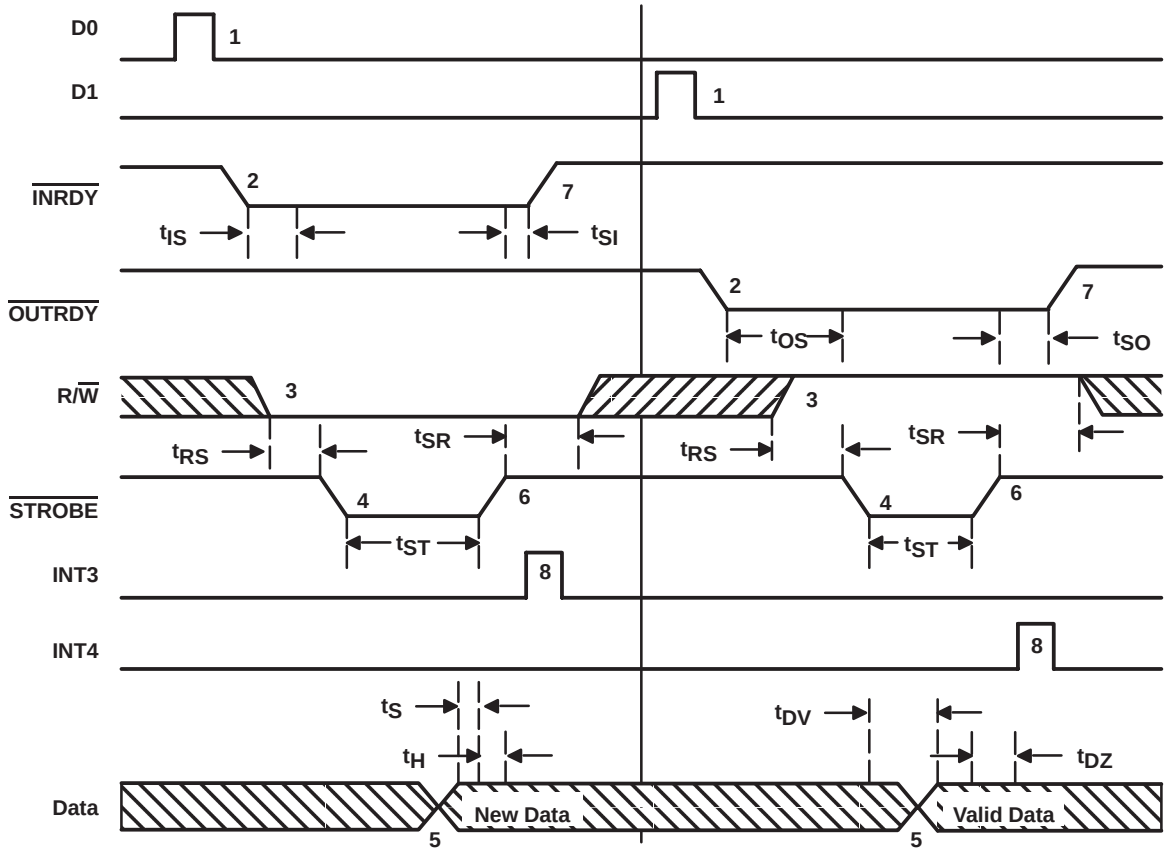


Figure 2. MSP50P604 External Interrupt Pin Pulse Width Requirements $t1_{WIDTH}$ and $t2_{WIDTH}$



timing diagram



Write to Slave

1. Slave signals readiness to receive data from host.
2. Slave drops $\overline{\text{INRDY}}$.
3. Host drops R/$\overline{\text{W}}$ to indicate a write.
4. Host drops $\overline{\text{STROBE}}$.
5. Host places data on the bus.
6. Host raises $\overline{\text{STROBE}}$ indicating data is valid.
7. Slave raises $\overline{\text{INRDY}}$, latching the data.
8. INT3 is triggered when $\overline{\text{INRDY}}$ rises.

Read from Slave

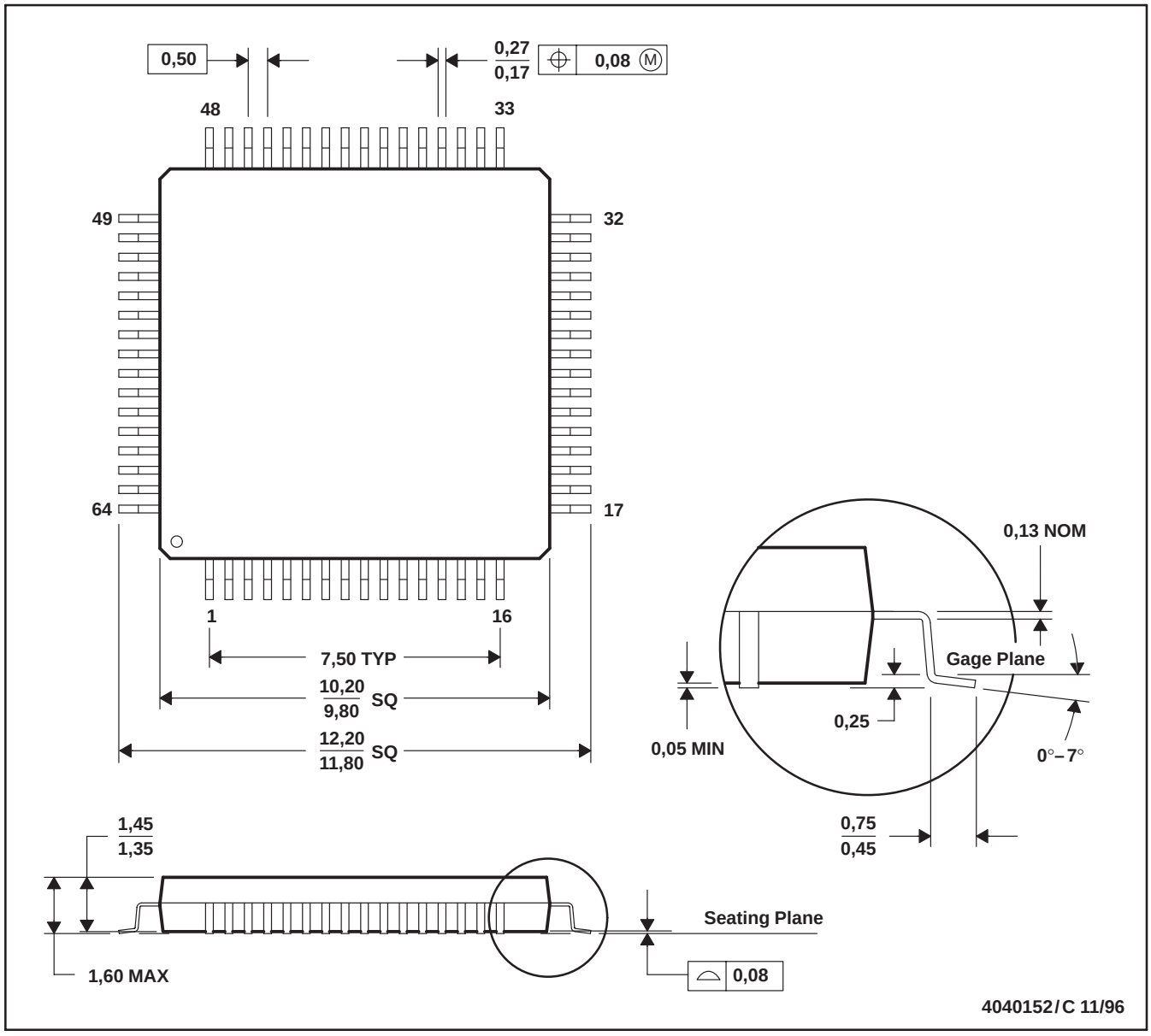
1. Slave signals readiness to send data to host.
2. Slave drops $\overline{\text{OUTRDY}}$.
3. Host raises R/$\overline{\text{W}}$ to indicate a read.
4. Host drops $\overline{\text{STROBE}}$.
5. Slave places data on the bus.
6. Host raises $\overline{\text{STROBE}}$ after reading the data.
7. Slave raises $\overline{\text{OUTRDY}}$.
8. INT4 is triggered when $\overline{\text{OUTRDY}}$ rises.

Table 1. Timing Constrains

Write to Slave		Read from Slave	
$\overline{\text{INRDY}}$ low to $\overline{\text{STROBE}}$ low	$t_{IS\ (min)}$ = 5 ns	$\overline{\text{OUTRDY}}$ low to $\overline{\text{STROBE}}$ low	$t_{OS\ (min)}$ = 5 ns
R/$\overline{\text{W}}$ to $\overline{\text{STROBE}}$ low	$t_{RS\ (min)}$ = 75 ns	R/$\overline{\text{W}}$ to $\overline{\text{STROBE}}$ low	$t_{RS\ (min)}$ = 75 ns
$\overline{\text{STROBE}}$ low	$t_{ST\ (min)}$ = 100 ns	$\overline{\text{STROBE}}$ low	$t_{ST\ (min)}$ = 100 ns
$\overline{\text{STROBE}}$ high to R/$\overline{\text{W}}$	$t_{SR\ (min)}$ = 25 ns	$\overline{\text{STROBE}}$ high to R/$\overline{\text{W}}$	$t_{SR\ (min)}$ = 25 ns
$\overline{\text{STROBE}}$ high to $\overline{\text{INRDY}}$ high	$t_{SI\ (max)}$ = 75 ns	$\overline{\text{STROBE}}$ high to $\overline{\text{OUTRDY}}$ high	$t_{SO\ (max)}$ = 75 ns
Data setup	$t_{S\ (min)}$ = 15 ns	$\overline{\text{STROBE}}$ Low to data valid	$t_{DV\ (max)}$ = 90 ns
Data hold	$t_{H\ (min)}$ = 80 ns	$\overline{\text{STROBE}}$ High to data high Z	$t_{DZ\ (min)}$ = 90 ns

MECHANICAL DATA

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

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