VOICE SYNTHESIS LSI T6803

1. General Description

The T6083 is a single chip PARCOR voice synthesis LSI with a built-in voice data ROM (64K bits) and low-pass filter circuit.

2. Featrures

- o PARCOR system 10 kHz sampling voice output.
- o Built-in 64K bits ROM for voice data.
- o The dedicated ROM can be externally connected. (Max. 2M bits)
- o Max. 63 speech phrases are selectable.
  (64 or more phrases can be specified when a microcomputer is connected.)
- o Various bit rates are selectable according to quality of sound (9.8, 5.6 and 2.5 Kbps).
- o 3 steps of speech speed can be changed over.
- o Built-in butterworth three stage low-pass filter.
- o 5V single power supply.
- o Low current consumption by C-MOS process (2mA when a low-pass filter is used.)
- o Power standby mode available (3 μA).

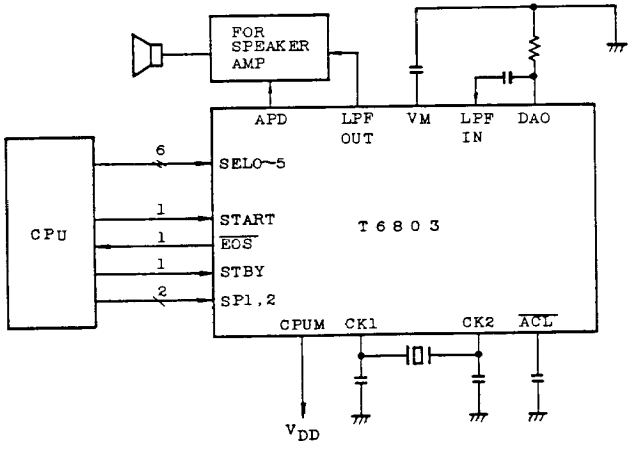
* PARCOR is the voice analysing and synthesizing method depend by Nippon Telegram and Telephone Public Corporation (NTT). Toshiba's voice synthesizing LSI has been developed under the direction of NTT. Patent Nos. are No.754418, 876024 and 1045100.

3. Examples of Voice Synthesizing System Configuration

When a voice synthesizing system is composed using the T6803, there are two types of configuration; CPU control type using a microcomputer, etc. and manual control type using SW, etc. In both types, connection of dedicated mask ROM is possible. Refer to (3).

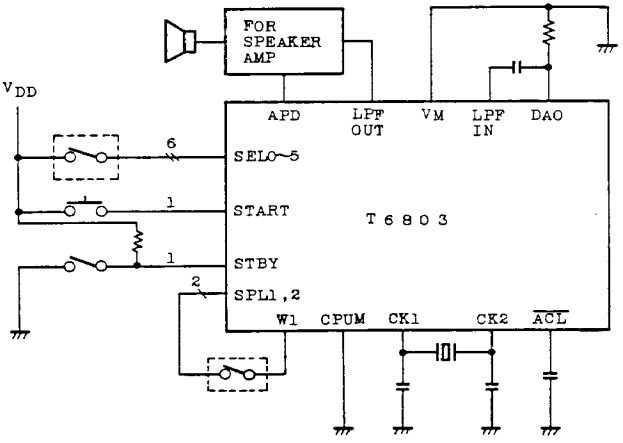
(1) CPU control type

The basic configuration is the 2 chips configuration of CPU + T6803.



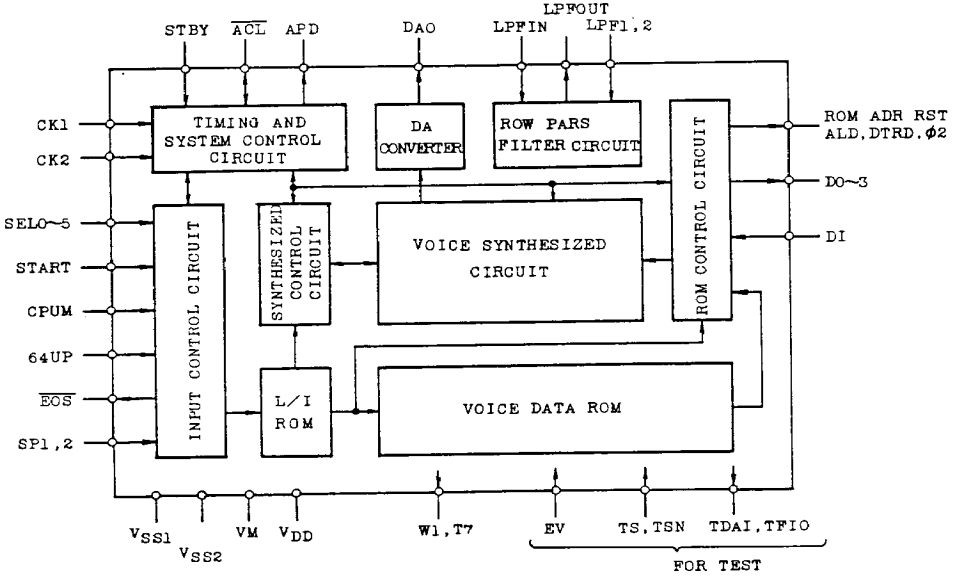
(2) Manual control type

The configuration is a minimum system and the 1 chip configuration of T6803.



4. LSI's Specifications

(1) Block Diagram



(2) Specifications for voice synthesizer

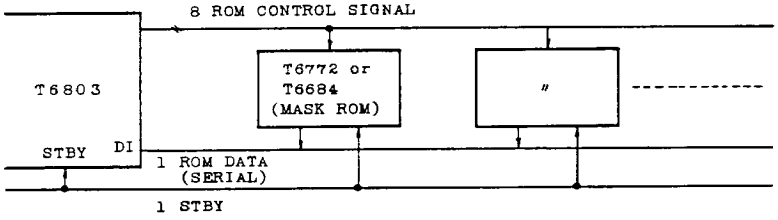
System	PARCOR
Number of arithmetic bits	15 bits
Sampling frequency	10 kHz
Interpalating calculation	Available
Frame length	10 mS/20 mS

(Selectable for every phrase .... L/I ROM)

Since the T6803 has the built-in filter circuit, voice can be output only when a speaker and speaker driving amplyfier are externally mounted to the voice output system.

When the capacity (64K bits) of built-in ROM of the T6803 is insufficient in (1) and (2), it is possible to expand the capacity by externally mounted ROM.

(3) Expansion of capacity by dedicated MASK ROM



T6772 : 64K bit dedicated mask ROM for voice
(connectable up to max. 8 pieces)

T6684 : 128K bit dedicated mask ROM for voice
(connectable up to max. 16 pieces)

Bit/frame	50 bit/56 bit/98 bit (selectable for every phrase .. L/I ROM)
Sound source	2 kinds (" ")
Number of filter stages	8 stages/10 stages (" ")
Synthesized sound	Melody/voice (" ")
DA converter	9 bits voltage type

(3) Specifications for low-pass filter

Type	Butterworth
No. of filter orders	3 stage of LPF
Filter characteristic	2 kinds (set up through the external terminal)
Cut off frequency	2 kinds (")
Circuit system	Switched capacitor

(4) L/I (LABEL/INDEX) ROM

L/I ROM is a ROM used to set up actual start address of DATA ROM, synthesizing conditions, and internal/external ROM designation, corresponding to phrase code (LABEL) selected by SEL0 to 5 terminals, and the following data are internally set up automatically in the indirect designation mode (64UP = "L"):

Address		20 bits
Synthesizing conditions		Following 5 data can be set up:
	① Frame length	(10ms or 20ms)
	② Bits/frame	(98 or 56 or 50)
	③ Voice source	(A or B)
	④ Filter stage	(10 or 8)
	⑤ Melody	(Melody or voice)
ROM designation		Built-in/externally mounted ROM

The above-mentioned INDEX data can be designated to all combinations of SEL0 to 5 terminals (max. 63 ... 1 to 63 except 0).

(5) Vioce data ROM

PARCOR analyzed voice data (64K bits) have been set.

[Note] L/I ROM and voice data ROM are MASK ROMs and contents desired by user will be incorporated at time of development.

5. Operational Description

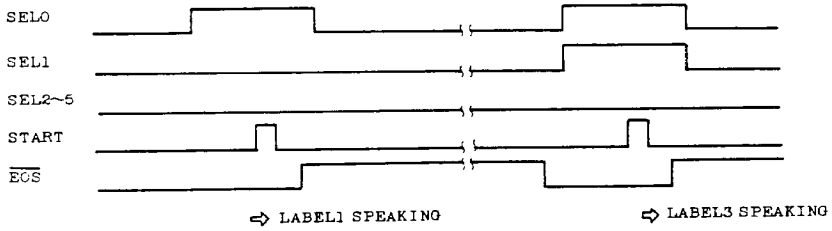
(1) Speaking phrase setting and speaking start instruction

There are two methods available for setting speaking phrases and directing start of speaking.

1 Indirect setting (64UP = "L" level)

o This is a method to use L/I ROM which is provide in the T6803. speaking phrases are set by combinatin of SEL0 to 5 (1 - 63) terminals and when the speaking start instruction START is input, the speaking of set phrases is started.

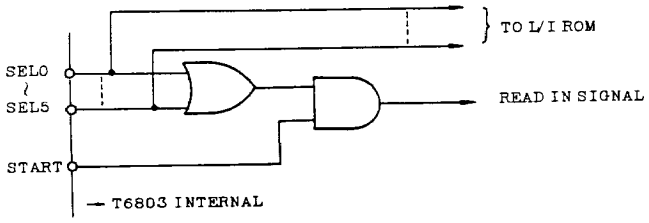
[Example 1] The speakings of LABEL 1 and LABEL 3



o There is the $\overline{EOS}$ terminal for an output signal to monitor whether this LSI is speaking or the speaking ended. This $\overline{EOS}$ terminal becoems "H" level when the speaking START signal is input and becomes "L" level when the speaking ends.

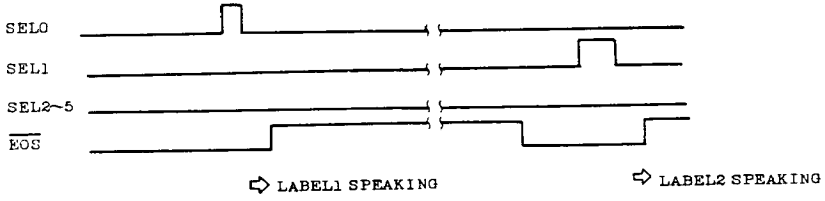
o SEL0 to 5 and START input of T6803 are as illustrated below. It is possible to make the speaking using only one of the SEL0 to 5 with the START terminal set at "H" level.

[Input]



[Example 2]

Pharase setting by SEL0 to 5 and speaking start (START input = "H" level)



o Example 1 is valid when SEL0 to 5 data lines are used commonly together with other peripheral devices, while in Example 2, SEL0 to 5 become the exclusive use data lines but it is possible to reduce number of lines to be connected by one line if the START terminal is set at "H" level when connecting to CPU.

2 Direct setting (64UP = "H" level)

o If number of phrases is over 63 phrases, it becomes possible to directly set synthesizing conditions and start address when the 64 UP terminal is set at "H" level.

- In case of the direct setting, data are set at the SEL0 to 3 terminals and written T6803 by the START signal, and types of data to be transferred (synthesizing conditions, start address, forced stop) are designated by the SEL4 and SEL5 terminals.

- Combinations are as shown in the following tables:

SEL4	SEL5	Kinds of Data	SEL3	SEL2	SEL1	SEL0
0	0	Start address	MSB			LSB
1	0	Synthesizing conditions 1	Voice source	ROM Designation	Melody	Bit/ Frame(1)
0	1	Synthesizing conditions 2	Bit/ Frame (2)	Frame length	0	Filter stages
1	1	Forced stop	*	*	*	*

1 : "H" Level

0 : "L" Level

* : Don't care

Data / Input Pin	0	1
SEL0	98 bit	98 bit
SEL1	Voice source	Melody
SEL2	Built-in ROM	External ROM
SEL3	Voice source A	Voice source B

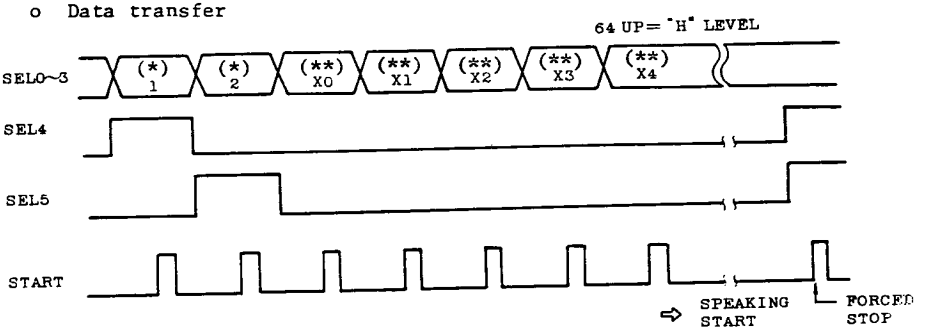
Synthesizing condition 1

Data / Input Pin	0	1
SEL0	10 stages	8 stages
SEL1		
SEL2	20 ms	10 ms
SEL3	56 bit	50 bit

Synthesizing condition 2

* When 98 bit is designated in Bit/Frame (1), Bit/Frame (2) (50/56) becomes invalid.

o Data transfer



(*): Synthesizing condition (**): Address

o Either synthesizing condition 1 or 2 can be first set. In addition, when synthesizing conditions were set several times, the conditions that have been finally set become valid.

o When transferring address data, divide 4-bit data into 5 times and transfer them from X_0 to X_4 successively. If synthesizing condition have been set during transfer of address data, after the forced stop, transfer address data again from the first.

o The synthesizing conditions are initialized (the state where synthesizing condition data become zero) at time of ACL or STBY. Except ACL and STBY, they are held until they are written again (including the indirect setting).

o Speaking is automatically made after 5 times of address transfer.

- o The forced stop can be input in any state.
- o Addresses X_0 to X_4 correspond to DATA ROM addresses as follows:

DATA ROM Address	A_{19}~A_{16}	A_{15}~A_{12}	A_{11}~A_8	A_7 ~ A_4	A_3	A_2	A_1	A_0
SEL0 ~ 3	Same as right	Same as right	Same as right	Same as right	SEL3	SEL2	SEL1	SEL0
X_0 ~ 4	X4	X3	X2	X1	X0			

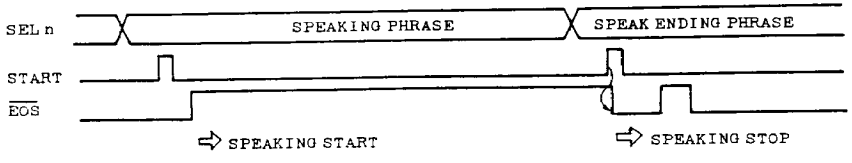
(2) Forced stop of speaking

There are 3 methods to stop voice speaking by force.

1 Forced stop at time of indirect setting (64 UP = "L" level)

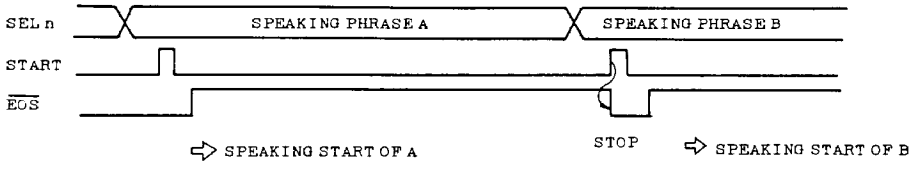
- o It is possible to switch speaking phrases by force.

Therefore, when the speaking end phrase is set at one of 63 LABELS, it is possible to effect the forced stop by inputting this LABEL.



Further, the forced change of a speaking phrase is possible by starting a desired phrase.

Change speaking prase A with B



2 Forced stop at time of direct setting (64 UP = "H" level)

- o As described in the above (2)-2 , the forced stop of speaking at time of the direct setting is possible when SEL4 and SEL5 are set at "H" level and the START signal is input.

- o As the forced change of a speaking phrase in the direct setting mode is impossible, to make the speaking phrase change, once perform the forced stop and then, start the speaking.

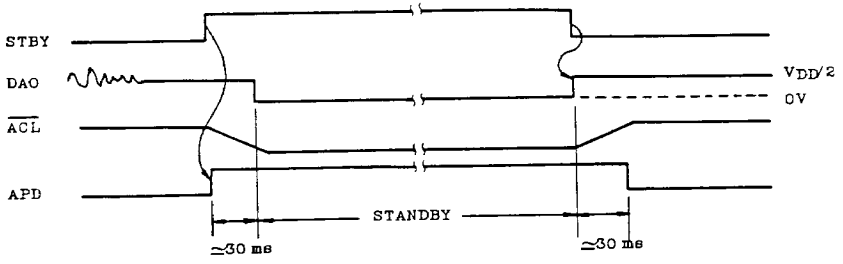
3 Speaking stop by $\overline{ACL}$ input

The $\overline{ACL}$ terminal is a terminal used to initialize the T6803 system at time of POWER ON by a capacitor connected to this terminal and an internally provided resistor. The T6803 is also initialized when a "L" level signal is input to this terminal from the outside. It is therefore possible to stop the speaking by inputting a "L" level signal to this terminal during the speaking.

(3) Standby operation

o The T6803 has the standby function. When a "H" level signal is input to the STBY terminal, the T6803 is put in the standby mode, which can be released by inputting a "L" level signal.

o The T6803 outputs APD (Audio Power Down) signal to control POWER ON/OFF of an external audio circuit, interlocking with the standby mode. This signal is set at "H" level in the standby mode and at "L" level when the standby mode is released.



o APD output becomes "H" level at the same time when STBY input becomes "H" level, but DAO output becomes "L" level ≈ 30ms later.

Further, DAO output becomes $V_{DD}/2$ level at the same time when STBY input becomes "L" level, but APD output becomes "L" level ≈ 30 ms later.

o $\overline{ACL}$ input becomes "L" level in the standby mode.

- As the T6803 is initialized for 30ms after the standby mode is released, no external control is accepted during this period.

Note: When a pul-down resistor is provided in SEL0 to 5 and START input terminals by mask option, SEL0 to 5 and START input terminals should be set at OPEN or GND level in the standby mode.

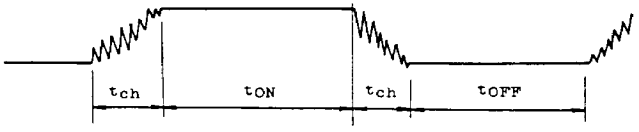
(4) Chattering preventing circuit

- In the manual control mode (CPUM = "L" level), the chattering preventing circuit is actuated to prevent malfunction of the switches connected to the START input and SEL0 to 5 terminals.

  The chattering preventing time is about 20ms and when the switches are stably kept at "H" level for about 60ms after they are depressed, the speaking is started.

  If the switches are onced released and depressed again, they should be kept at "L" level stably for about 60ms.

Switch input



- In the CPU control mode (CPUM= "H" level), the chattering preventing circuit is not actuated, enabling the pulse operation.

(5) Speech speed

Speech speed is changable by setting SP1 or SP2.

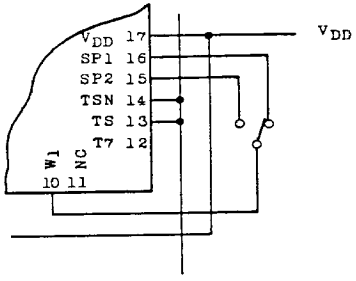
Slow speed = 1.24 × normal speed.

Fast speed = 0.76 × normal speed.

a) manual control

	slow	normal	fast
SP1	W1	open	open
SP2	open	open	W1

Note: SP1 and SP2 is built-in pull down register by mask option.



b) CPU control

	slow	normal	fast
SP1	V_{DD}	GND	GND
SP2	GND	GND	V_{DD}

Note: SP1 and SP2 is not built-in pull down registor by mask option.

6. Low-pass Filter

The T6803 has built-in butterworth three stage low- pass filters used by the latest switched capacitor technology and it is possible to output synthesized sound by connecting a speaker amplifier circuit externally.

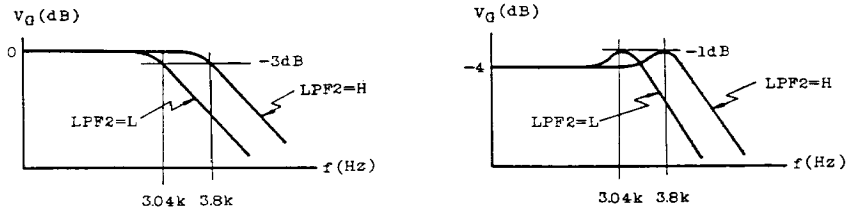
(1) Filter characteristic selecting function

The filter built in the T6803 have four kinds of characteristics. Any one of the characteristcs can be selected by setting LPF1 and LPF2 terminals.

LPF1 : Filter shape change-over terminal

LPF2 : Cut-off frequency change-over terminal

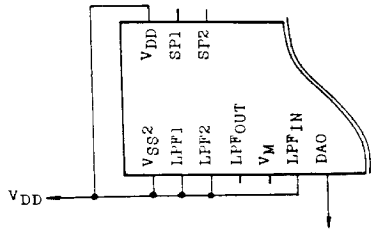
Filter type-1 (LPF1="L" level) Filter type-2 (LPF1="H" level)



(The cut-off frequency shown is a value when oscillation frequency of T6803 is 800 kHz.)

(2) When no built-in filter is used

Since the power supply ($V_{SS}2$) for the low-pass filters built-in the T6803 separated from the power supply ($V_{SS}1$) for the digital synthesizer, when a filter circuit is connected extermely as illustrated below, it becomes possible to save power of the built-in low-pass filters.



With LPF1 LPF2, LPF_{IN} and $V_{SS}2$ connected to V_{DD}, open LPF_{OUT} and V_M.

(It is not feasible to save power of the digital synthesizer and use the low-pass filters only.)

7. Pin Description & Pin Connection

(1) Pin Description

PIN NAME	PIN NO.		CONFIGURATION		DESCRIPTION
	DIP 42 PIN	MFP 44 PIN	I/O	PULL-UP/ -DOWN RESISTOR	
V_{SS2}	1	18	(*)	-	0V
LPF2	2	19	Input	without	Change-over input of low-pass filter characteristic
LPF1	3	20			
LPF OUT	4	21	Output	-	Low-pass filter output
VM	5	22	Output		Reference voltage output for low-pass filter
LPF IN	6	23	Input	without	Low-pass filter input
DA0	7	24	DAC Output	-	D/A converter output
APD	8	25	Output	-	Power down output for external audio circuit
TDAI	9	26	Input	without	Test input
TFIO	10	27	Output	-	Test output
ø2	11	28	Output	-	Clock pulse to external ROM
EV	12	29	Input	Pull-down	Input terminal for test
ROMADR RST	13	30	Output	-	Address reset output to external ROM
ALD	14	31			Start address set pulse to "
DI	15	32	Input	Pull-up	Data input from external ROM
DTRD	16	33	Output	-	Data read pulse from external ROM
D3	17	34			Address data output from external ROM
D2	18	35			
D1	19	36			
D0	20	37			
V_{SS1}	21	38	(*)	-	0V
SEL0	22	40	Input		Phrase selection input
SEL1	23	41			
SEL2	24	42			
SEL3	25	43			
SEL4	26	44			
SEL5	27	1			

(*): Power Supply

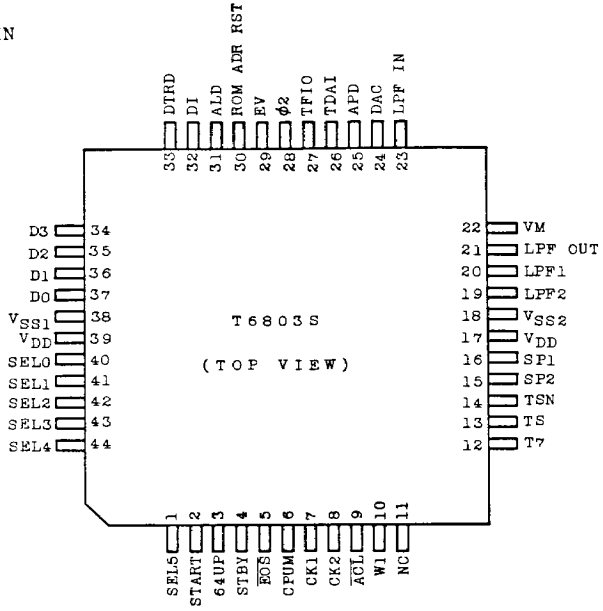
PIN NAME	PIN NO.		CONFIGIRATION		DESCRIPTION
	DIP 42 PIN	MFP 44 PIN	I/O	PULL-UP/ -DOWN RESISTOR	
START	28	2	Input	*	Speaking start instruction input
64 UP	29	3		without	Direct/indirect designation mode change-over input
STBY	30	4			Power down input
$\overline{EOS}$	31	5	Output	-	END OF SPEECH Output
CPUM	32	6	Input	without	Chattering prevention YES/NO change-over input
CK1	33	7	Input	without	Ceramic vibrator connecting pin
CK2	34	8	Output	-	
$\overline{ACL}$	35	9	I/O	-	Power ON auto clear, Schmitt input
W1	36	10	Output	-	Timing signal output
T7	37	12			Test output
TS	38	13	Input	Pull-down	Test input
TSN	39	14			
SP2	40	15	Input	*	Speaking speed change-over input
SP1	41	16			
VDD	42	17, 39	Power supply	-	+5V

* Pull-down resistor Yes/No can be designated by the mask option.

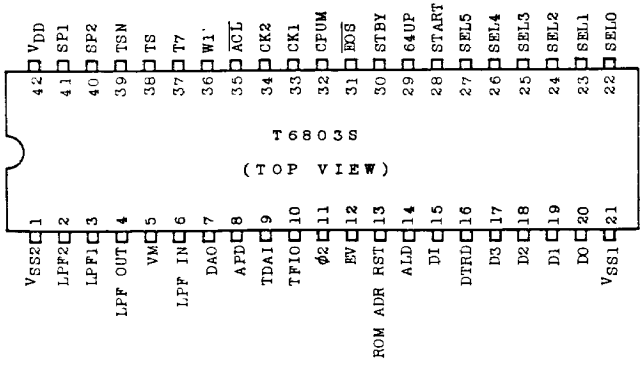
Option Designation	START, SEL0 ~ 5	SP1, 2
No designation	No	No
Option 1	No	Pull-down
Option 2	Pull-down	No
Option 3	Pull-down	Pull-down

(2) PIN CONNECTION

1 MFP 44 PIN



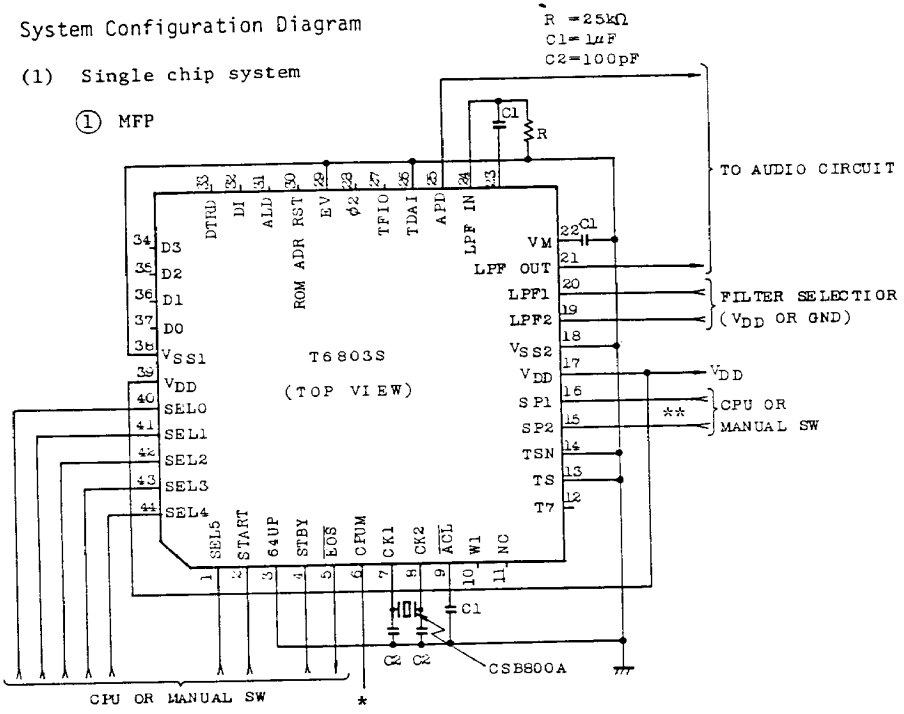
2 DIP 42 PIN



8. System Configuration Diagram

(1) Single chip system

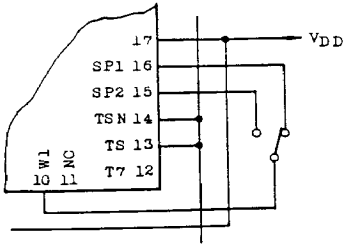
① MFP



* Connect to V_{DD} when the system is connected to CPU, and connect to GND when connected to MANUAL SW.

** Speed change-over can be also set externally.

(Example)

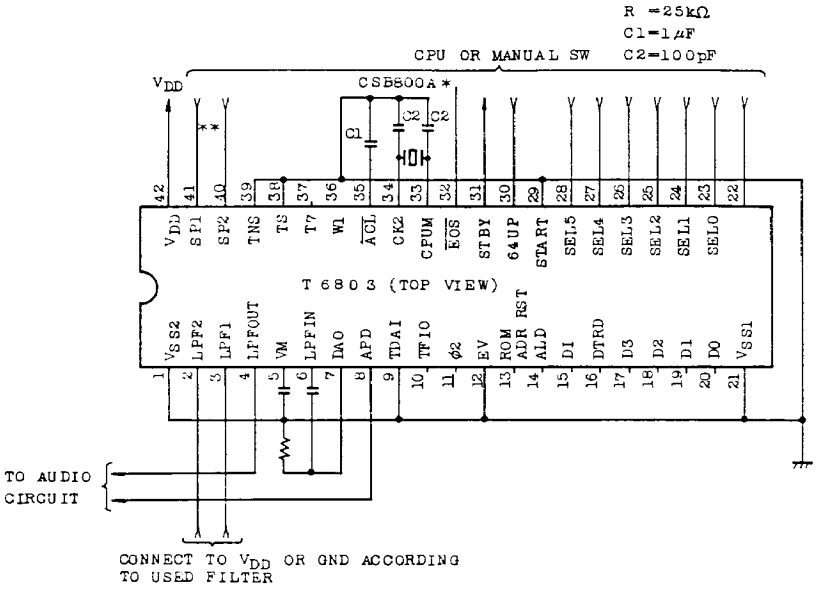


(When the pull-down resistor is available by the mask option.)

Note 1. Position the ceramic vibrator and capacitor, which are to be connected to CK1 and CK2 terminals of T6803 at locations very close to CK1 and CK2.

2. Do not use terminals as a reley terminal except NC terminal.

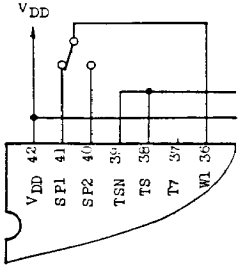
② DIP



* Connect to V_{DD} when the system is connected to CPU, and connect to GND when connected to MANUAL SW.

** Speed change-over can be also set externally.

(Example)



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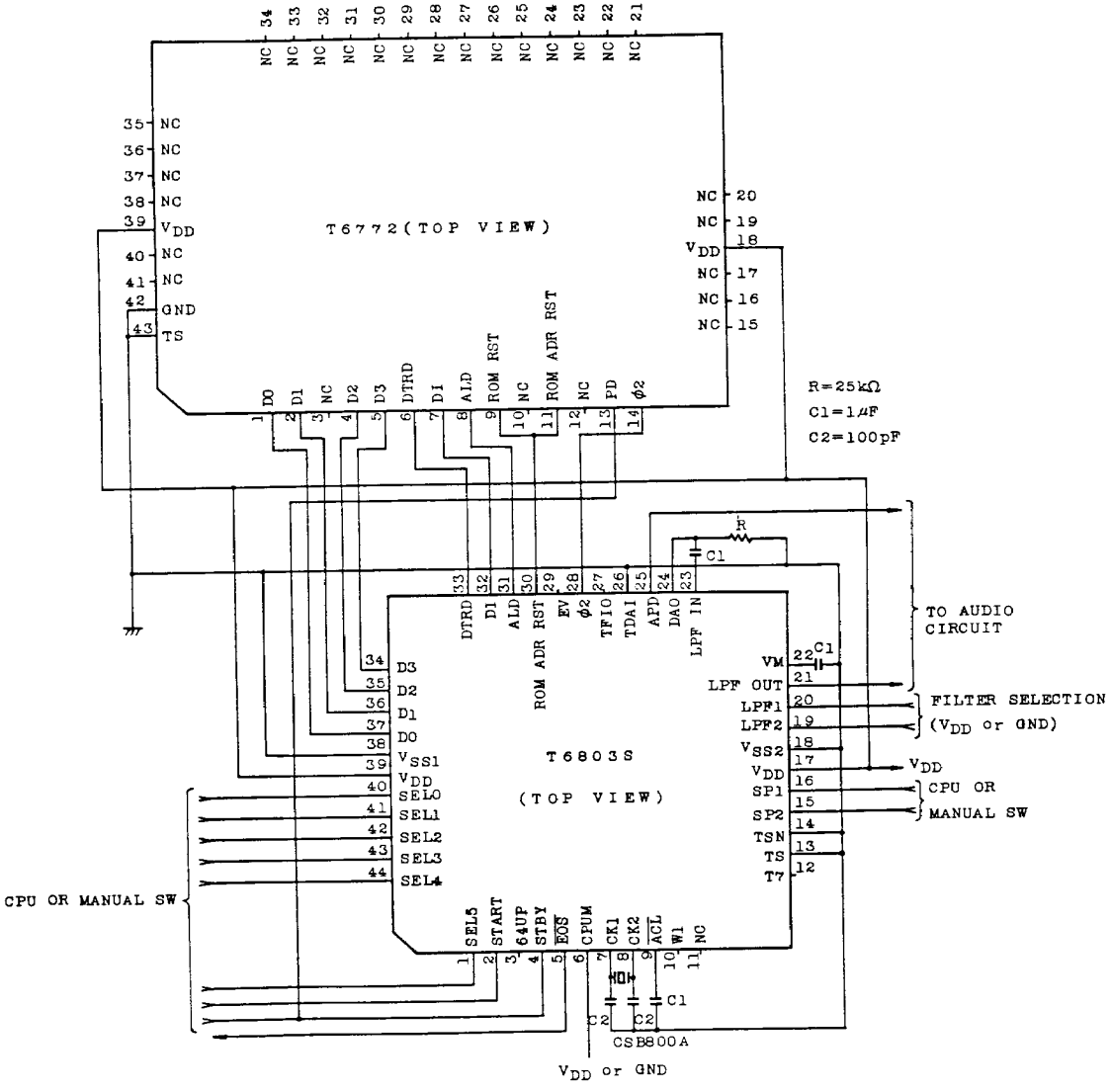
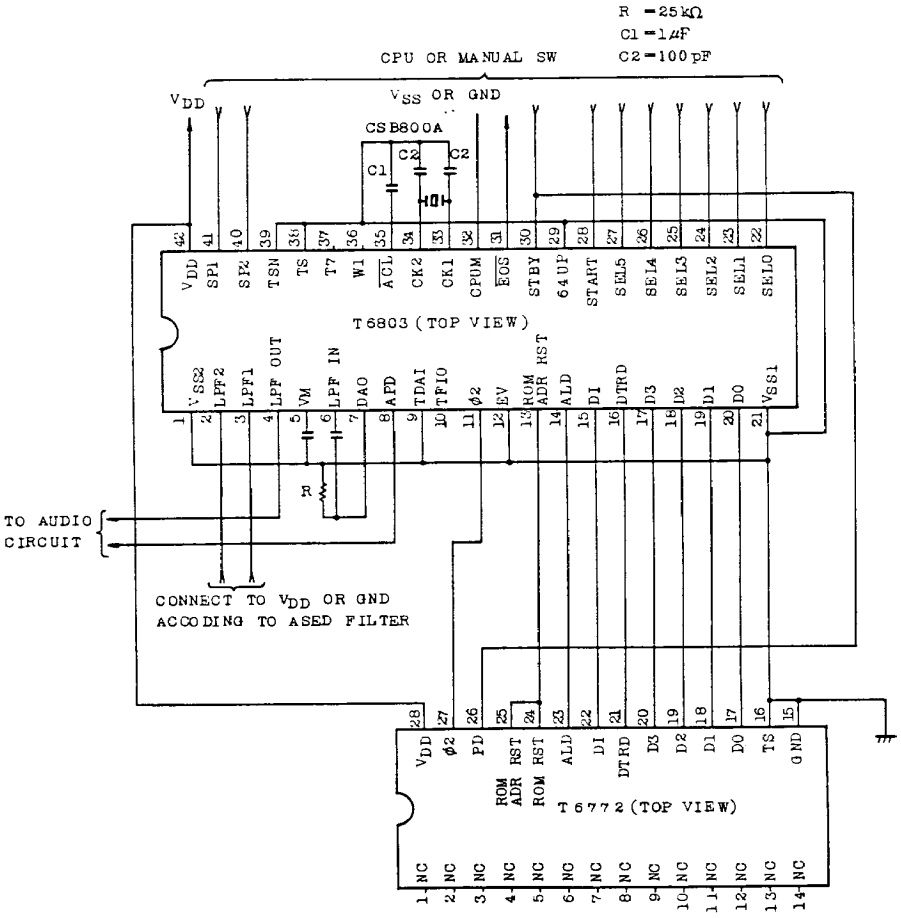
(2) ROM Expansion System

1 MFP

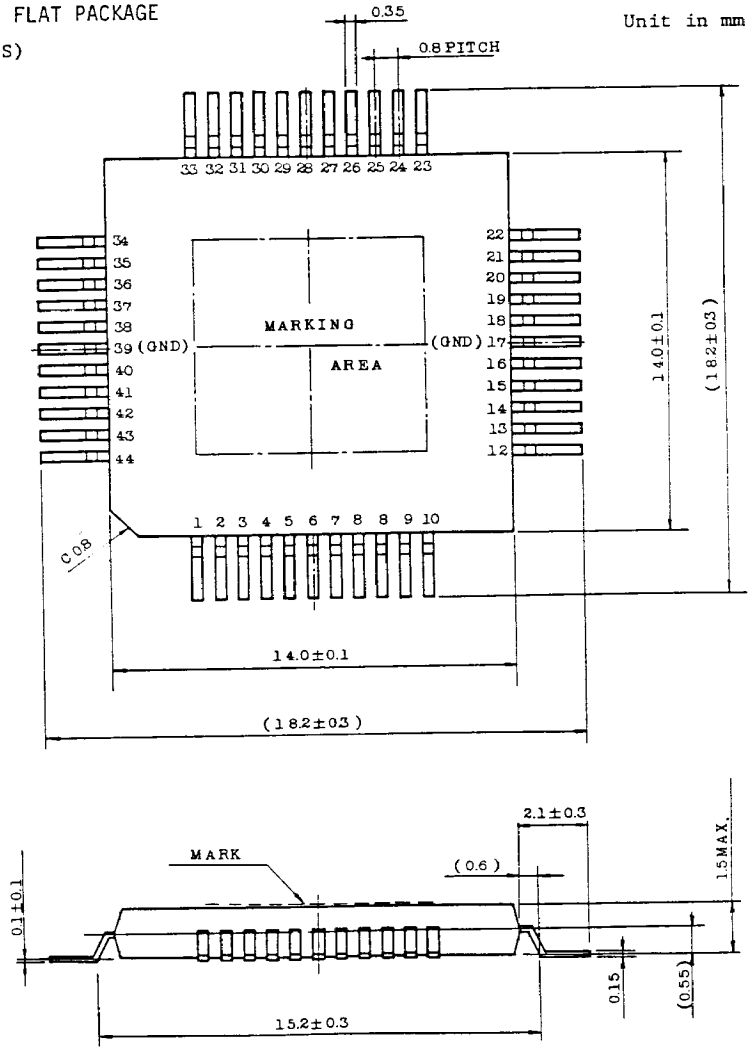


② DIP

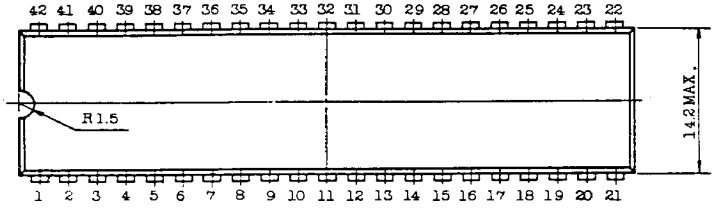


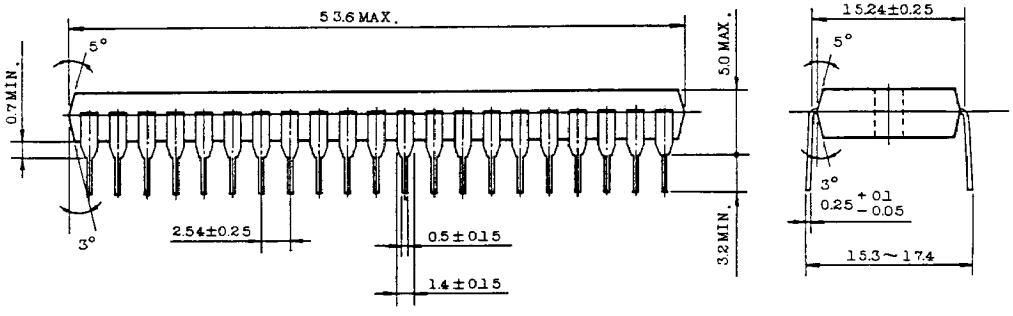
44 PIN MINI FLAT PACKAGE
(MFP 44-4 BS)

Unit in mm



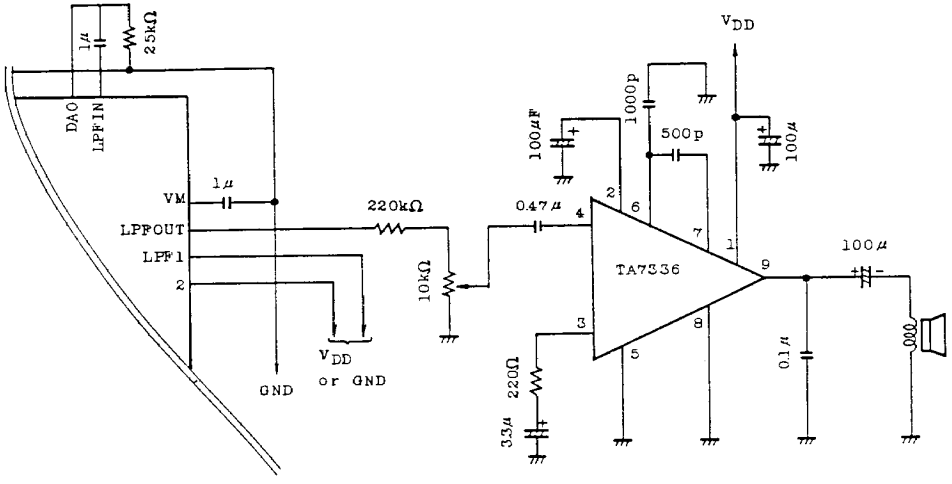
Unit in mm





(Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.42 leads.

9. APPLICATION OF AUDIO CIRCUIT



10. ELECTRICAL CHARACTERISTICS

(1) ABSOLUTE MAXIMUM RATINGS (V_{SS1}=V_{SS2}=0V)

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Supply Voltage	V_{SS}-0.3 ∿ V_{SS}+6.0	V
V_{IN}	Input Voltage	V_{SS}-0.3 ∿ V_{DD}+0.3	V
V_{OUT}	Ouptut Voltage	V_{SS}-0.3 ∿ V_{DD}+0.3	V
T_{stg}	Storage Temperature	-55 ∿ 125	°C
T_{opr}	Operating Temperature	-10 ∿ 55	°C
T_{sol}	Lead Temperature 10 sec	260	°C

(2) DC CHARACTERISTICS (V_{SS1}=V_{SS2}=0V, V_{DD}=5V, Ta=25°C Unless otherwise specified limit value MIN. and MAX. values are defined by their absolute values.)

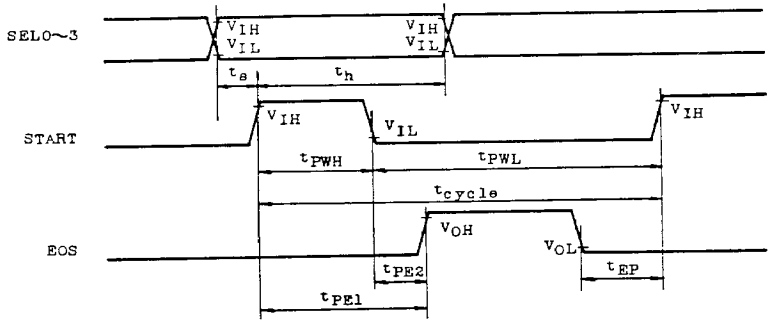
SYMBOL	PARAMETER	APPLIED TERMINAL	CONDITIONS	LIMITS			UNIT
				MIN.	TYP.	MAX.	
V_{DD}	Supply Voltage	V_{DD}	-	3.9	5	5.7	V
$I_{DDO(1)}$	Supply Current (1)	V_{DD}	V_{DD}=5V	-	1.2	2.7	mA
$I_{DDO(2)}$ *1	Supply Current (2)	V_{DD}	V_{DD}=5V	-	0.7	1.5	mA
I_{DDS}	Supply Current during power down	V_{DD}	V_{DD}=5V	-	-	3	μA
f_{OSC}	Frequency range	CK1	V_{DD}=3.9 ∿ 5.7V	760	800	840	kHz
V_{IH}	High level input voltage	Except $\overline{ACL}$, LPFIN	V_{DD}=3.9 ∿ 5.7V	V_{DD}-0.8	-	V	V
V_{IL}	Low level input voltage	Except $\overline{ACL}$, LPFIN	V_{DD}=3.9 ∿ 5.7V	0	-	0.8	V
$R_{PD(1)}$	Pull down registor(1)	SP1, SP2 *2	-	-	500	-	kΩ
$R_{PD(2)}$	Pull down registor(2)	SEL0 ∿ 5, START *2	-	-	30	-	kΩ
R_{PU}	Pull up registor	DI	-	-	500	-	kΩ
I_{IH}	High level input current	Except TS, TSN, EV *3	V_{IN}=V_{DD}	-	-	5	μA
I_{IL}	Low level input current	-	V_{IN}=0V	-	-	-5	μA
I_{OH}	High level output current	Except DA0, $\overline{ACL}$, LPFOUT CK2	V_{OUT}=V_{DD}-0.4V	-0.4	-	-	mA
I_{OL}	Low level output current	"	V_{OUT}=0.4V	0.4	-	-	mA
V_{OUT}	D/A converter output voltage	DA0	No load	0	-	V_{DD}	V
R_{OUT}	D/A converter impedance	DA0		35	50	65	kΩ

*1 Condition of low pass filter is not active. (V_{SS2}=V_{DD})
*2 Apply only pull down registor is built-in.
*3 Apply only pull down registor is not built-in.

(3) AC CHARACTERISTICS (V_{SS1}=V_{SS2}=0V, V_{DD}=5V, C_L=15pF, Ta=-10 ∿ 55°C)
Unless otherwise CPUM=High level, 64UP=Low level)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{PWH}	High level START pulse width		4			μs
t_{PWL}	Low level START pulse width	64UP="H"	24			μs
t_{cycle}	START cycle time	64UP="H"	32			μs
t_s	Data set up time	-	2			μs
t_h	Data hold time	-	2			μs
		64UP="H"	18			μs
t_{PE1}	EOS Delay time (1)		-	-	2	ms
t_{PE2}	EOS Delay time (2)		-	-	2	ms
t_{EP}	START set up time		0	-	-	ms

SWITCHING CHARACTERISTICS TEST WAVEFORM (CPUM="H")



(4) ANALOG CHARACTERISTICS (Unless otherwise V_{SS1}=V_{SS2}=0V, V_{DD}=5V, Ta=25°C)

SYMBOL	PARAMETER	Applied Terminal	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{IN}	Range of input voltage	LPF IN	V_{DD}=3.9 ∿ 5.7V	1.2	-	V_{DD}-1.2	V
V_{OUT}	Output voltage	LPF OUT	"	1.2	-	V_{DD}-1.2	V
V_G	Voltage gain	-	LPF1="L", 1Hz ∿ 1kHz	-0.5	0	+0.5	dB
		-	LPF1="H", 1Hz ∿ 1kHz	-4.5	-4	-3.5	dB
f_c	Cutoff frequency	-	LPF2="L"	2.88	3.04	3.20	kH
		-	LPF2="H"	3.6	3.8	4.0	kH
THD	Total harmonic distortion	-	V_{IN}=1 Vp-p	-	-	1.0	%
R_{IN}	Input registance	LPF IN		1.0	4.0	-	MΩ
R_{OUT}	Output registance	LPF OUT		-	1.0	1.5	kΩ

MEASUREMENT CIRCUIT

V_{IN}, V_{OUT}, fc, THD