

MOS FIELD EFFECT TRANSISTOR

2SK2413

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK2413 is N-Channel MOS Field Effect Transistor designed for high speed switching applications.

FEATURES

- Low On-Resistance
 $R_{DS(on)1} = 70 \text{ m}\Omega \text{ MAX. (@ } V_{GS} = 10 \text{ V, } I_D = 5.0 \text{ A)}$
 $R_{DS(on)2} = 95 \text{ m}\Omega \text{ MAX. (@ } V_{GS} = 4 \text{ V, } I_D = 5.0 \text{ A)}$
- Low C_{iss} $C_{iss} = 860 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diodes
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

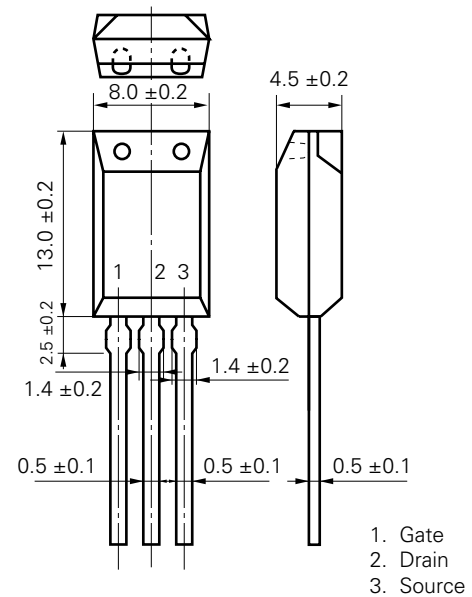
ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 10	A
Drain Current (pulse)*	$I_{D(pulse)}$	± 40	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_T	1.8	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Current**	I_{AS}	10	A
Single Avalanche Energy**	E_{AS}	10	mJ

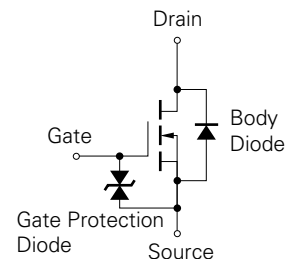
* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

** Starting $T_{ch} = 25^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0$

PACKAGE DIMENSIONS (in millimeter)



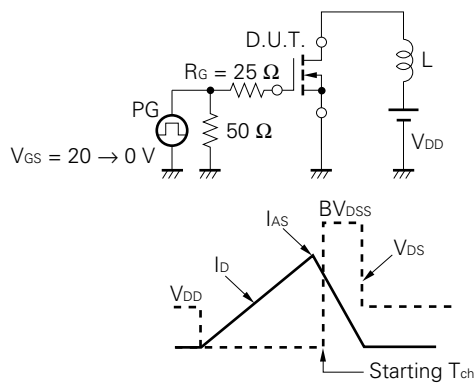
MP-10 (ISOLATED TO-220)



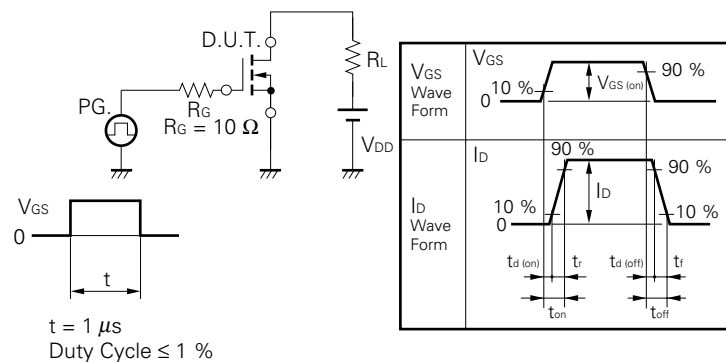
ELECTRICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	$R_{DS(on)1}$		50	70	$m\Omega$	$V_{GS} = 10\text{ V}$, $I_D = 5.0\text{ A}$
Drain to Source On-Resistance	$R_{DS(on)2}$		70	95	$m\Omega$	$V_{GS} = 4\text{ V}$, $I_D = 5.0\text{ A}$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	1.0	1.6	2.0	V	$V_{DS} = 10\text{ V}$, $I_D = 1\text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	7.0	12		S	$V_{DS} = 10\text{ V}$, $I_D = 5.0\text{ A}$
Drain Leakage Current	I_{BSS}			± 10	μA	$V_{DS} = 60\text{ V}$, $V_{GS} = 0$
Gate to Source Leakage Current	I_{GSS}			± 10	μA	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0$
Input Capacitance	C_{iss}		860		pF	$V_{DS} = 10\text{ V}$
Output Capacitance	C_{oss}		440		pF	$V_{GS} = 0$
Reverse Transfer Capacitance	C_{rss}		110		pF	$f = 1\text{ MHz}$
Turn-On Delay Time	$t_{d(on)}$		15		ns	$I_D = 5.0\text{ A}$
Rise Time	t_r		90		ns	$V_{GS(on)} = 10\text{ V}$
Turn-Off Delay Time	$t_{d(off)}$		75		ns	$V_{DD} = 30\text{ V}$
Fall Time	t_f		30		ns	$R_G = 10\text{ }\Omega$
Total Gate Charge	Q_G		24		nC	$I_D = 20\text{ A}$
Gate to Source Charge	Q_{GS}		3.0		nC	$V_{DD} = 48\text{ V}$
Gate to Drain Charge	Q_{GD}		6.0		nC	$V_{GS} = 10\text{ V}$
Body Diode Forward Voltage	$V_{F(S-D)}$		1.0		V	$I_F = 10\text{ A}$, $V_{GS} = 0$
Reverse Recovery Time	t_{rr}		95		ns	$I_F = 10\text{ A}$, $V_{GS} = 0$
Reverse Recovery Charge	Q_{rr}		250		nC	$di/dt = 100\text{ A}/\mu\text{s}$

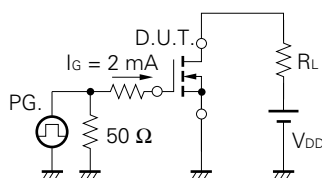
Test Circuit 1 Avalanche Capability



Test Circuit 2 Switching Time

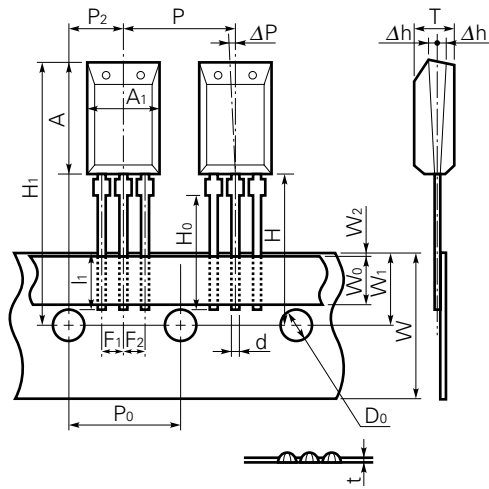


Test Circuit 3 Gate Charge



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

Radial Tape Specification

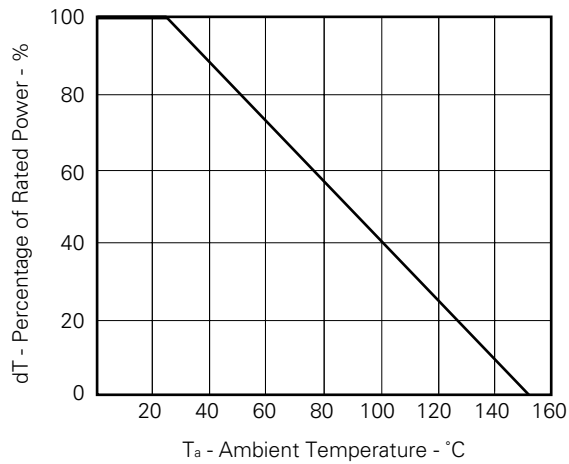


Dimension (unit: mm)

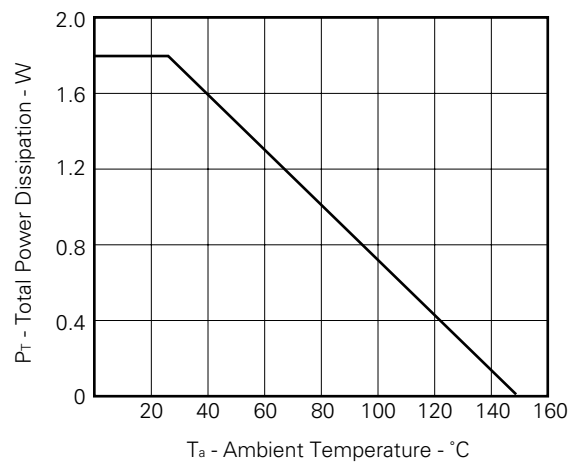
Item		
Component Body Length along Tape	A ₁	8.0 ± 0.2
Component Body Height	A	13.0 ± 0.2
Component Body Width	T	4.5 ± 0.2
Component Lead Width Dimension	d	0.5 ± 0.1
Lead Wire Enclosure	l ₁	2.5 MIN.
Component Center Pitch	P	12.7 ± 1.0
Feedhole Pitch	P ₀	12.7 ± 0.3
Feedhole Center to Center Lead	P ₂	6.35 ± 0.5
Component Lead Pitch	F ₁ , F ₂	2.5 ^{+0.4} _{-0.1}
Deflection Front or Rear	Δh	±1.0
Deflection Left or Right	ΔP	±1.3
Carrier Strip Width	W	18.0 ^{+1.0} _{-0.5}
Adhesive Tape Width	W ₀	5.0 MIN.
Feedhole Location	W ₁	9.0 ± 0.5
Adhesive Tape Position	W ₂	0.7 MIN.
Height of Seating Plane	H ₀	16.0 ± 0.5
Feedhole to upper of Component	H ₁	32.2 MAX.
Feedhole to Bottom of Component	H	20.0 MAX.
Tape Feedhole Diameter	D ₀	4.0 ± 0.2
Overall Taped Package Thickness	t	0.7 ± 0.2

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$)

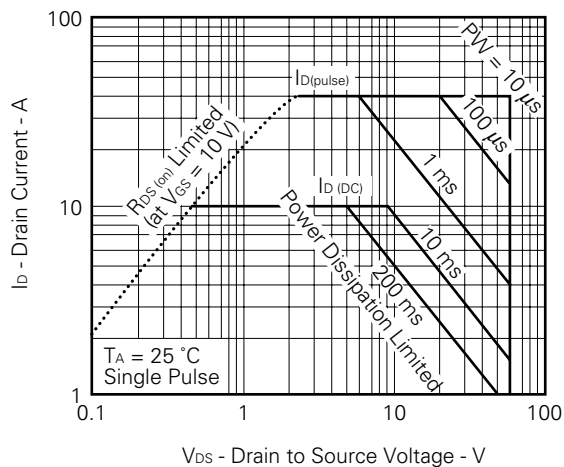
DERATING FACTOR OF FORWARD BIAS
SAFE OPERATING AREA



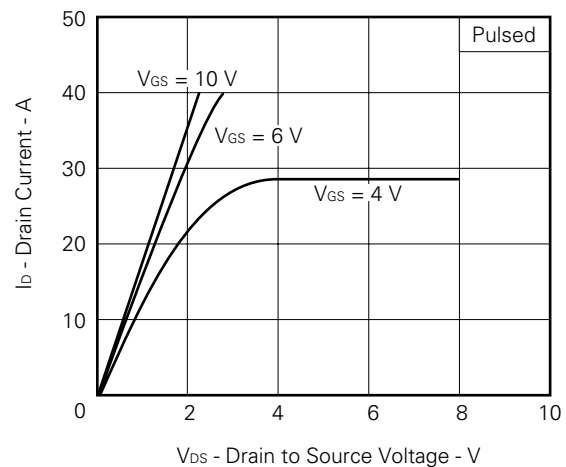
TOTAL POWER DISSIPATION vs.
AMBIENT TEMPERATURE



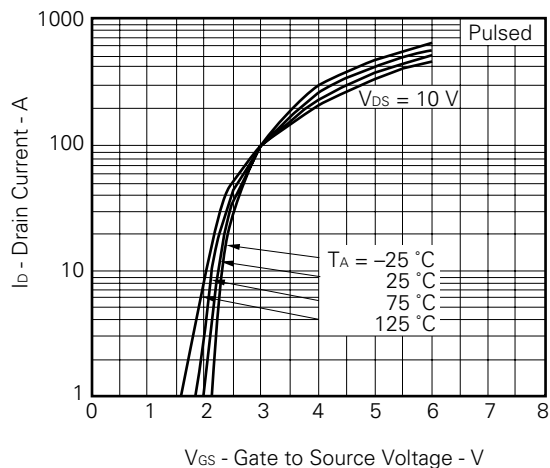
FORWARD BIAS SAFE OPERATING AREA



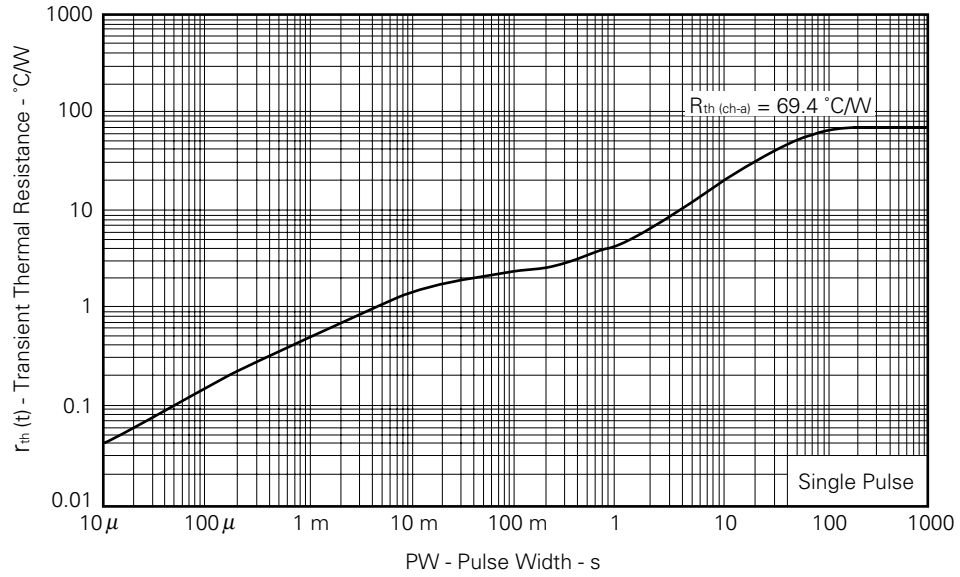
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



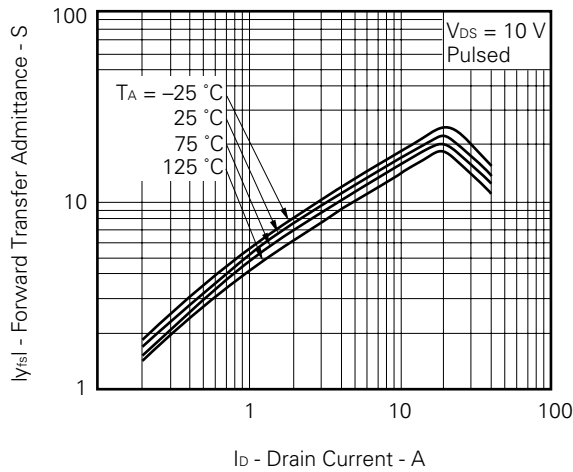
FORWARD TRANSFER CHARACTERISTICS



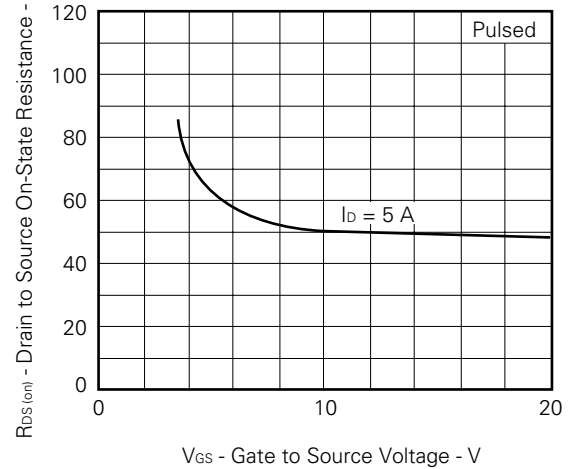
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



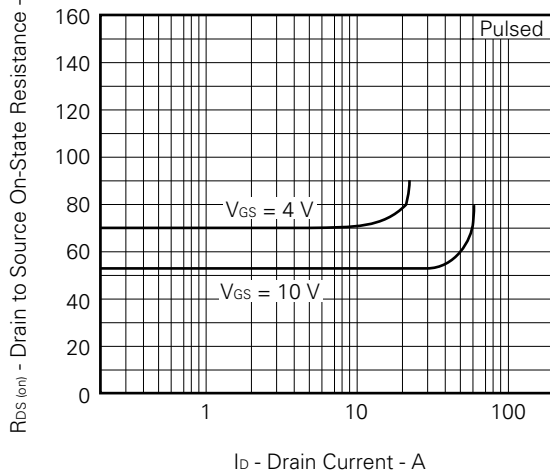
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



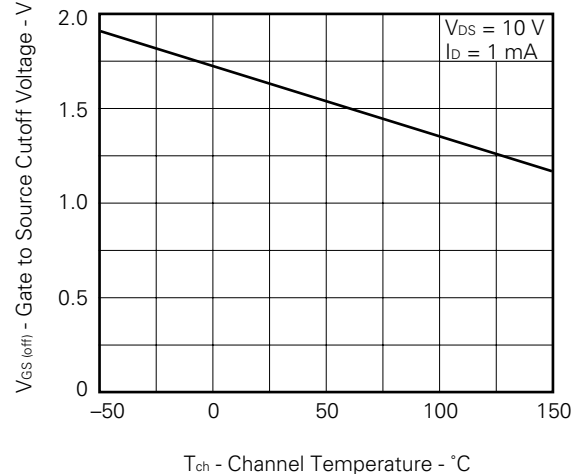
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

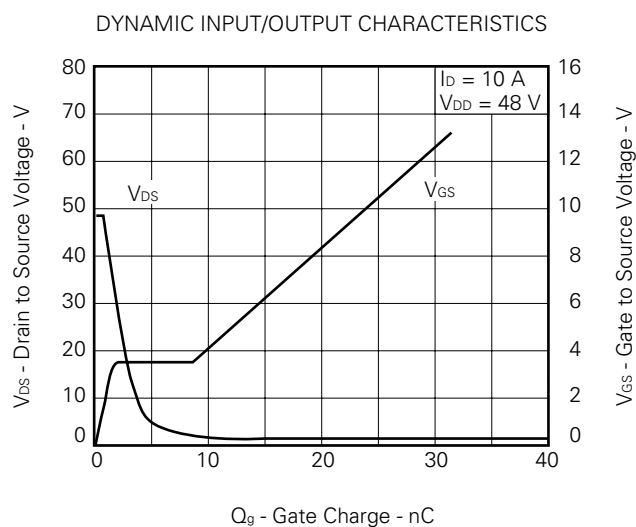
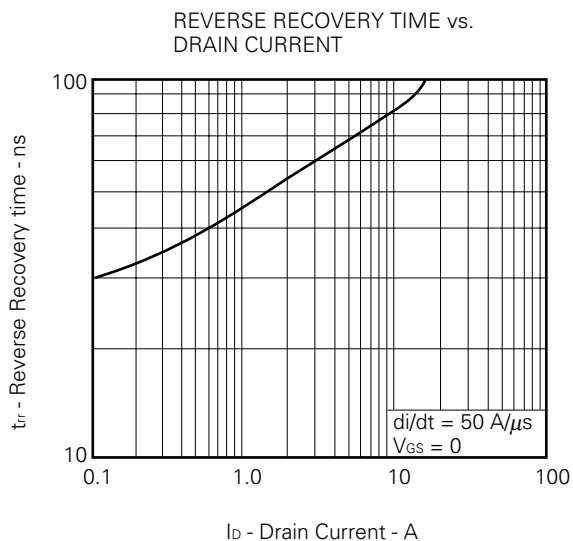
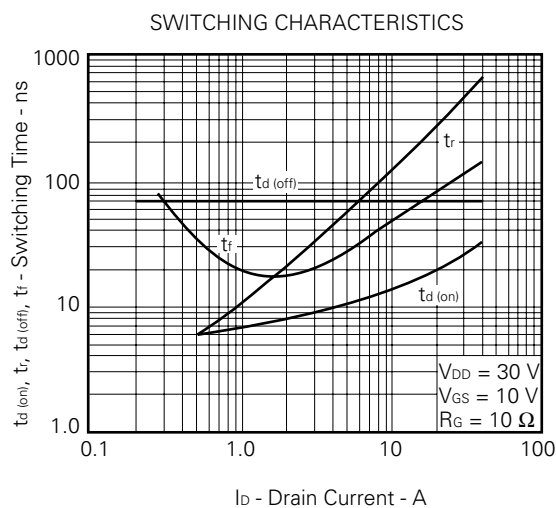
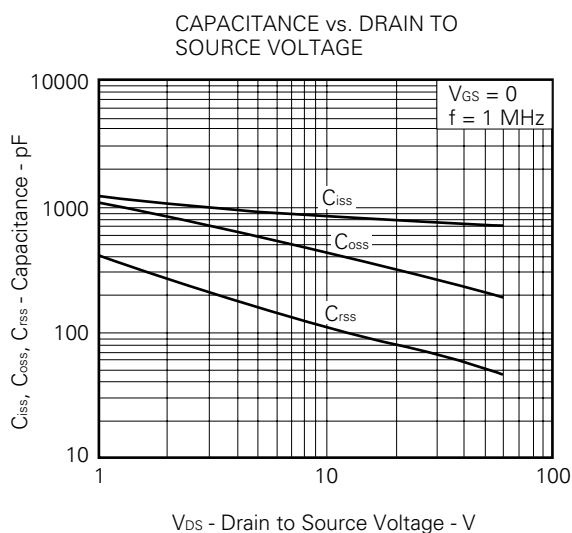
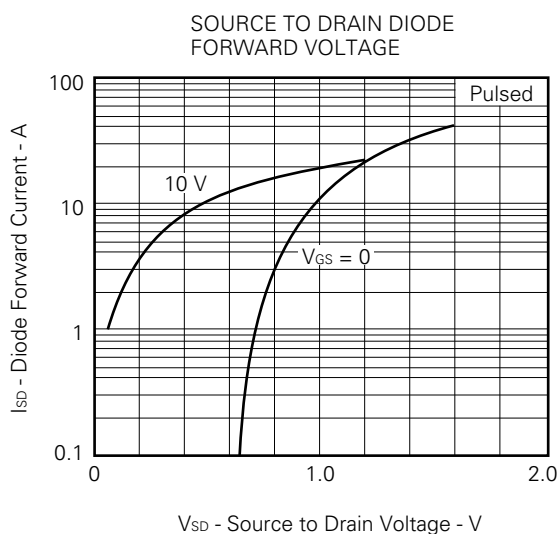
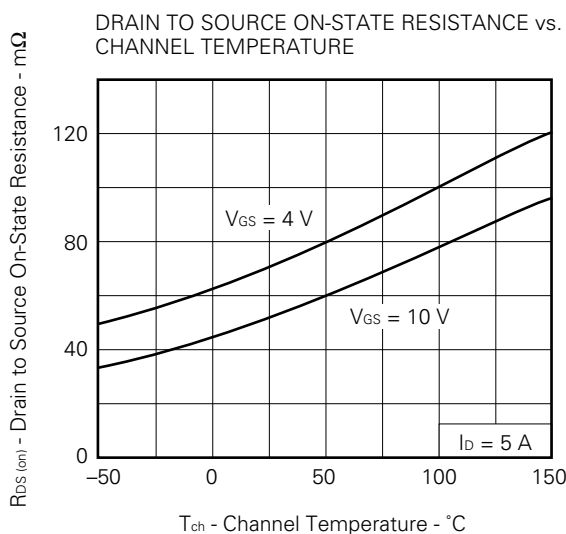


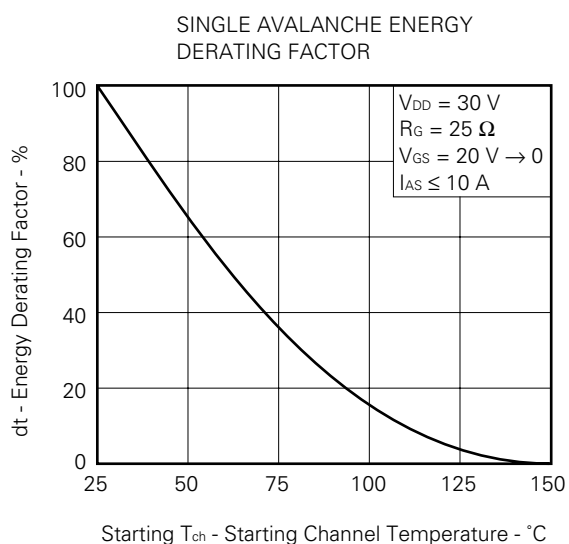
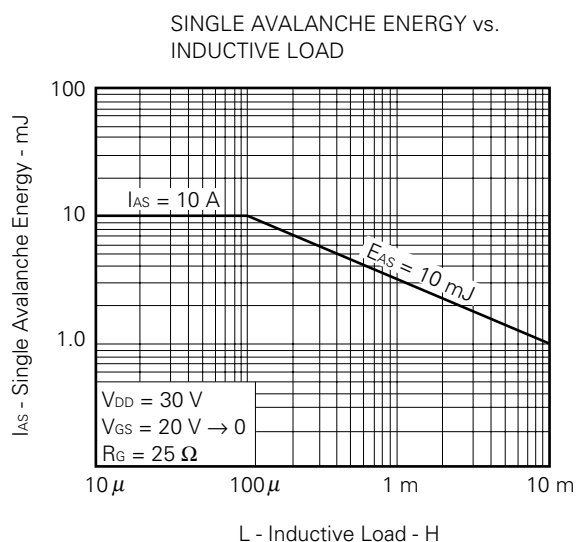
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE







REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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