

## MOS FIELD EFFECT TRANSISTORS

# 2SK2367/2SK2368

### SWITCHING

### N-CHANNEL POWER MOS FET

### INDUSTRIAL USE

#### DESCRIPTION

The 2SK2367/2SK2368 is N-Channel MOS Field Effect Transistor designed for high voltage switching applications.

#### FEATURES

- Low On-Resistance  
2SK2367:  $R_{DS(on)} = 0.5 \Omega$  ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 8.0 \text{ A}$ )  
2SK2368:  $R_{DS(on)} = 0.6 \Omega$  ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 8.0 \text{ A}$ )
- Low  $C_{iss}$   $C_{iss} = 1\,600 \text{ pF TYP.}$
- High Avalanche Capability Ratings

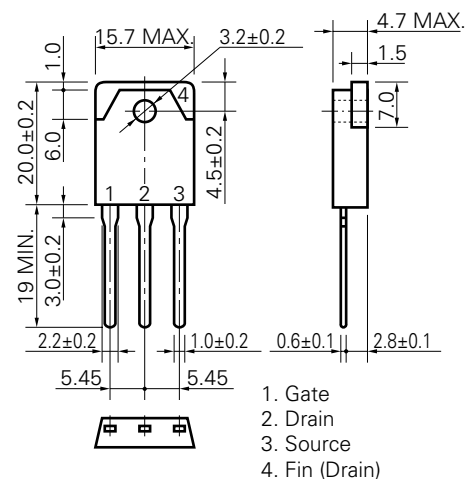
#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

|                                                      |                     |                        |                  |
|------------------------------------------------------|---------------------|------------------------|------------------|
| Drain to Source Voltage (2SK2367/2SK2368)            | $V_{DS}$            | 450/500                | V                |
| Gate to Source Voltage                               | $V_{GS}$            | $\pm 30$               | V                |
| Drain Current (DC)                                   | $I_D(\text{DC})$    | $\pm 15$               | A                |
| Drain Current (pulse)*                               | $I_D(\text{pulse})$ | $\pm 60$               | A                |
| Total Power Dissipation ( $T_c = 25^\circ\text{C}$ ) | $P_{T1}$            | 120                    | W                |
| Total Power Dissipation ( $T_A = 25^\circ\text{C}$ ) | $P_{T2}$            | 3.0                    | W                |
| Channel Temperature                                  | $T_{ch}$            | 150                    | $^\circ\text{C}$ |
| Storage Temperature                                  | $T_{stg}$           | $-55 \text{ to } +150$ | $^\circ\text{C}$ |
| Single Avalanche Current**                           | $I_{AS}$            | 15                     | A                |
| Single Avalanche Energy**                            | $E_{AS}$            | 161                    | mJ               |

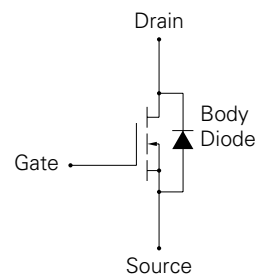
\*  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

\*\* Starting  $T_{ch} = 25^\circ\text{C}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0$

#### PACKAGE DIMENSIONS (in millimeter)



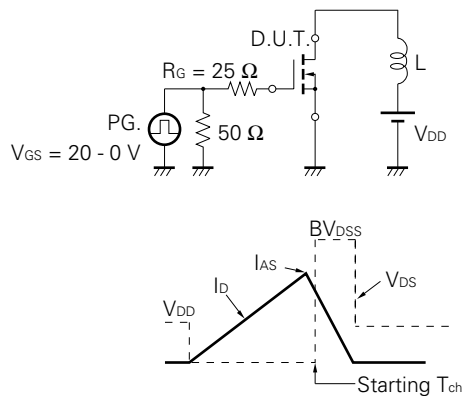
#### MP-88



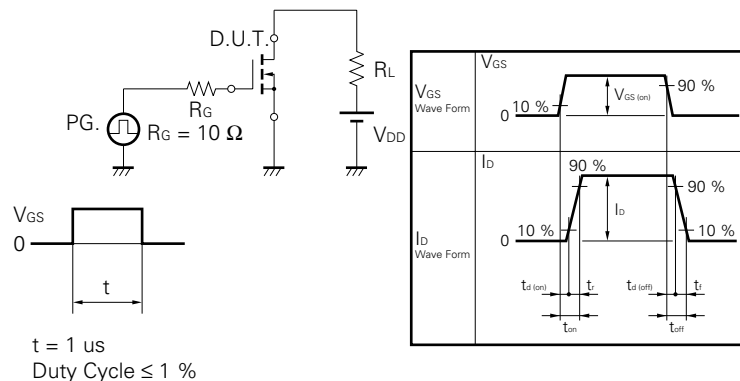
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

| CHARACTERISTIC                 | SYMBOL               | MIN. | TYP.  | MAX. | UNIT | TEST CONDITIONS                                          |         |
|--------------------------------|----------------------|------|-------|------|------|----------------------------------------------------------|---------|
| Drain to Source On-Resistance  | R <sub>DS(on)</sub>  |      | 0.4   | 0.5  | Ω    | V <sub>GS</sub> = 10 V                                   | 2SK2367 |
|                                |                      |      | 0.5   | 0.6  |      | I <sub>D</sub> = 8.0 A                                   | 2SK2368 |
| Gate to Source Cutoff Voltage  | V <sub>GS(off)</sub> | 2.5  |       | 3.5  | V    | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA            |         |
| Forward Transfer Admittance    | y <sub>fs</sub>      | 5.0  |       |      | S    | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 8.0 A           |         |
| Drain Leakage Current          | I <sub>DSS</sub>     |      |       | 100  | μA   | V <sub>DS</sub> = V <sub>DSS</sub> , V <sub>GS</sub> = 0 |         |
| Gate to Source Leakage Current | I <sub>GSS</sub>     |      |       | ±100 | nA   | V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0             |         |
| Input Capacitance              | C <sub>iss</sub>     |      | 1 600 |      | pF   | V <sub>DS</sub> = 10 V                                   |         |
| Output Capacitance             | C <sub>oss</sub>     |      | 300   |      | pF   | V <sub>GS</sub> = 0                                      |         |
| Reverse Transfer Capacitance   | C <sub>rss</sub>     |      | 30    |      | pF   | f = 1 MHz                                                |         |
| Turn-On Delay Time             | t <sub>d(on)</sub>   |      | 30    |      | ns   | I <sub>D</sub> = 8.0 A                                   |         |
| Rise Time                      | t <sub>r</sub>       |      | 40    |      | ns   | V <sub>GS</sub> = 10 V                                   |         |
| Turn-Off Delay Time            | t <sub>d(off)</sub>  |      | 70    |      | ns   | V <sub>DD</sub> = 150 V                                  |         |
| Fall Time                      | t <sub>f</sub>       |      | 25    |      | ns   | R <sub>G</sub> = 10 Ω R <sub>L</sub> = 18.8 Ω            |         |
| Total Gate Charge              | Q <sub>G</sub>       |      | 43    |      | nC   | I <sub>D</sub> = 15 A                                    |         |
| Gate to Source Charge          | Q <sub>GS</sub>      |      | 10    |      | nC   | V <sub>DD</sub> = 400 V                                  |         |
| Gate to Drain Charge           | Q <sub>GD</sub>      |      | 20    |      | nC   | V <sub>GS</sub> = 10 V                                   |         |
| Body Diode Forward Voltage     | V <sub>F(S-D)</sub>  |      | 1.0   |      | V    | I <sub>F</sub> = 15 A, V <sub>GS</sub> = 0               |         |
| Reverse Recovery Time          | t <sub>rr</sub>      |      | 400   |      | ns   | I <sub>F</sub> = 15 A, V <sub>GS</sub> = 0               |         |
| Reverse Recovery Charge        | Q <sub>rr</sub>      |      | 1.8   |      | μC   | di/dt = 50 A/μs                                          |         |

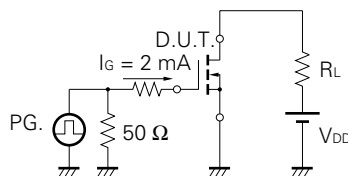
**Test Circuit 1 Avalanche Capability**



**Test Circuit 2 Switching Time**

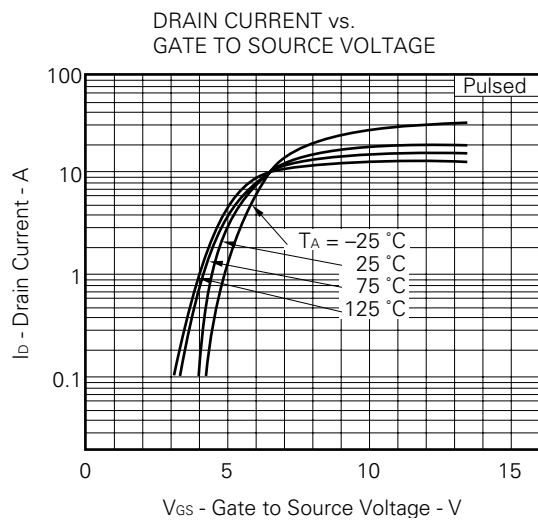
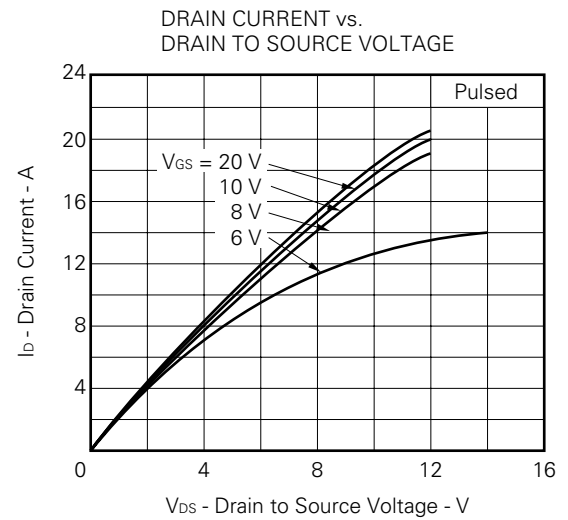
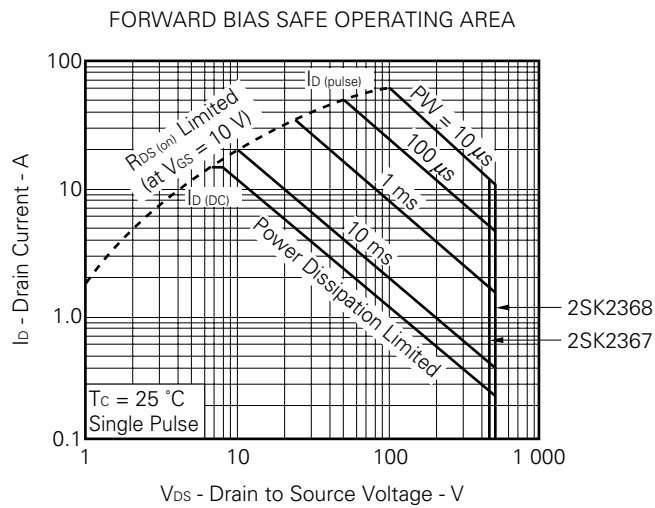
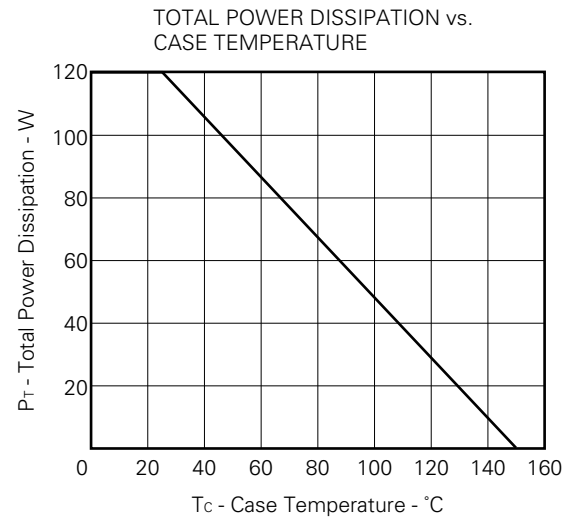
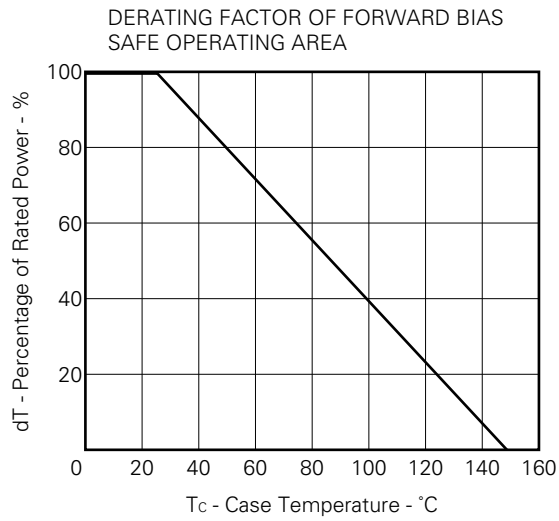


**Test Circuit 3 Gate Charge**

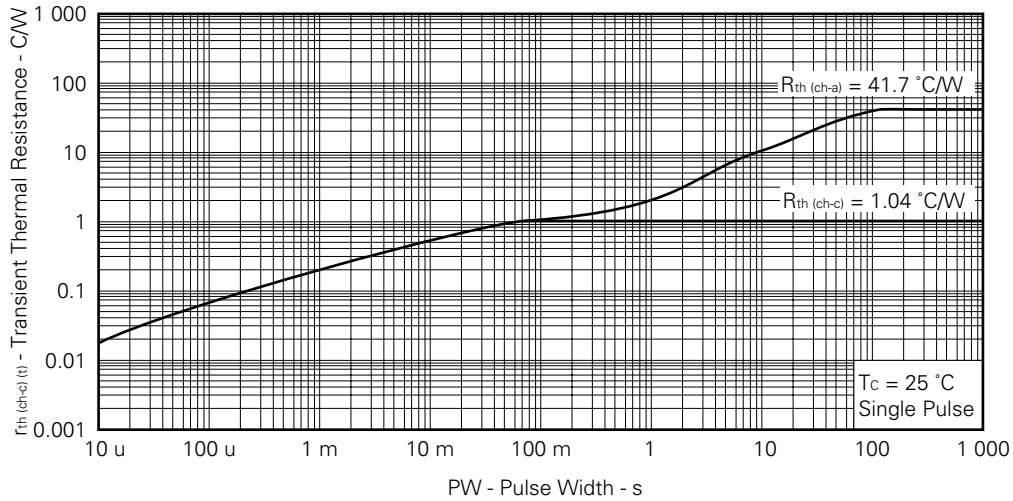


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

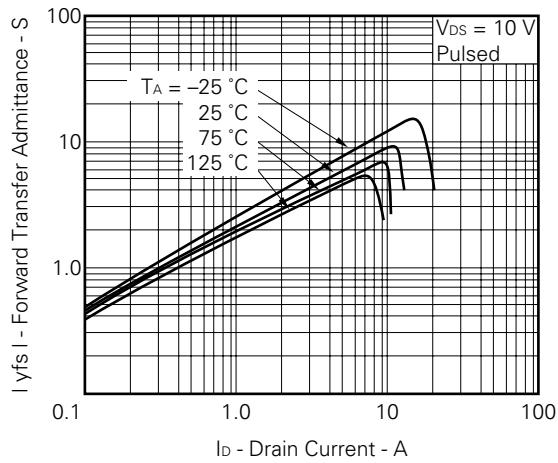
TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )



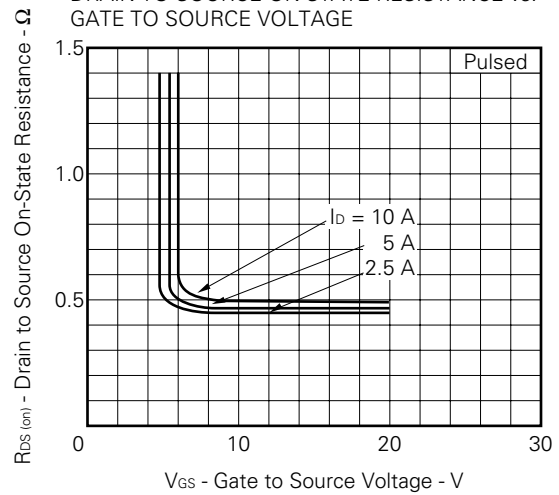
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



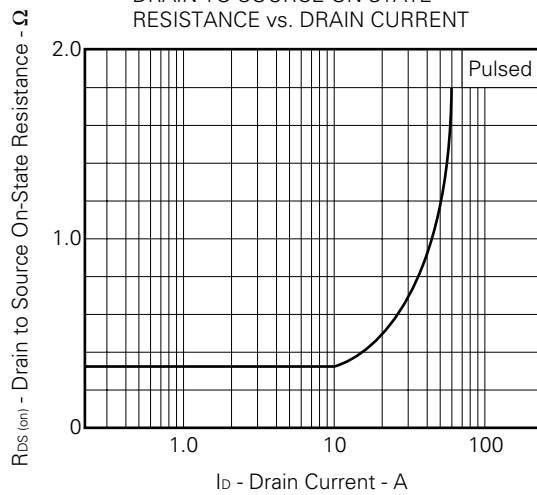
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



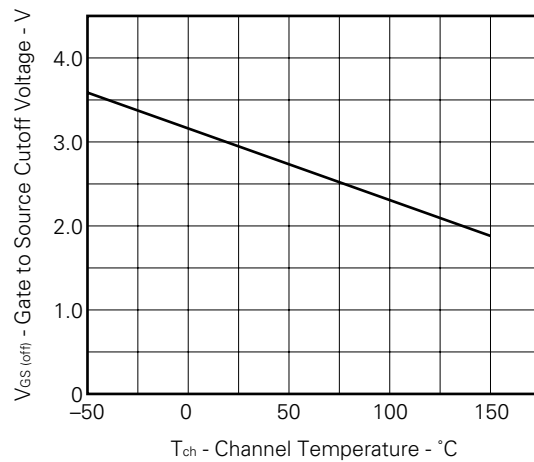
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

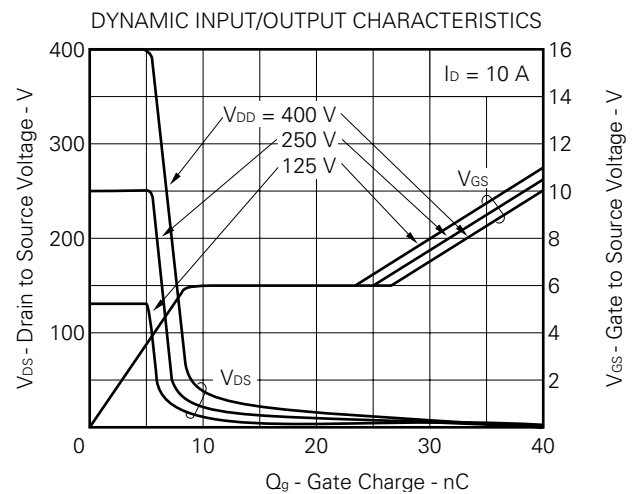
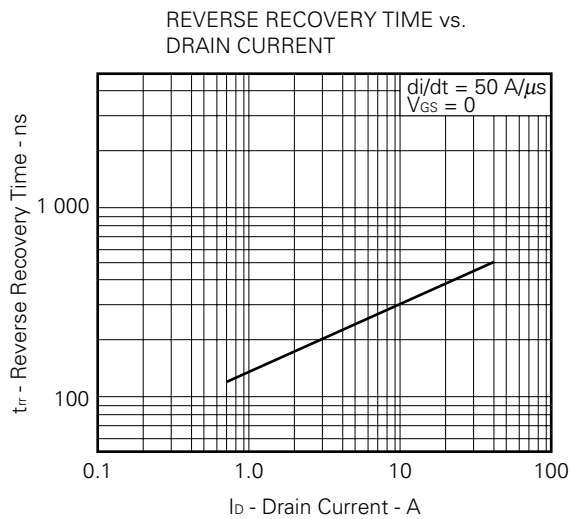
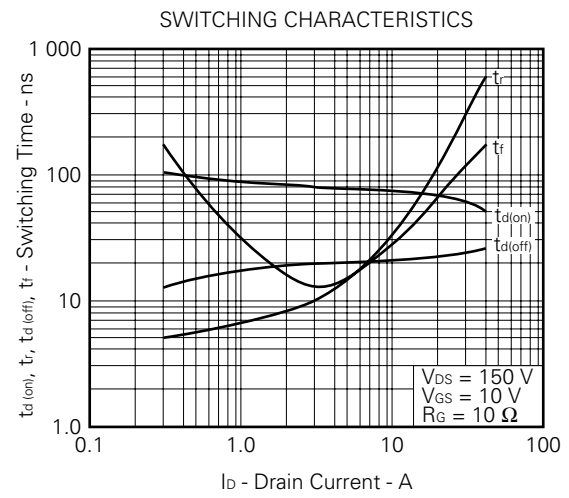
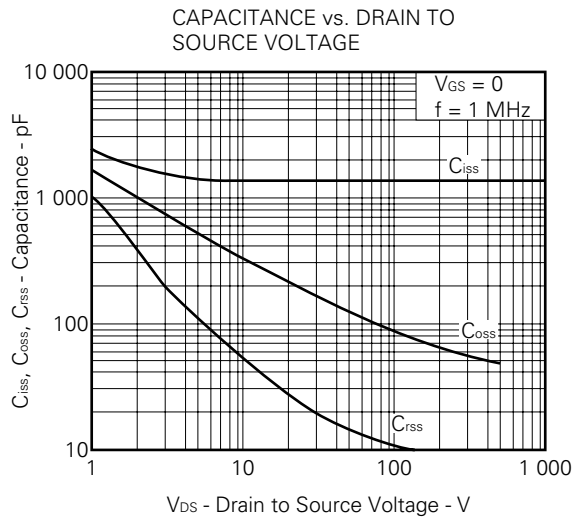
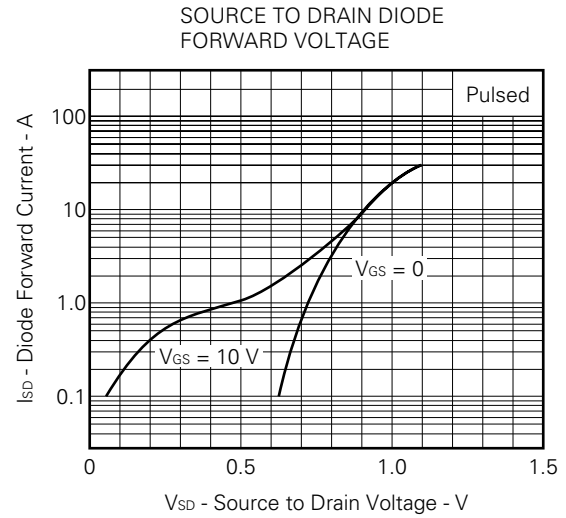
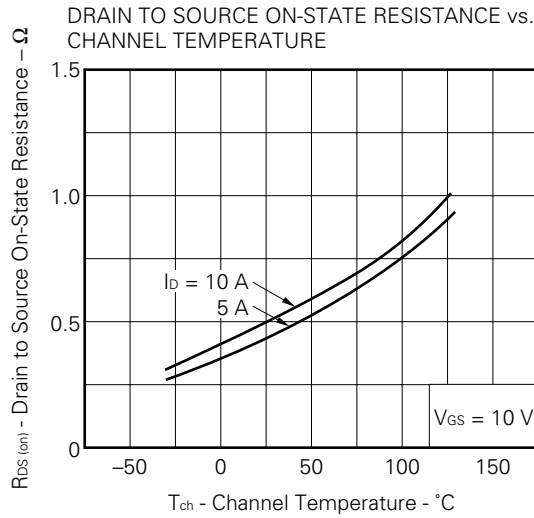


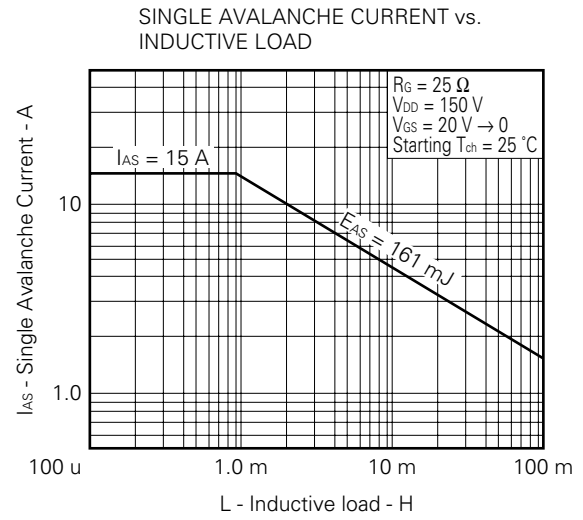
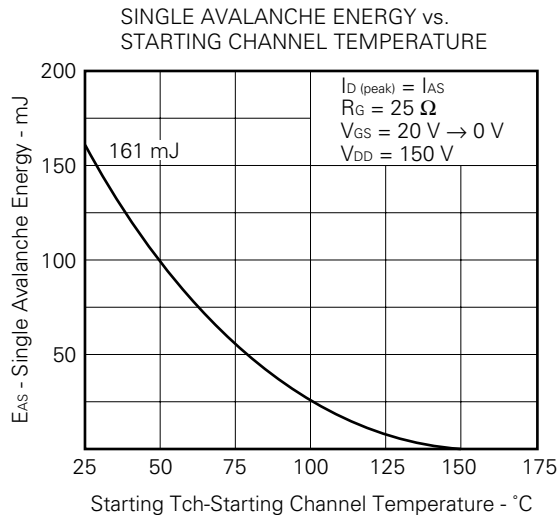
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE







## REFERENCE

| Document Name                                                  | Document No. |
|----------------------------------------------------------------|--------------|
| NEC semiconductor device reliability/quality control system.   | TEI-1202     |
| Quality grade on NEC semiconductor devices.                    | IEI-1209     |
| Semiconductor device mounting technology manual.               | IEI-1207     |
| Semiconductor device package manual.                           | IEI-1213     |
| Guide to quality assurance for semiconductor devices.          | MEI-1202     |
| Semiconductor selection guide.                                 | MF-1134      |
| Power MOS FET features and application switching power supply. | TEA-1034     |
| Application circuits using Power MOS FET.                      | TEA-1035     |
| Safe operating area of Power MOS FET.                          | TEA-1037     |

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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