TOSHIBA MOS MEMORY PRODUCTS

TC5514AP-2/-3
TC5514APL-2/-3

1,024 WORD × 4 BIT CMOS STATIC RAM
SILICON GATE CMOS

DESCRIPTION

The TC5514AP is a 4,096 bit high speed and low power random access memory organized as 1,024 words by 4 bits using CMOS technology, and operates from a single 5-volt supply.

The 5514AP is compatible with the industry produced NMOS 2114 type 4KRAM, yet offers a more than 90% reduction in power of their NMOS equivalents.

The TC5514AP is a fully CMOS RAM, therefore it is suited for use in low power applications where battery operation and battery back up for nonvolatility are required. Furthermore the TC5514APL guaranteed a standby current equal to or less than 1μA at 60℃ ambient temperature is avaliable.

The TC5514AP is guaranteed for data retention at a power supply as low as 2 volts. The TC5514AP is directly TTL compatible in all inputs and outputs.

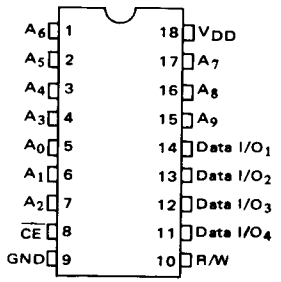
The TC5514AP is offered in standerd 18 pin plastic, 0.3inch in width.

FEATURES

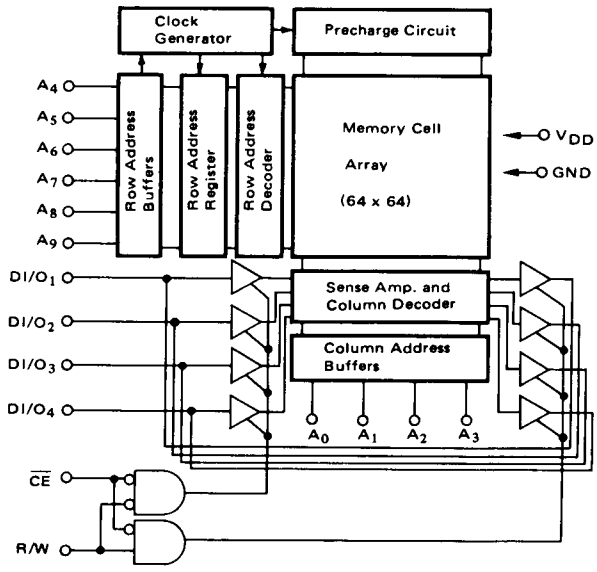
- Standby Current
  0.2μA (Max.) at Ta=25°C } : TC5514APL
  1.0μA (Max.) at Ta=60°C }
  20μA (Max.) : TC5514AP
- Low Power Dissipation : 15mW (Typ.) operating
- Single 5-volt Supply : 5V ± 10%
- Data Retention Supply Voltage : 2 ~ 5.5V
- Three State Outputs
- All Inputs and Outputs : Directly TTL Compatible
- Access Time
  200ns (Max.) : TC5514 AP/APL-2
  300ns (Max.) : TC5514 AP/APL-3
- Fully Static Operation
- On-chip Address Transition Detector
- Fully Compatible with TMM2114AP Family (Nch 2114 type 4KRAM)
- Package
  Plastic DIP : TC5514AP/APL

PIN CONNECTION

(TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_9$	Address Inputs
R/W	Read Write Control Input
$\overline{CE}$	Chip Enable Input
Data $I/O_{1 \sim 4}$	Data Input/Output
V_{DD}/GND	Power Supply Terminals

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3 ~ 7.0	V
V_{IN}	Input Voltage	−0.3 ~ 7.0	V
$V_{I/O}$	I/O Voltage	0 ~ V_{DD}	V
P_D	Power Dissipation(Ta = 85°C)	550	mW
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{STG}	Storage Temperature	−55 ~ 150	°C
T_{OPR}	Operating Temperature	−30 ~ 85	°C

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Level Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Level Voltage	−0.3	–	0.8	V
V_{DH}	Data Retention Voltage	2.0	–	5.5	V

D.C. CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = −30 ~ 85°C unless otherwise noted.)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP. (1)	MAX.	UNIT
I_{IL}	Input Leakage Current	$0V \leqq V_{IN} \leqq V_{DD}$			–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$, $0V \leqq V_{I/O} \leqq V_{DD}$			–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.0	–	–	mA
I_{DDS}	Standby Current	V_{DD} = 2V ~ 5.5V All Inputs = 0.2V or V_{DD} − 0.2V	TC5514APL	Ta = 25°C	–	–	0.2	μA
				Ta = 60°C	–	–	1.0	μA
			TC5514AP		–	0.05	20	μA
I_{DDO1}	Operating Current	t_{cycle} = 1μs, I_{OUT} = 0mA			–	5.0	9.0	mA
I_{DDO2}		t_{cycle} = 1μs, $V_{IH} = V_{DD}$, V_{IL} = 0V, I_{OUT} = 0mA			–	3.0	5.0	

Note (1): V_{DD} = 5V, Ta = 25°C

CAPACITANCE(2) (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	4	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	–	5	10	pF

Note (2): This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = −30 ~ 85°C)

- **READ CYCLE**

SYMBOL	PARAMETER	TC5514AP-2/APL-2		TC5514AP-3/APL-3		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	200	–	300	–	ns
t_{ACC}	Access Time	–	200	–	300	ns
t_{CO}	$\overline{CE}$ Access Time	–	70	–	100	ns
t_{OH}	Output Data Hold Time	15	–	20	–	ns
t_{DIS}	Output Disable Time	–	60	–	80	ns
t_{COE}	Output Enable Time	5	–	5	–	ns

- **WRITE CYCLE**

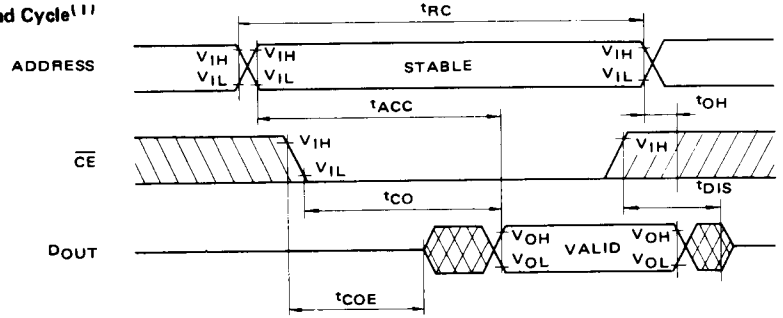
SYMBOL	PARAMETER	TC5514AP-2/APL-2		TC5514AP-3/APL-3		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	200	–	300	–	ns
t_{AW}	Address Setup Time	0	–	0	–	ns
t_{WP}	Write Pulse Width	120	–	150	–	ns
t_{DS}	Data Setup Time	120	–	150	–	ns
t_{DH}	Data Hold Time	0	–	0	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	ns

A.C. TEST CONDITIONS

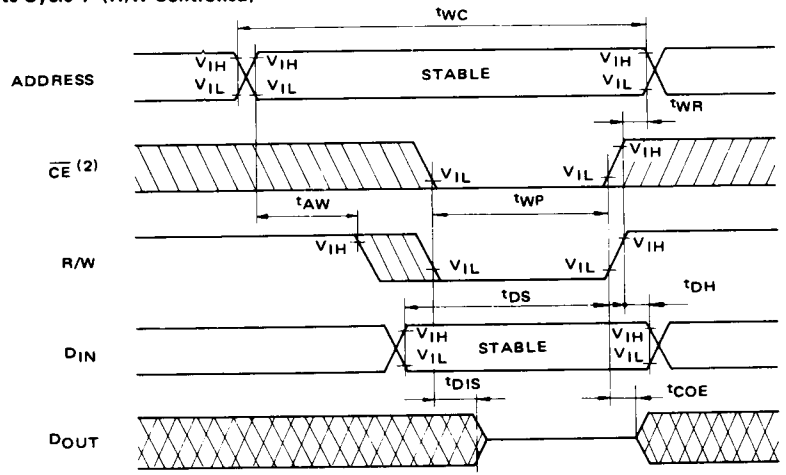
- Output Load : 100 pF + 1 TTL Gate
- Input Pulse Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels
  - Input : 0.8V, 2.2V
  - Output : 0.8V, 2.2V
- Input Pulse Rise and Fall Times : 10 ns

TIMING WAVEFORMS

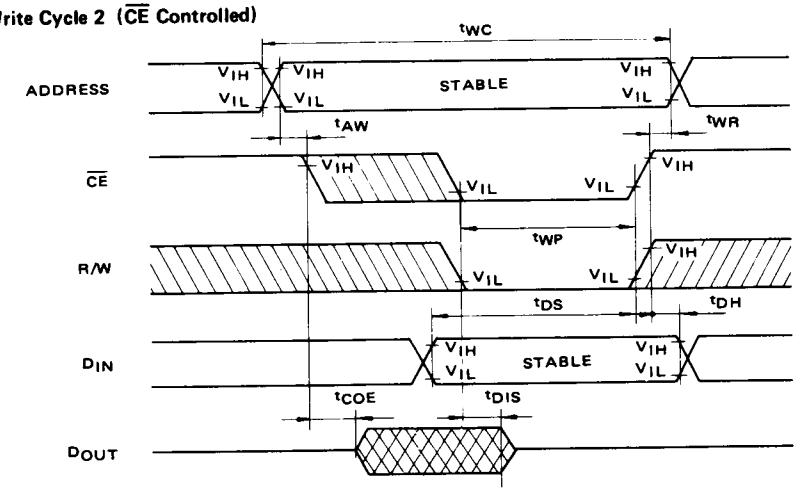
● Read Cycle[1]



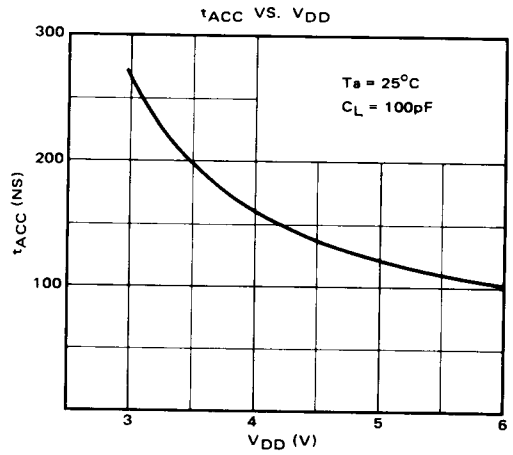
● Write Cycle 1 (R/W Controlled)

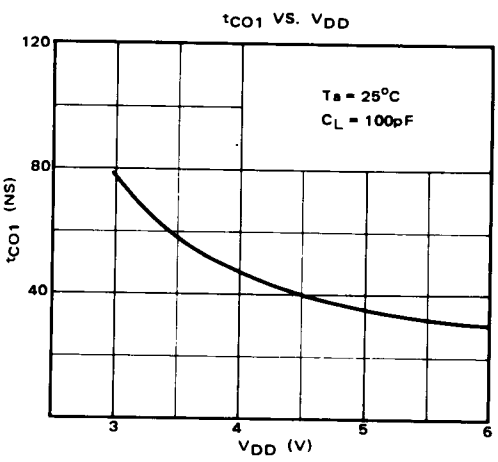


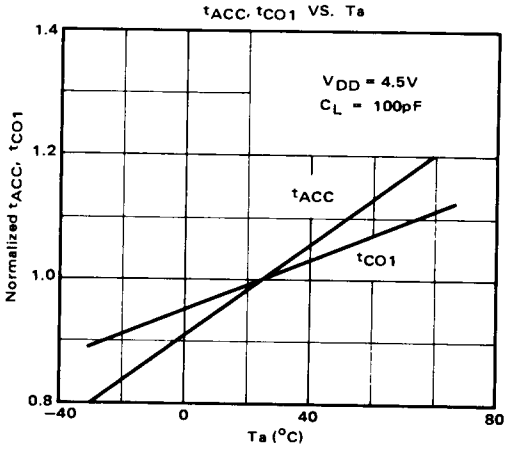
● Write Cycle 2 ($\overline{CE}$ Controlled)

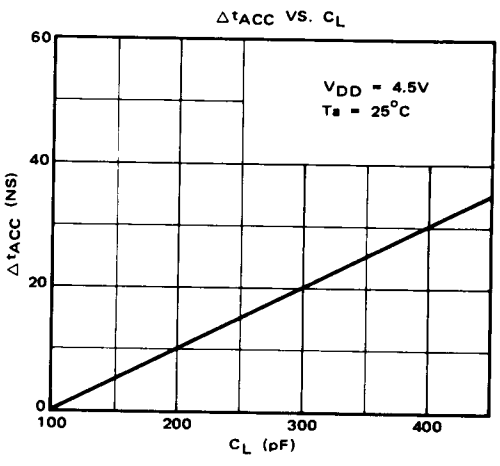


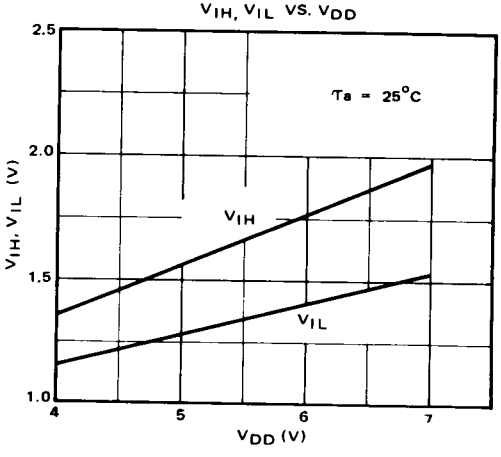
Notes: (1) R/W is high for a Read Cycle.
(2) If the $\overline{CE}$ low transition occurs simultaneously with the R/W low transition, the output buffers remain in a high impedance state.

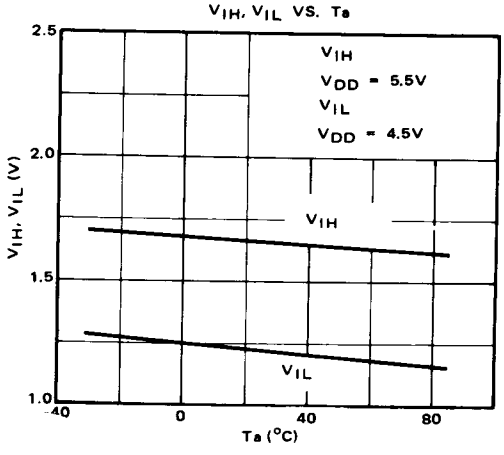

t_{ACC} VS. V_{DD}
Ta = 25°C
C_L = 100pF
t_{ACC} (NS)
300
200
100
3
4
5
6
V_{DD} (V)


t_{CO1} VS. V_{DD}
Ta = 25°C
C_L = 100pF
t_{CO1} (NS)
120
80
40
3
4
5
6
V_{DD} (V)

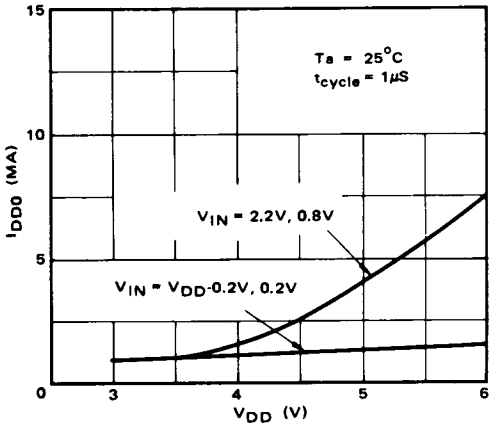

t_{ACC}, t_{CO1} VS. Ta
V_{DD} = 4.5V
C_L = 100pF
t_{ACC}
t_{CO1}
Normalized t_{ACC}, t_{CO1}
1.4
1.2
1.0
0.8
−40
0
40
80
Ta (°C)


Δt_{ACC} VS. C_L
V_{DD} = 4.5V
Ta = 25°C
Δt_{ACC} (NS)
60
40
20
0
100
200
300
400
C_L (pF)

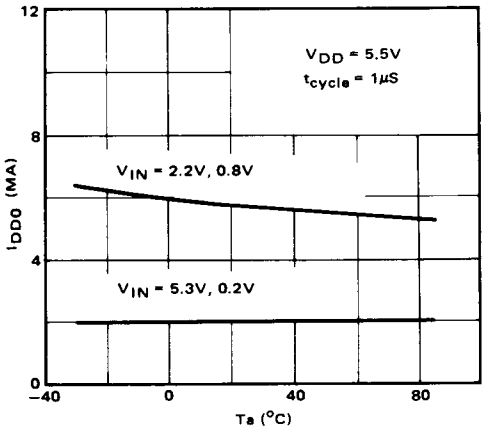

V_{IH}, V_{IL} VS. V_{DD}
Ta = 25°C
V_{IH}
V_{IL}
V_{IH}, V_{IL} (V)
2.5
2.0
1.5
1.0
4
5
6
7
V_{DD} (V)


V_{IH}, V_{IL} VS. Ta
V_{IH}
V_{DD} = 5.5V
V_{IL}
V_{DD} = 4.5V
V_{IH}, V_{IL} (V)
2.5
2.0
1.5
1.0
−40
0
40
80
Ta (°C)

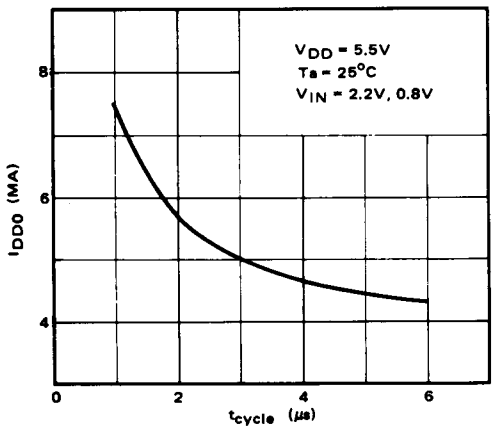
I_{DDO} VS. V_{DD}



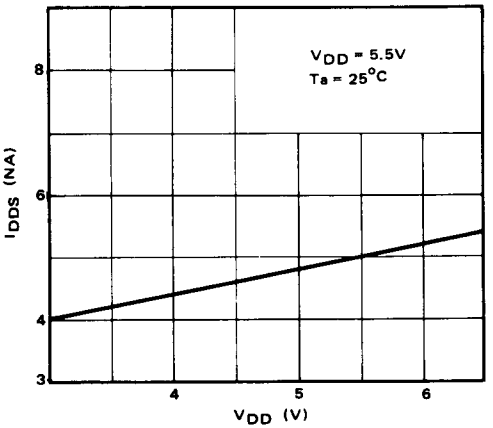
I_{DDO} VS. Ta



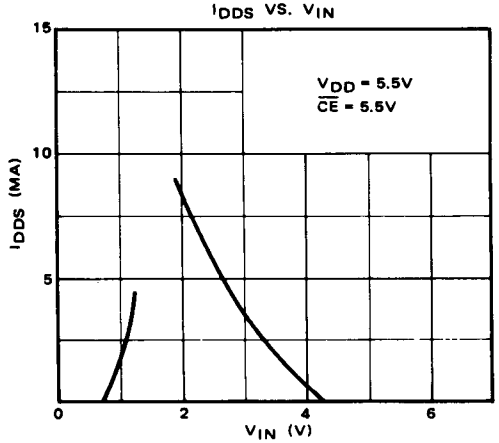
I_{DDO} VS. t_{cycle}



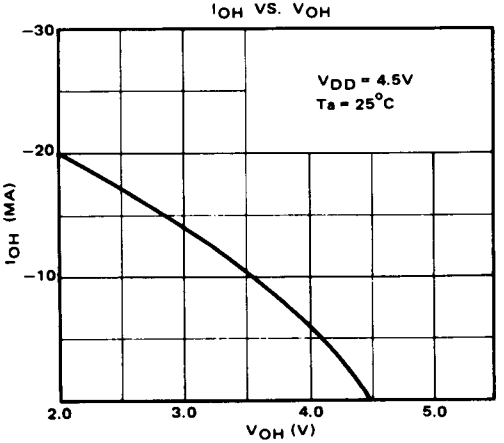
I_{DDS} VS. V_{DD}

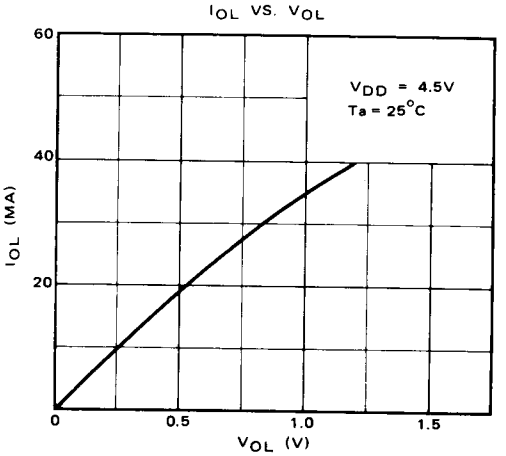


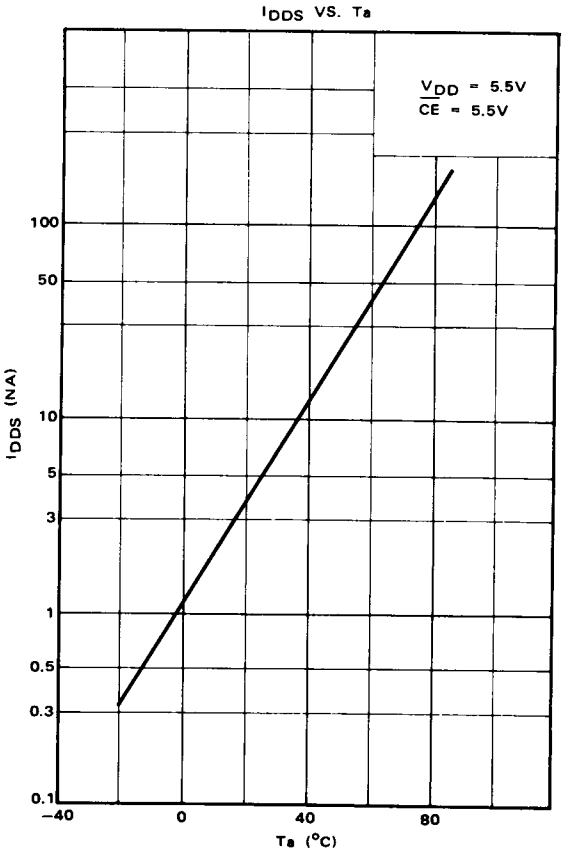
I_{DDS} VS. V_{IN}



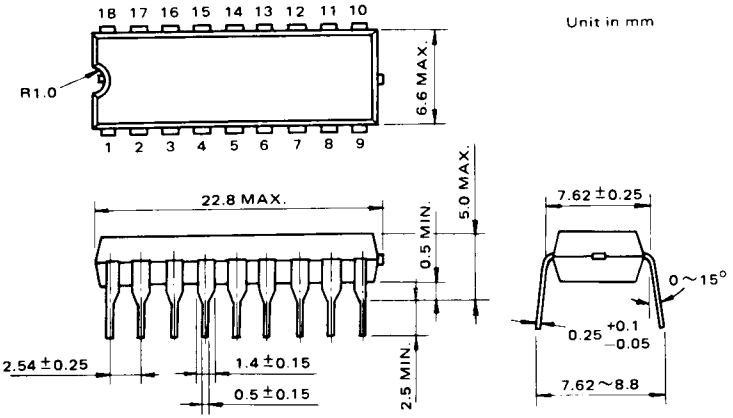
I_{OH} VS. V_{OH}




I_{OL} VS. V_{OL}
V_{DD} = 4.5V
Ta = 25°C
I_{OL} (MA)
60
40
20
0
0.5
1.0
1.5
V_{OL} (V)


I_{DDS} VS. Ta
V_{DD} = 5.5V
$\overline{CE}$ = 5.5V
I_{DDS} (NA)
100
50
10
5
3
1
0.5
0.3
0.1
−40
0
40
80
Ta (°C)

- PLASTIC PACKAGE



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.18 leads.
All dimensions are in millimeters.