TEXAS INSTRUMENTS

TSB14AA1A, TSB14AA1AI, TSB14AA1AT

3.3-V IEEE 1394-1995 Backplane PHY

Data Manual

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1 Introduction

1.1 Description

The TSB14AA1A (TSB14AA1A refers to all three devices: TSB14AA1A, TSB14AA1AI, and TSB14AA1AT) is the second-generation 1394 backplane physical layer device. It is recommended for use in all new designs instead of the first generation TSB14C01A. It provides the physical layer functions needed to implement a single port node in a backplane based 1394 network. The TSB14AA1A provides two pins for transmitting, two for receiving, and two pins to externally control the transceivers for data and strobe. In addition to supporting open-collector drivers, the TSB14AA1A can also support 3-state† (high-impedance) drivers. The TSB14AA1A is not designed to drive the backplane directly; this function must be provided externally. The TSB14AA1A is designed to interface with a link-layer controller (LLC), such as the TSB12LV01B, TSB12LV32, TSB12LV21B, etc.

The TSB14AA1A requires an external 98.304-MHz reference oscillator input for S100 asynchronous only operation or 49.152-MHz for S50 asynchronous only operation. Two clock select pins (CLK_SEL0, CLK_SEL1) select the speed mode for the TSB14AA1A (see Table 1–1). For S100 operation, the 98.304-MHz reference signal is internally divided to provide the 49.152-MHz system clock signals used to control transmission of the outbound encoded strobe and data information. The 49.152-MHz clock signal is also supplied to the associated LLC for synchronization of the two chips and is used for resynchronization of the received data. For S50 operation, a 49.152-MHz reference signal is used. This reference signal is internally divided to provide the 24.576-MHz system clock signals for S50 operations.

Table 1–1. Speed Mode Setting

SPEED MODE	CLK_SEL0 PIN	CLK_SEL1 PIN	INPUT TO XI PIN	PHY_SCLK OUTPUT	MAXIMUM FREQUENCY OF TDATA, TSTRB
100 Mbits/s	0	0	100 MHz	X1/2 (50 MHz)	50 MHz
50 Mbits/s	1	0	50 MHz	X1/2 (25 MHz)	25 MHz
Reserved	1	1	—		
Reserved	0	1	—	—	—

During packet transmit, data bits to be transmitted are received from the LLC on two parallel paths and are latched internally in the TSB14AA1A in synchronization with the system clock. These bits are combined serially, encoded, and transmitted as the outbound data-strobe information stream. During transmit, the encoded data information is transmitted on TDATA, and the encoded strobe information is transmitted on TSTRB.

During packet reception, the data information is received on RDATA and strobe information is received on RSTRB. The received data and strobe information is decoded to recover the received clock signal and the serial data bits, which are resynchronized to the local system clock. The serial data bits are split into two parallel streams and sent to the associated LLC. The PHY-Link interface has been made compliant to IEEE 1394a–2000 including timing and transfer of register 0 to the link-layer automatically after every 1394 bus reset.

The TSB14AA1A is a 3.3 V device that provides LVCMOS level outputs. The TSB14AA1A is an asynchronous only device.

† 3-State means a driver may drive high, low, or may be placed in a high-impedance state

1.2 Features

- Provides a Backplane 1394 Environment That Supports an Asynchronous Transfer Rate of 50 or 100 Mbits/s Across 2 Etches
- Single 3.3-V Supply Operation With 5-V Tolerance on the Transceiver Receive Interface
- Allows Utilization of 3-State Drivers as Well as Open-Collector Drivers
- Software Compatible With the TSB14CO1APM
- Enhanced Compatibility With the 1394 Cable Link Layer. Compatible With 1394–1995 and 1394a–2000 Link Layers; PHY/link Interface is 1394a Compliant†
- Supports Provisions of IEEE 1394–1995‡§
- Extensive Testability and Debug Functions Added. Expanded Register Set Including Automatic Saving of ID and Priority for Last Node Winning Arbitration
- 100 MHz or 50 MHz Oscillator Provides Transmit, Receive Data, and Link Layer Controller (LLC) Clocks
- Logic Performs System Initialization Arbitration Functions. Encode And Decode Functions Included for Data-Strobe Bit Level Encoding. Incoming Data Resynchronized to Local Clock.
- Operates Over the Extended Temperature Ranges of 0°C to 70°C (no suffix), –40°C to 85°C (I suffix), and –40°C to 105°C (T suffix)
- Packaged in the Very Compact 48-Pin 7 x 7 x 1 mm PFB Package

1.3 Ordering Information

ORDERING NUMBER	TEMPERATURE	VCC	PACKAGE
TSB14AA1A	0°C to 70°C	3.3 V	48-pin PFB
TSB14AA1AI	–40°C to 85°C	3.3 V	48-pin PFB
TSB14AA1AT	–40°C to 105°C	3.3 V	48-pin PFB

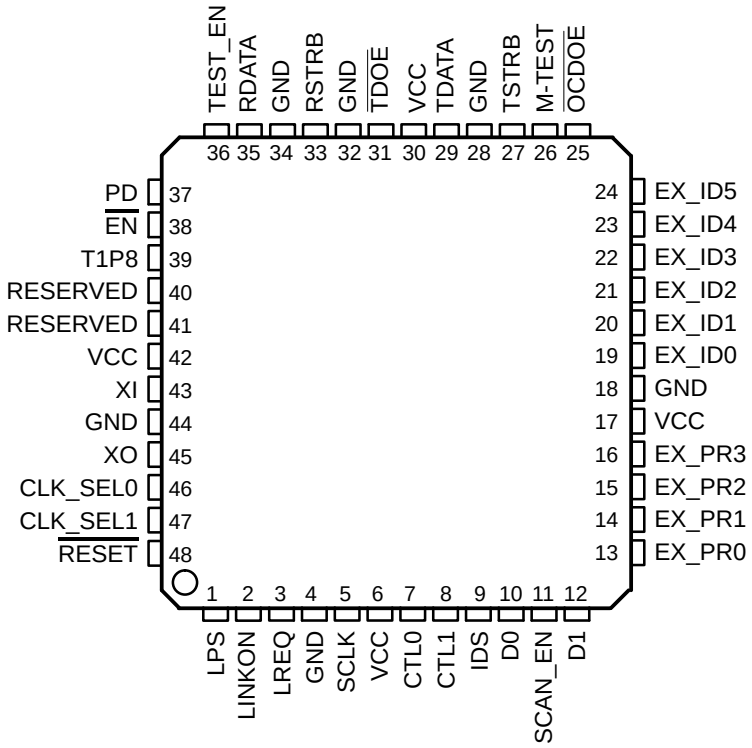
† IEEE Std 1394a–2000, *IEEE Standard for a High Performance Serial Bus – Amendment 1*

‡ † IEEE Std 1394–1995, *IEEE Standard for a High Performance Serial Bus*

§ Implements technology covered by one or more patents of Apple Computer, Inc. and ST Microelectronics.

1.4 Terminal Assignments/Package

PFB PACKAGE
(TOP VIEW)



1.5 Terminal Descriptions

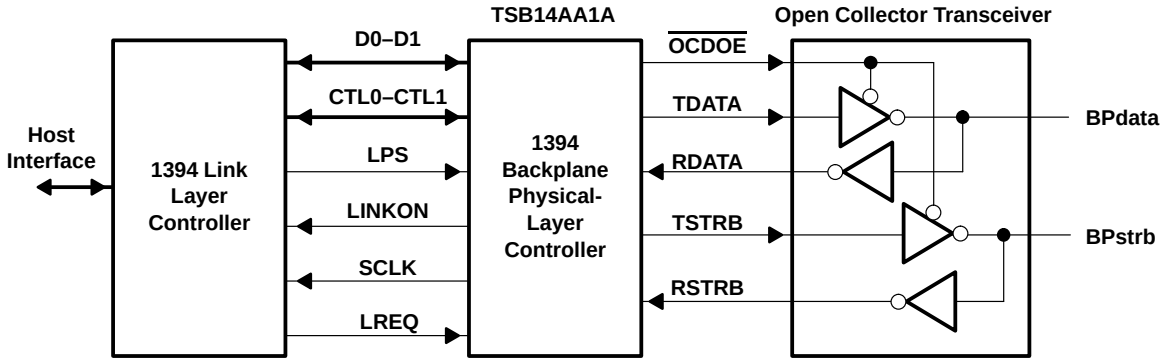
TERMINAL NAME	TERMINAL NO.	TYPE	I/O	DESCRIPTION
CLK_SEL0	46	CMOS	I	Clock select 0. If this terminal is set to low (0) then the speed is 98.304 Mbps. If this terminal is set to high (1) the speed is 49.152 Mbps. To operate at 100 Mbps requires an input clock of 98.304 MHz. To operate at 49.152 Mbps requires an input clock of 49.152 MHz.
CLK_SEL1	47	CMOS	I	Clock select 1. CLK_SEL1 must be tied to ground during normal operation.
CTL0, CTL1	7, 8	CMOS	I/O	Control I/O. These are bidirectional signals that communicate between the TSB14AA1A and the link layer that controls the passage of information between the two devices.
D0, D1	10, 12	CMOS	I/O	Data I/O. These are bidirectional information signals that communicate the data between the TSB14AA1A and the link layer controller.
$\overline{\text{EN}}$	38	Supply	I	Enable on-chip regulator. This active low pin enables the 1.8 V on–chip regulator.
EX_ID0	19	CMOS	I	External ID 0. The state of this pin sets the value of bit 0 of the *PHYSICAL_ID* field in the *NODE ID* Register upon hardware or SWHRST reset. The register bit may be modified by software.
EX_ID1	20	CMOS	I	External ID 1. The state of this pin sets the value of bit 1 of the *PHYSICAL_ID* field in the *NODE ID* register upon hardware or SWHRST reset. The register bit may be modified by software.
EX_ID2	21	CMOS	I	External ID 2. The state of this pin sets the value of bit 2 of the *PHYSICAL_ID* field in the *NODE ID* register upon hardware or SWHRST reset. The register bit may be modified by software.
EX_ID3	22	CMOS	I	External ID 3. The state of this pin sets the value of bit 3 of the *PHYSICAL_ID* field in the *NODE ID* register upon hardware or SWHRST reset. The register bit may be modified by software.
EX_ID4	23	CMOS	I	External ID 4. The state of this pin sets the value of bit 4 of the *PHYSICAL_ID* field in the *NODE ID* register upon hardware or SWHRST reset. The register bit may be modified by software.
EX_ID5	24	CMOS	I	External ID 5. The state of this pin sets the value of bit 5 of the *PHYSICAL_ID* field in the *NODE ID* register upon hardware or SWHRST reset. The register bit may be modified by software.
EX_PR0	13	CMOS	I	External priority 0. The state of this pin sets the value of bit 0 of the *PRIORITY* field in the *PRIORITY* register upon hardware or SWHRST reset. The register bit may be modified by software.
EX_PR1	14	CMOS	I	External priority 1. The state of this pin sets the value of bit 1 of the *PRIORITY* field in the *PRIORITY* register upon hardware or SWHRST reset. The register bit may be modified by software.
EX_PR2	15	CMOS	I	External priority 2. The state of this pin sets the value of bit 2 of the *PRIORITY* field in the *PRIORITY* register upon hardware or SWHRST reset. The register bit may be modified by software.
EX_PR3	16	CMOS	I	External priority 3. The state of this pin sets the value of bit 3 of the *PRIORITY* field in the *PRIORITY* register upon hardware or SWHRST reset. The register bit may be modified by software.
GND	4, 18, 28, 32, 34, 44	Supply		Ground voltage reference
IDS	9	CMOS	I	Invert data strobe. When this pin is set low, the TDATA, TSTRB, RDATA, RSTRB, $\overline{\text{OCDOE}}$, and $\overline{\text{TDOE}}$ pins operate normally (i.e., true). When this pin is set high, these six pins are inverted.
LINKON	2	CMOS	O	Link-On output. This pin notifies the LLC to power-up and become active. LINKON is a square-wave signal with a frequency between 4 and 8 MHz when active. LINKON is otherwise driven low, except during a hardware reset when it is high impedance. LINKON is activated if the LPS is inactive (LLC inactive) and when the PHY receives a link-on PHY packet addressed to this node. Once activated, LINKON will continue active until the LPS becomes active (LLC active). The PHY also deasserts (low) LINKON when a bus-reset occurs.

1.5 Terminal Descriptions (Continued)

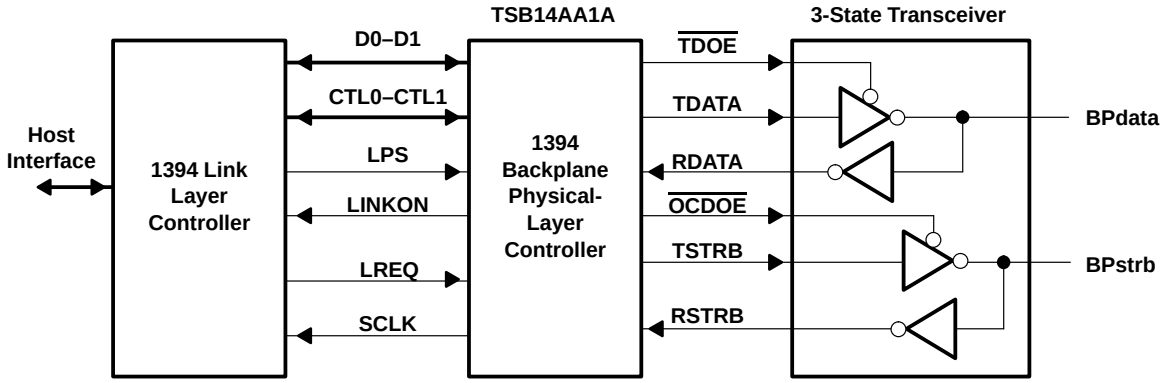
TERMINAL NAME	TERMINAL NO.	TYPE	I/O	DESCRIPTION
LPS	1	CMOS	I	Link power status input. This pin monitors the active/power status of the link layer controller and controls the state of the PHY-LLC interface. This pin must be connected to either a pulsed output that is active when the LLC is powered, or to the V_{DD} supplying the LLC through a 10-kΩ resistor. The LPS input is considered inactive if it is sampled low by the PHY for more than 128 SCLK cycles and is considered active otherwise (i.e., asserted steady high or an oscillating signal with a low time less than 2.6 μs). The LPS input must be high for at least 21 ns in order to ensure observation as high by the PHY. When the TSB14AA1A detects that LPS is inactive, it will place the PHY-LLC interface into a low–power reset state. In the reset state, the CTL and D outputs are held in the logic zero state and the LREQ input is ignored; however, the SCLK output remains active. If the LPS input remains low for more than 1280 SCLK cycles, the PHY-LLC interface is placed into a low-power disabled state in which the SCLK output is also held inactive. The PHY-LLC interface is placed into the disabled state upon hardware reset. The LLC is considered active only if the LPS input is active.
LREQ	3	CMOS	I	Link request input. The LLC uses this input to initiate a service request to the TSB14AA1A.
M-TEST	26	CMOS	I	Manufacturing tests. When M-TEST is set high, manufacturing test modes are enabled. For normal operation, this pin must be set low.
$\overline{\text{OCDOE}}$	25	CMOS	O	Open collector driver output enable pin. This pin is driven low to enable the open-collector transceivers for both TDATA and TSTRB. $\overline{\text{OCDOE}}$ is also used to enable the TSTRB transceiver when used with 3-state transceivers. When IDS is high, the output of this pin is inverted.
PD	37	CMOS	I	Power-down input. This pin is used for manufacturing tests. It should be tied to ground for normal operation.
RDATA	35	TTL	I	Receive data input. Incoming data from the external transceiver is received at the data rate set by the CLK_SELX pins and input clock frequency. When IDS is high the pin input is inverted.
$\overline{\text{RESET}}$	48	CMOS	I	Hardware reset input. When pulsed low for a minimum of (2*SCLK) seconds, a hardware reset is initiated.
RSTRB	33	TTL	I	Receive strobe input. The incoming strobe signal from the external transceiver is received at the data rate set by the CLK_SELX pins and input clock frequency. When IDS is high the pin input is inverted.
SCAN_EN	11	CMOS	I	Scan enable. When set high this pin enables the manufacturing scan test of the TSB14AA1A device. It is set low for normal operation.
SCLK	5	CMOS	O	System clock output. This pin provides a clock signal synchronized with the data transfers and output to the link. It pulses at a rate of 1/2 the data rate. At a data rate of 98.304 Mbps it oscillates at 49.152 MHz, and at a data rate of 49.152 Mbps it oscillates at 24.576 MHz.
T1P8	39		O	1.8 V regulator output. This pin is the output of the on-chip 1.8 V voltage regulator. T1P8 must be decoupled to GND with a 0.1 μF capacitor.
TDATA	29	CMOS	O	Transmit data output. Data to be transmitted is serialized on TDATA and output to the external transceiver. When IDS is high the pin output is inverted.
$\overline{\text{TDOE}}$	31	CMOS	O	3-state (high-impedance) driver output enable. This pin will only be asserted under any of the following conditions: 1. Data is transmitted after winning arbitration. 2. The arbitration state being driven is 1 (TDATA and TSTRB both = 1). 3. Bus reset is initiated. It is driven low to enable high impedance transceivers for the TDATA signal. When IDS is high the pin output is inverted.
TEST_EN	36	CMOS	I	Test enable input. When set high, this pin enables a manufacturing test mode. In normal operation, this pin must be tied to GND.
TSTRB	27	CMOS	O	Transmit strobe output. TSTRB encodes the transmit of the strobe signal and the output to the external transceiver. When IDS is high the pin output is inverted.
VCC	6, 17, 30, 42	Supply	I	3.3-V supply voltage
XI	43	Crystal	I	Crystal oscillator input. When used with an oscillator, this pin must be connected to the output of the oscillator. When operating at 98.304 Mbps this input must be 98.304 MHz. When operating at 49.152 Mbps, this input must be 49.152 MHz.
XO	45	Crystal	O	Oscillator output. When used with an oscillator, this pin must be left unconnected.

2 Detailed Description

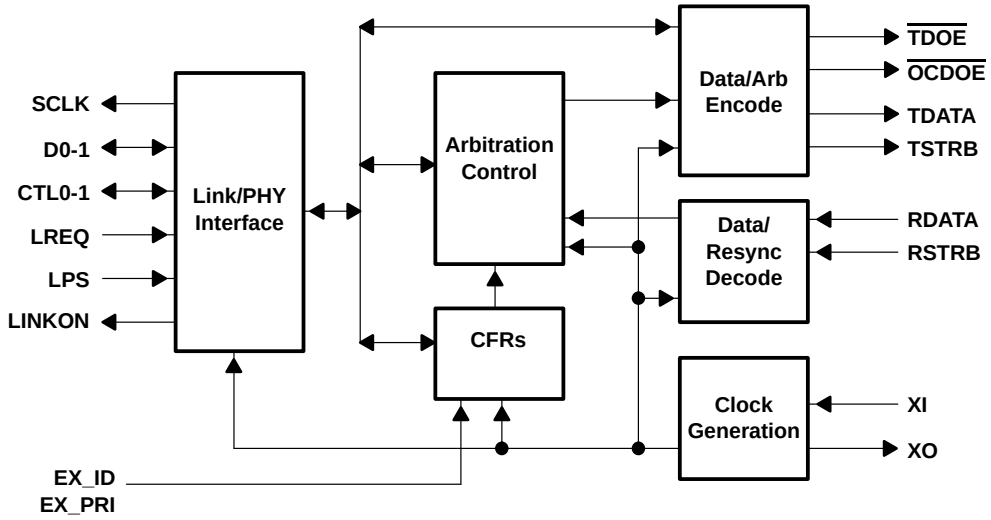
2.1 Open Collector Transceiver System Block Diagram



2.2 3-State Transceiver System Block Diagram



2.3 Functional Block Diagram



2.3.1 Link/PHY Interface

Four operations may occur on the PHY-LLC interface: link service request, status transfer, data transmit, and data receive. The LLC issues a link service request to read or write a PHY register, or to request that the PHY gain control of the serial-bus to transmit a packet. (refer to Section 5).

2.3.2 Arbitration Control

Controls the arbitrating sequence that the TSB14AA1A uses to arbitrate the bus between competing nodes (refer to Section 6).

2.3.3 Data Resync/Decode

During packet reception, the data information is received on RDATA and strobe information is received on RSTRB. The received data and strobe information is decoded to recover the received clock signal and the serial data bits, which are resynchronized to the local system clock. The serial data bits are split into two parallel streams and sent to the associated LLC.

2.3.4 Data/Arb Encode

During packet transmit, data bits to be transmitted are received from the LLC on two parallel paths and are latched internally (in the TSB14AA1A) in synchronization with the system clock. These bits are combined serially, encoded, and transmitted as the outbound data-strobe information stream. During transmit, the encoded data information is transmitted on TDATA, and the encoded strobe information is transmitted on TSTRB.

2.3.5 CFRs

The configuration registers (CFRs) control the operation of the TSB14AA1A. The register definitions are specified in Section 3.

2.3.6 Clock Generation

Provides system clock signals used to control transmission of the outbound encoded strobe and data information, synchronization of the LLC and PHY, and is used for resynchronization of the received data.

3 Internal Register Configuration

There are 10 accessible internal registers in the TSB14AA1A. The configuration of the registers is shown in Table 3–1, and corresponding field descriptions given in Table 3–2.

A reserved register or register field (marked as reserved or RSVD in the following register configuration tables) is read as 0, but is subject to future usage.

Table 3–1. Base Register Configuration

Address	BIT POSITION							
	0	1	2	3	4	5	6	7
0000	PHYSICAL_ID						R_F_TEST	
0001	TD	IBR	RESERVED					
0010	LAST_ARB_WON_PHYSICAL_ID						RSVD	E
0011	RDATA	RSTRB	XFR_SPD		E_REGISTER_COUNT			
0100	PRIORITY				RESERVED			
0101	PRODUCT IDENTIFIER				RESERVED FOR TEST			
0110	EBLREQ	IRBR	SMRST	SWHRST	LAST_ARB_WON_PRIORITY			
0111	DDLS	DSLS	ENDLS	RESERVED	TDATA	TSTRB	$\overline{\text{TDOE}}$	$\overline{\text{OCDOE}}$
1000	RESERVED FOR TEST							
1001	RESERVED FOR TEST							

Table 3–2. Base Register Field Description

FIELD	SIZE	TYPE	DESCRIPTION
RESERVED		R/W	All fields marked as reserved or RSVD must be read as 0. Whenever software is developed that writes to a register that has a reserved field, software must write a 0 to each reserved bit. In this way a bit can be added later with the default value of 0 that reverts to previous functionality. Whenever a read is done of a register that has reserved fields, software must not depend on the reserved fields to hold any particular value.
RESERVED FOR TEST		Reserved for Test	All fields marked as reserved for test or R_F_TEST may only be written to as a test to allow reading of and writing to the entire 8 bits of a register. For normal operation of the PHY the bit(s) should be set to 0. Whenever a read is done of a register that has reserved for test fields, software must not depend on the reserved for test fields to hold any particular value.
PHYSICAL_ID	6	R/W	Physical layer ID for this node. Unlike the equivalent field in the cable environment, the physical ID in the backplane environment is writeable. The power-up state of this field is 000000b. The hardware-reset state of this field is the binary state of the external ID pins on the device. This field is unaffected by bus reset (IBR, IRBR) and state machine reset (SMRST). It is reinitialized to the external pin values by a hardware reset or reset initiated by writing to the software initiated hard reset (SWHRST) bit.
TD	1	R/W	Transceiver disable. When set to 1 the PHY sets the output enable signals so that the bus transceivers are disabled. The TSB14AA1A ignores any link layer service actions that require a change to this bus output state. The power-up state of this field is 0. The state of this bit is not affected by bus resets.
IBR	1	R/W	Initiate bus-reset. When set to 1, the PHY initiates a bus request immediately (without arbitration). This bit causes assertion of the reset signal for approximately 8 μs and is self-clearing. The IBR bit may be used to initiate bus resets when open collector transceivers are implemented. In general the IRBR bit must be used to initiate bus resets instead of IBR. The IBR bit is retained for software compatibility with the TSB14CO1A when used with open-collector transceivers. When 3-state transceivers are implemented, the IRBR bit must be used to initiate bus resets. The power-up state of this field is 0.

Table 3-2. Base Register Field Description (Continued)

FIELD	SIZE	TYPE	DESCRIPTION
LAST_ARB_WON_PHY_ID	6	R	Last physical layer node ID that won arbitration. This field contains the physical ID of the node that last won the arbitration phase on the bus. This field is only valid when the E bit is 1. It is supplied for system debug purposes. The power-up state of this field is 000000b. The state of these bits is not affected by bus resets.
E	1	R	Enhanced register map. This bit is set to 1 to signify that additional extended registers beyond address 0100b are implemented. When this bit is set to 1, the values in the LAST_ARB_WON_PHY_ID, LAST_ARB_WON_PRIORITY, RDATA, RSTRB, TDATA, TSTRB, TDOE, OCDOE fields are valid. When this bit is 0 the values in these fields are not valid. The power-up state of this field is 1. This bit is always read in a TSB14AA1A as a 1.
RDATA	1	R	Received data line state. When the enhanced (E) bit is 1, the sampled and latched line state read from this field is valid. This bit reads 1 for a data bit 1 (logical 1) received by the TSB14AA1A and 0 for a data bit 0 (logical 0). The power-up state of this field is 0. This bit is updated on a best effort basis. It is not required to be toggled with every change of its namesake's input pin. It can be expected to be updated at least every 9 SCLKs, the length of the register read LREQ.
RSTRB	1	R	Received strobe line state. When the enhanced (E) bit is 1, the sampled and latched line state read from this field is valid. This bit reads 1 for a strobe line 1 (logical 1) received by the TSB14AA1A and 0 for a strobe line 0 (logical 0). The power-up state of this field is 0. This bit is updated on a best effort basis. It is not required to be toggled with every change of its namesake's input pin. It can be expected to be updated at least every 9 SCLKs, the length of the register read LREQ.
XFR_SPD	2	R	Transfer speed. These bits map exactly to the CLK_SEL0 and CLK_SEL1 pins (CLK_SEL0 is the left most bit, CLK_SEL1 is the right most bit). This enables software to verify the state of those pins and therefore the performance level of the bus transfers (100 Mbps or 50 Mbps). See the definitions for CLK_SEL0 and CLK_SEL1 for decoding. The state of these bits is not affected by bus resets or state machine resets. Upon power up, hardware reset, or SWHRST reset these bits are reloaded with the values from the CLK_SEL0 and CLK_SEL1 pins.
E_REGISTER_COUNT	4	R	Enhanced register count. When the E bit is 1, this field is valid. This field is set to 0101b to signify that there are five register addresses implemented above 0100b. The power-up state of this field is 0101b.
PRIORITY	4	R/W	Priority setting. These bits contain the priority of the local node. These bits contain the priority used in the arbitration process and transmitted as the PRI field in the packet header. The power-up state of this field is 0000b. Bit field 0 maps to priority [0] the most significant bit of the priority field used during arbitration. The hardware or SWHRST reset state of this field is the binary state of the external priority pins on the device. The state of these bits is not affected by bus resets or state machine resets. When this field is nonzero TSB14AA1A uses urgent arbitration even when a fair request is made of the PHY by the link. When this field is zero, the PHY uses fair arbitration unless the link makes an urgent request using an 11-bit LREQ, if this device is configured to accept 11-bit LRFQs.
PRODUCT_IDENTIFIER	4	R	Product identifier. This field contains the product identifier for the part. For the TSB14AA1A this field should be 0000b. Bits 0-3 are used to indicate functional changes to the design. The power-up state of this field for the TSB14AA1A is 0000b.
EBLREQ	1	R/W	Enable backplane LREQ. When this bit is set to 1, TSB14AA1A interprets all bus request LREQs from the link as 11 bits long in the backplane format. The power-up state of this field is 0b. When this bit is set to 0, TSB14AA1A interprets the bus request LREQs as being 7 bits long (standard cable LLC LREQs). The value of this bit must match the value of its corresponding bit in the attached link layer or the node will not function properly. Bus reset or state machine reset does not affect the state of this bit. This bit is cleared to 0 upon HW or SWHRST reset.
IRBR	1	R/W	Initiate robust bus reset. The IRBR bit is used when operating with 3-state transceivers to ensure a bus reset is communicated without bus contention. It works equally well for open collector transceivers. This bit is self-clearing. The power-up state of this field is 0b. This bit should be used for all SW initiated bus resets. Care should be taken that when writing to the IRBR bit, other bits in this same register are not changed. This register should be first read, then the read value should have bit 1 (the bit to be written to the IRBR field) set to 1 and the value written into the register.

Table 3-2. Base Register Field Description (Continued)

FIELD	SIZE	TYPE	DESCRIPTION
SMRST	1	R/W	State machine reset. When this bit is written to, TSB14AA1A first clears, then resets all state machines in the PHY. This bit is self-clearing. The power-up state of this field is 0b.
SWHRST	1	R/W	Software initiate hardware reset. When this bit is set to 1, TSB14AA1A performs a reset of the same nature as the reset caused by toggling the RESET pin on the device. This clears all state machines and register settings to their power-on reset states. This bit is self-clearing. The power-up state of this field is 0b.
LAST_ARB_WON_PRIORITY	4	R	Priority code of physical layer node that last won arbitration. This field contains the priority used by the node that last won the arbitration process on the bus. It is only valid when the E bit is 1. This field is supplied for system debug purposes. The power-up state of this field is 0b.
DDLS	1	R/W	Drive data line state. When the M_TEST pin is asserted (high) and the ENDLS bit is set to 1, the TSB14AA1A drives the state of the DDLS bit on the TDATA output pin of the device. This mode of operation is for diagnostic testing only. It is not a valid 1394 operating mode and will not allow proper 1394 bus operation if connected to a 1394 bus. The power-up state of this bit is 0b. The state of this bit is not affected by bus resets or state machine resets. This bit is cleared upon HW or SWHRST reset.
DSLS	1	R/W	Drive strobe line state. When the M_TEST pin is asserted (high) and the ENDLS bit is set to 1, the TSB14AA1A drives the state of the DSLS bit on the TSTRB output pin of the device. This mode of operation is for diagnostic testing only. It is not a valid 1394 operation mode and will not allow proper 1394 bus operation if connected to a 1394 bus. The power-up state of this bit is 0b. The state of this bit is not affected by bus resets or state machine resets. This bit is cleared upon hardware or SWHRST reset.
ENDLS	1	R/W	Enable drive line state. When the M_TEST pin is asserted (high) and ENDLS is set to 1, the TSB14AA1A drives the state of the DDLS bit on the TDATA output pin of the device. It also drives the state of the DSLS bit on the TSTRB output pin of the device. This mode of operation is for diagnostic testing only. It is not a valid 1394 operation mode and will not allow proper 1394 bus operation if connected to a 1394 bus. The power-up state of this bit is 0b. The state of this bit is not affected by bus resets or state machine resets. This bit is cleared upon hardware or SWHRST reset.
TDATA	1	R	Transmitted data line state. When the E bit is 1, the line state read from this field is valid. This bit reads 1 for a data line 1 (logical 1) being transmitted by the TSB14AA1A and 0 for a data line 0 (logical 0). The power-up state of this field is 0b. This bit is updated on a best effort basis. TDATA is not required to be toggled with every change of the TDATA output pin. It can be expected to be updated at least every 9 SCLKs, the length of the register read LREQ.
TSTRB	1	R	Transmit strobe line state. When the E bit is 1, the line state read from this field is valid. This bit reads 1 for a strobe line 1 (logical 1) being transmitted by the TSB14AA1A and 0 for a strobe line 0 (logical 0). The power-up state of this field is 0b. This bit is updated on a best effort basis. TSTRB is not required to be toggled with every change of the TSTRB output pin. It can be expected to be updated at least every 9 SCLKs, the length of the register read LREQ.
$\overline{\text{TDOE}}$	1	R	3-State output enable. When the E bit is 1, the state read from this field is valid. The power-up state of this field is 0b. This bit is updated on a best effort basis. $\overline{\text{TDOE}}$ is not required to be toggled with every change of the $\overline{\text{TDOE}}$ output pin. It can be expected to be updated at least every 9 SCLKs, the length of the register read LREQ.
$\overline{\text{OCDOE}}$	1	R	Open collector output enable. When the E bit is 1, the state read from this field is valid. The power-up state of this field is 0b. This bit is updated on a best effort basis. $\overline{\text{OCDOE}}$ is not required to be toggled with every change of the $\overline{\text{OCDOE}}$ output pin. It can be expected to be updated at least every 9 SCLKs, the length of the register read LREQ.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings Over Operating Junction Temperature (Unless Otherwise Noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . –0.3 V to 4 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{DD}+0.5 V
Oscillator input voltage (see Note 1) . . . . . 1.8 V
5V tolerant I/O supply voltage range, V_{DD_5V} . . . . . –0.3 V to 5.5 V
5V tolerant input voltage range, $V_{I–5V}$ . . . . . –0.5 V to V_{DD_5V}+0.5 V
Output voltage range at any output, V_O . . . . . –0.5 V to V_{DD}+0.5V
Electrostatic discharge (see Note 2) . . . . . HBM: 2 kV, MM: 200 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free air temperature, T_A (TSB14AA1A) . . . . . 0°C to 70°C
(TSB14AA1AI) . . . . . –40°C to 85°C
(TSB14AA1AT) . . . . . –40°C to 105°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground.
2. HBM is human body model, MM is machine model.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR† ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING
PFB‡	2.01 W	20.1 mW/°C	1.11 W	402 mW

† This is the inverse of the traditional junction--to-ambient thermal resistance ($R_{\theta JA}$).
‡ Standard JEDEC high-K board

4.2 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
Supply voltage, VDD		3	3.3	3.6	V
High-level input voltage, V_{IH}	CMOS input and output	$0.7\times V_{DD}$			V
	TTL inputs	2			V
Low-level input voltage, V_{IL}	CMOS input and output	0		$0.3\times V_{DD}$	V
	TTL inputs	0		0.8	V
Input voltage V_I	CMOS/TTL	0		V_{DD}	V
High-level output current, I_{OH}	CMOS Drivers			4	mA
Low-level output current, I_{OL}	CMOS Drivers			4	mA
High-level output voltage, V_{OH}	I_{OH} = max, V_{CC} = min	$0.8V_{DD}$			V
Low-level output voltage, V_{OL}	I_{OL} = min, V_{CC} = max			$0.22V_{DD}$	V
Input current	$V_I = V_{CC}$ or 0			±1	µA
High-impedance state output current, I_{OZ}	$V_I = V_{CC}$ or 0			±10	µA

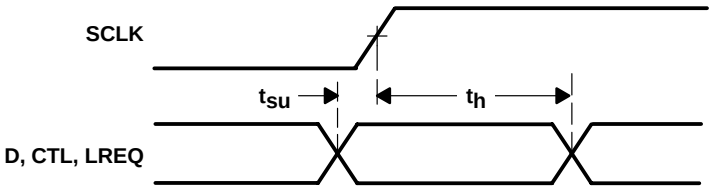
4.3 Thermal Characteristics

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Air flow	0 fpm		100.978		°C/W
			150 fpm		77.142		
			250 fpm		76.544		
			500 fpm		75.550		
$R_{\theta JC}$	Junction-to-case thermal resistance				35.483		°C/W

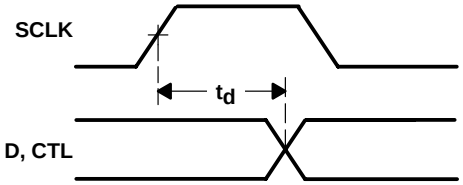
4.4 Switching Characteristics, V_{CC} = 3.3 V, T_A = 25°C (see Note 3)

PARAMETER		MEASURED	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{su}	D, CTL, LREQ low or high before SCLK high	50% to 50%	See Figure 4–1	6			ns
t_h	D, CTL, LREQ low or high after SCLK high	50% to 50%	See Figure 4–1	0			ns
t_d	Delay time, SCLK high to D, CTL high or low	50% to 50%	See Figure 4–1	0.5		13.5	ns

NOTE 3: These parameters are ensured by design and are not production tested.



D, CTL, LREQ Input Setup and Hold Times Waveforms



D, CTL Output Delay Relative to SCLK Waveforms

Figure 4–1. Parameter Measurement Information

5 Application Information

5.1 Transceiver Selection

The system designer must select transceivers appropriate for the TSB14AA1A and the link layer selected. The following are requirements for the transceivers needed:

- The transceivers used must be appropriate to the backplane technology used.
  - The various backplane technologies require different electrical characteristics in their backplanes. For example, gunning transceiver logic (GTL) uses an operating voltage on the backplane of 1.2 V and a characteristic impedance of 50 Ω [1] while low-voltage differential signaling (LVDS) uses an operating voltage of 2.4 V and a difference impedance of 100 Ω [2]. If a backplane is designed to use GTL technology, then it would be appropriate to also use that technology for the two lines dedicated to the 1394 serial bus. The drivers selected also must be able to supply the current required for the expected backplane loading. For example, backplane transceiver logic (BTL) operates correctly for a FutureBus+ [3] configuration backplane at 50 Mbits/s or for a limited number of nodes in a custom configuration at 100 Mbits/s.
- The transceivers used must be able to monitor the bus and drive the bus at the same time.
  - During arbitration, each node that is arbitrating for the bus drives its priority code and then its node number out onto the bus. During each bit period, each node reads back what has been placed on the bus. If it reads the same data it was sending, the arbitrating node stays in contention for winning the bus. If it reads something different than what it was driving, the arbitrating node loses the bus and drops out of contention. As long as each node is still sending 0s onto the bus during arbitration, all nodes are still contending to win the bus. The node with the highest priority (or if all priorities were 0, then the highest node number) is the first to drive a 1 onto the bus during arbitration. The node that sends the first 1 (asserting the bus) and reads it back wins the bus. All other nodes read back a 1, which does not match the 0 (releasing the bus) they are sending, and drop out of contention. This arbitration process requires the transceiver selected to be able to read from the bus at the same time it is driving the bus.
- The transceivers used must be appropriate for the transfer speed required.
  - The 1394 bus has two data lines that use data-strobe encoding on the bus. This requires that the transceivers be able to operate at a maximum frequency of one half of the maximum data transfer rate. When operating at 49.152 Mbits/s, the maximum frequency the drivers are required to operate at is 24.576 MHz. When operating at 98.304 Mbits/s, the maximum frequency the drivers are required to operate at is 49.152 MHz.
- Recommended transceivers:
  - When the designer has a choice of transceiver, the open collector transceiver SN74GTLP1394 [4] is recommended. This is the device used to verify lab operation at both S50 and S100 data rates.
  - When the designer must choose a differential transceiver, the 3-state transceiver SN65LVDM176 [5] is recommended. This device was also used to verify lab operation at both S50 and S100 data rates.

[1] *GTL/BTL a Low Swing Solution for High-Speed Digital Logic* (SCEA003)
(2] *Low-Voltage Differential Signaling (LVDS) Design Notes* (SLLA014)
[3] IEEE Std 896.1–1991, *IEEE Standard for FutureBus+—Logical Protocol Specification*
[4] *SN74GTLP1394, 2-Bit LVTLL-to-GTLP Adjustable-Edge Rate Bus Transceiver With Selectable Polarity* data sheet (SCES286A)
[5] *SN65LVDM176, High-Speed Differential Line Transceiver* data sheet (SLLS320D)

– When the designer must choose a backplane transceiver logic (BTL) transceiver, the FutureBus+ transceiver SN74FB2041A [6] is recommended.

– When the designer must choose a VERSA module Eurocard (VME) bus transceiver, the VME1395 is recommended (to be released).

– When the designer must choose a high speed 5-V transistor-transistor logic (TTL) transceiver, the SN74BCT756 [7] is recommended.

Refer to application report *TSB12LV01B/TSB14AA1A Reference Schematic* [8] and application report TSB14AA1A/Transceivers Reference Schematic [9] for more information.

5.2 Link Selection

The system designer must select links appropriate for the TSB14AA1A and the host interface selected. The following are requirements for the LLCs needed:

- Using the TSB14AA1A at 100 Mbits/s, any 1394 cable link layer can be used.
- Using the TSB14AA1A at 50 Mbits/s, it is appropriate to use the TSB12LV01B, TSB12LV32 (GP2Lynx), or TSB12LV21B (PCILynx), depending on the host-link interface. For example:
  - TSB12LV01B has a 32-bit data bus and is used most appropriately with a host that has 32 or 64-bit data bus.
  - TSB12LV32 is designed for interface with a Motorola-type microprocessor and should be used for an 8 or 16-bit host.
  - TSB12LV21B is best used if the host is the PCI bus.

It is necessary to verify that the CLK on the PHY-link interface is faster than the CLK on the link-host interface, based on LPS low time and detecting SCLK.

5.3 Layout Recommendation

A local clock (either 98.304 MHz for S100, or 49.152 MHz for S50) is used for the synchronization of the TSB14AA1A state machine within the PHY logic. The source of this clock must be placed as close as possible to PHY pin XI. The greater the distance, the more the chance of interference from noise. The local clock reference signal is internally divided to provide the clock signals used to control transmission of the outbound encoded strobe and data information and system clock (SCLK) sent to the link layer to synchronize the PHY-link interface.

The PHY-link interface (SCLK, LREQ, CTL[0,1], and D[0,1]) must be short (less than 4 inches if practical). The signals driven across the PHY-link interface are at 3.3 V, but are at 49.152 MHz and should be treated with due care. These signals should also be approximately the same length. The short distance is to minimize noise coupling from other devices and signal loss due to resistance. They should be kept the same length to reduce propagation delay mismatches across this synchronous interface. Refer to *Recommendations for PHY Layout* [10] for more information.

The TSB14AA1A requires an external 98.304-MHz reference oscillator input for S100 operation or 49.152-MHz for S50 operation. Because of the frequencies involved (up to 49.152 MHz system clock at 100 Mbps) the etches propagating the DATA and STRB signal in the backplane should be treated as transmission lines.

[6] *SN74FB2041A, 7–Bit TTL/BTL Transceiver* data sheet (SCBS172J)
(7] SN74BCT756, *Octal Buffer/Driver With Open-Collector Inputs* (SCBS056B)
[8] *TSB12LV01B/TSB14AA1A Reference Schematic (SLLS465)*
[9] *TSB14AA1A/Transceivers Reference Schematic* (?????????)
[10] *Recommendations for PHY Layout* (SLLA020A)

5.4 Using the EX_ID and EX_PRI Pins

During arbitration, each node that is arbitrating for the bus drives its priority code and then its arbitration number out onto the bus. The most significant bit (MSB) of the priority field is transmitted first. The least significant bit (LSB) of the priority field is followed by the MSB of the arbitration number. The lowest priority level (all zeroes) is reserved for fair arbitration, and the highest priority level (all ones) is reserved for the identification of the cycle start packet. The node with the highest priority (or if all priorities were zero, the highest node number) is the first to drive a 1 onto the bus during arbitration. The node that sends the first 1 and reads it back wins the bus. In the TSB14AA1A, the priority code and arbitration number can be set externally through the EX_PR and EX_ID pins. Upon hardware reset or SWHRST, the 4-bit priority code and 6-bit physical_ID are reinitialized to the external pin values. However, unlike the equivalent field in the cable environment, the priority and physical_ID in the backplane environment is writeable. The priority code and physical_ID of each node can be reassigned to different values other than the external pin values after the hardware reset or SWHRST.

5.5 Testability and Debug

The TSB14AA1A offers an extensive testability and debug function. The TSB14AA1A offers the following testability enhancements:

- Register 0000b may have all eight bits written to and read from for verification of *stuck at* bits or pins. Note that bits 6 and 7 must be at a logical low (0) for correct normal operation.
- Register 0010b contains the physical ID that last won the bus (sent the last packet). Note that after a robust bus reset this field becomes all ones.
- Register 0011b contains the currently captured values of the received data and received strobe pins on the device for verification of the recent state of the 1394 bus. It also contains the state of the CLK_SEL0 and CLK_SEL1 pins to verify correct setup of the TSB14AA1A.
- Register 0101 contains the product identifier for the TSB14AA1A. This allows software to verify the revision of the part that is installed in a system.
- Register 0110b contains the priority of the last packet sent on the bus. Note that after a robust bus reset this field becomes all ones.
- Register 0111b may be used to verify the state of the pins TDATA, TSTRB, $\overline{\text{OCDOE}}$, and $\overline{\text{TDOE}}$ by reading the bits with the same name.
- Register 0111b, in combination with register 0011b and the M-TEST pin, may be used to verify the connectivity of the 14AA1A, the transceiver selected and the 1394 bus. Note that this test will break the 1394 bus by driving DC states on the bus. Normal operation is *not possible* when this test mode is invoked. The connectivity test is performed as follows:
  1. Set the M_TEST pin to the HIGH state, to hardware enable this testing mode. To enable this, use a jumper, dip switch, or higher layer GPIO.
  2. Set the ENDLS bit to 1 via register write, to software enable the DC driving of the TDATA, TSTRB, $\overline{\text{OCDOE}}$, and $\overline{\text{TDOE}}$ pins.
  3. With the M_TEST pin and ENDLS register bit set to 1, write 0 to DDLS.
  4. Verify the TDATA bit reads 0 and RDATA bit reads 0
  5. With the M_TEST pin and ENDLS register bit set to 1, write 1 to DDLS.
  6. Verify the TDATA bit reads 1 and RDATA bit reads 1
  7. With the M_TEST pin and ENDLS register bit set to 1, write 0 to DSLS.
  8. Verify the TSTRB bit reads 0 and RSTRB bit reads 0
  9. With the M_TEST pin and ENDLS register bit set to 1, write 1 to DSLS.
  10. Verify the TSTRB bit reads 1 and RSTRB bit reads 1
  11. To return to normal operation, set the M_TEST pin to 0 and set the ENDLS register bit to 0. The RDATA, RSTRB, TDATA, TSTRB, $\overline{\text{TDOE}}$, and $\overline{\text{OCDOE}}$ bits will still be operational since they are read-only bits.

6 Principles of Operation

6.1 PHY/Link Interface Operation

The TSB14AA1A is designed to operate with link layer controllers (LLC) such as the Texas Instruments TSB12LV01B, TSB12LV21B, and TSB12LV32. Details of operation for the Texas Instruments LLC devices are found in the respective LLC data sheets. The following paragraphs describe the operation of the PHY-LLC interface.

The interface to the LLC consists of the SCLK, CTL0–CTL1, D0–D1, LREQ, LPS, and LINKON terminals on the TSB14AA1A, as shown in Figure 6–1.

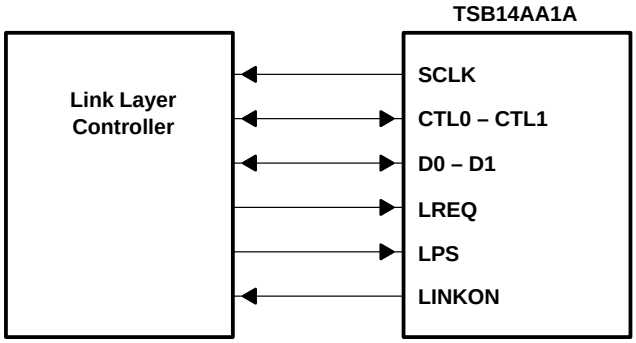


Figure 6–1. Block Diagram of the TSB14AA1A/LLC Interface

The SCLK terminal provides either a 49.152-MHz interface clock for S100 data transfers or 24.576-MHz interface clock for S50 data transfers. All control and data signals are synchronized to, and sampled on, the rising edge of SCLK.

The CTL0 and CTL1 terminals form a bidirectional control bus, which controls the flow of information and data between the TSB14AA1A and the LLC.

The D0 and D1 terminals form a bidirectional data bus, which is used to transfer status information, control information, or packet data between the devices. The TSB14AA1A supports S50 and S100 data transfers over the D0 and D1 data bus.

The LREQ terminal is controlled by the LLC to send serial service requests to the PHY in order to request access to read or write internal PHY registers, or to ask the PHY to initiate a transmit action. The PHY initiates a receive action whenever a packet is received from the serial bus.

The LPS and LINKON terminals are used for power management of the PHY and LLC. The LPS terminal indicates the power status of the LLC, and may be used to reset the PHY-LLC interface or to disable SCLK. The LINKON terminal is used to send a wake-up notification to the LLC and to indicate an interrupt to the LLC when LPS is inactive. Note that not all LLCs contain a LINKON terminal, though an external circuit to operate the wake-up mode may always be implemented at the discretion of the designer.

The TSB14AA1A normally controls the CTL0–CTL1 and D0–D1 bidirectional busses. The LLC is allowed to drive these buses only after the LCC has been granted permission to do so by the PHY.

There are four operations that may occur on the PHY-LLC interface: link service request, status transfer, data transmit, and data receive. The LLC issues a link service request to read or write a PHY register, or to request the PHY to gain control of the serial-bus in order to transmit a packet.

The PHY may initiate a status transfer either autonomously or in response to a register request from the LLC.

The PHY initiates a data transmit operation after winning control of the serial-bus following a bus-request by the LLC. The data transmit operation is initiated when the PHY grants control of the interface to the LLC.

The PHY initiates a data receive operation whenever a packet is received from the serial-bus.

The encoding of the CTL0–CTL1 bus is shown in Table 6–1 and Table 6–2.

Table 6–1. CTL Encoding When PHY Has Control of the Bus

CTL0	CTL1	NAME	DESCRIPTION
0	0	Idle	No activity (this is the default mode)
0	1	Status	Status information is being sent from the PHY to the LLC.
1	0	Receive	An incoming packet is being sent from the PHY to the LLC.
1	1	Grant	The LLC has been given control of the bus to send an outgoing packet.

Table 6–2. CTL Encoding When LLC Has Control of the Bus

CTL0	CTL1	NAME	DESCRIPTION
0	0	Idle	The LLC releases the bus (transmission has been completed).
0	1	Hold	The LLC is holding the bus while data is being prepared for transmission, or indicating that another packet is to be transmitted (concatenated) without arbitrating.
1	0	Transmit	An outgoing packet is being sent from the LLC to the PHY.
1	1	Reserved	Reserved

When the link needs to request the bus or access a register that is located in the TSB14AA1A PHY, a serial stream of information is sent across the LREQ line. The length of the stream varies depending on whether the transfer is a bus request, a read command, or a write command (see Table 6–3). Regardless of the type of transfer, a start bit of 1 is required at the beginning of the stream, and a stop bit of 0 is required at the end of the stream. Bit 0 is the MSB, and is transmitted first. The LREQ line is required to idle low (logic level 0).

Table 6–3. Request Bit Length

REQUEST TYPE	NUMBER OF BITS
Bus request (cable)	7
Bus request (backplane)	11
Read register request	9
Write register request	17

For a bus request in the cable environment, the length of the LREQ data stream is 7 bits as shown in Table 6–4.

Table 6–4. Bus Request for Cable Environment

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–3	Request type	Indicates the type of bus request (see Table 6–8 for the encoding of this field)
4–5	Request speed	Indicates the speed at which the PHY sends the packet for this request. This field has the same encoding as the speed code from the first symbol of the receive packet. See Table 6–5 for the encoding of this field. This field can be expanded to support data higher than 400 Mbit/s in the future.
6	Stop bit	Indicates the end of the transfer (always 0).

The 14AA1A will accept an LREQ transfer bus request in the backplane format. This request is 11 bits long and has the format shown in Table 6–5. This is an optional feature of the backplane environment; it allows the priority of a packet to be changed on a packet by packet basis. When using normal cable LREQs that are 7 bits long, the packet will have the priority contained in the priority register of the TSB14AA1A. For this case to change the priority requires software to change the value of the priority register inside the PHY.

Table 6–5. Bus Request for Backplane Environment

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–3	Request type	Indicates the type of bus request (see Table 6–8 for the encoding of this field)
4–5	Request speed	Ignored (set to 00 for cable S100) for backplane environment
6–9	Request priority	Indicates the priority of urgent requests. It is only used with a FairReq request type. All zeros indicate a fair request. All ones are reserved (this priority is implied by a PriReq). Other values are used to indicate the priority of an urgent request.
10	Stop bit	Indicates the end of the transfer (always 0)

For a Read Register Request the length of the LREQ data stream is 9 bits as shown in Table 6–6 (also see Table 3–2 for the bit definitions).

Table 6–6. Read Request Format

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1).
1–3	Request type	Always a 100 indicating that this is a read register request.
4–7	Address	The address of the PHY register to be read.
8	Stop bit	Indicates the end of the transfer (always 0).

For a Write Register Request the length of the LREQ data stream is 17 bits as shown in Table 6–7 (see Table 3–1 for the bit field format).

Table 6–7. Write Request Format

BIT(s)	NAME	DESCRIPTION
0	Start bit	Indicates the beginning of the transfer (always 1)
1–3	Request type	Always 101b indicating that this is a write register request
4–7	Address	The address of the PHY register to be written to
8–15	Data	The data that is to be written to the specified register address
16	Stop bit	Indicates the end of the transfer (always 0)

The 3-bit request field is defined in Table 6–8.

Table 6–8. Request Field

LREQ1	LREQ2	LREQ3	NAME	DESCRIPTION
0	0	0	ImmReq	Immediate request. When an idle is detected, the PHY takes control of the bus immediately (no arbitration).
0	1	1	Fair/Urgent Req	Fair or urgent request. The PHY arbitrates after a subaction gap using fair protocol. Fair/Urgent Req is used for fair transfers with the request priority field differentiating fair and urgent transfers for the backplane environment.
1	0	0	RdReq	Read register. Returns the specified register contents through a status transfer.
1	0	1	WrReq	Write register. Writes to the specified register.
1	1	0	Reserved	Reserved
1	1	1		

LREQ Timing is shown in Figure 6–2. Each cell represents one clock sample time.

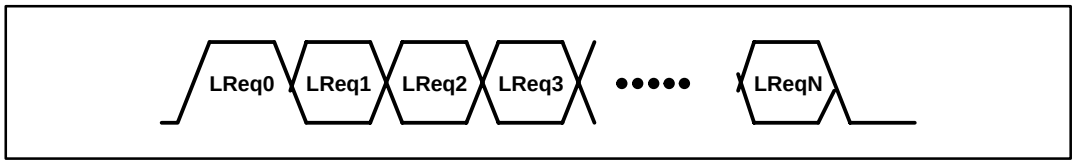


Figure 6–2. LREQ Timing

6.1.1 Bus Request

For fair or priority access, the link requests control of the bus at least one clock cycle after the PHY–link interface becomes idle. When the link senses that the CTL terminals are in a receive state (CTL0 and CTL1 = 10), then it knows that its request has been lost. This is true anytime during or after a bus request transfer by the link. Additionally, the PHY ignores any fair requests if it asserts the receive state while the link is requesting the bus. When the link finds the CTL terminals in a receive state, the link reissues the bus request transfer one clock cycle after the next interface idle.

To send an acknowledge, the link must issue an ImmReq request during the reception of the packet addressed to it. This is required because the delay from end-of-packet to acknowledge requests adds directly to the minimum delay every PHY must wait after every packet to allow an acknowledge to occur. After the packet ends, the PHY immediately takes control of the bus and grants the bus to the link. If the header cyclic redundancy check (CRC) of the packet turns out to be bad, the link releases the bus immediately. The link cannot use this grant to send another type of packet. To ensure this, the link must wait 160 ns after the end of the received packet to allow the PHY to grant it the bus for the acknowledgement, and then the link releases the bus and proceeds with another request.

Although improbable, it is conceivable that two separate nodes can believe that an incoming packet is intended for them. The nodes then issue an ImmReq request before checking the CRC of the packet. Since both PHYs seize control of the bus at the same time, a temporary, localized collision of the bus occurs. As soon as the two nodes check the CRC, the mistaken node drops its request and the false line is removed. The only side effect is the loss of the intended acknowledgement packet (this is handled by the higher-layer protocol).

Once the link issues an immediate, fair, or urgent request for access to the bus it cannot issue another request until the PHY indicates a lost (incoming packet) or won (transmit) signal. The PHY ignores new requests while a previous request is pending.

6.1.2 Read/Write Requests

For read requests (see Table 6–6), the PHY returns the contents of the addressed register at the next opportunity through a status transfer. For write requests, the PHY takes the value in the data field (see Table 6–7) of the transfer and loads it into the addressed register as soon as the transfer is complete. When the status transfer is interrupted by an incoming packet, the PHY continues to attempt the transfer of the requested register until it is successful.

6.1.3 Status

When the PHY has status information to transfer to the link, it initiates a status transfer. The PHY waits until the interface is idle to perform the transfer. The PHY initiates the transfer by asserting status (01) on the CTL terminals, along with the first two bits of status information on D0 and D1. The PHY maintains CTL status for the duration of the status transfer. The PHY can temporarily halt a status transfer by asserting something other than status on the CTL terminals. This is done in the event that a packet arrives before the status transfer completes. There must be at least one idle cycle between consecutive status transfers.

The PHY normally sends only the first 4 bits of status to the link. These bits are status flags that are needed by link state machines. The PHY sends an entire status packet to the link after a request transfer that contains a read request.

The definition of the bits in the status transfer are shown in Table 6–9 (also see Table 3–1 and Table 6–6). Status transfer timing is shown in Figure 6–3.

Table 6–9. Status Bit Description

BIT(s)	NAME	DESCRIPTION
0	Arbitration Reset Gap	Indicates that the PHY has detected that the bus has been idle for an arbitration reset gap time. This time is defined in the 1394–1995 standard†. This bit is used by the link in its busy/retry state machine.
1	Subaction Gap	Indicates that the PHY has detected that the bus has been idle for a subaction gap time. This time is defined in the 1394 standard.
2	Bus Reset	Indicates that the PHY has entered the bus reset state
3	Reserved	Reserved
4–7	Address	Holds the address of the PHY register whose contents are transferred to the link
8–15	Data	Indicates the data that is to be sent to the link

† IEEE Std 1394–1995, *IEEE Standard for a High Performance Serial Bus*

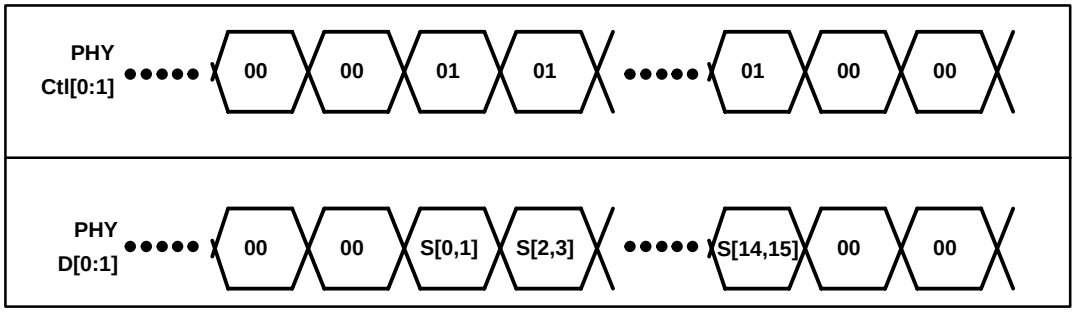


Figure 6–3. Status Transfer Timing

6.1.4 Transmit

When the link requests access to the serial bus through the LREQ terminal, the PHY arbitrates for access to the serial bus. When the PHY wins the arbitration, it grants the bus to the link by asserting transmit on the CTL terminals for one SCLK cycle, followed by idle for one cycle. After sampling the transmit state from the PHY, the link takes over control of the interface by asserting either hold or transmit on the CTL terminals. The link asserts hold to keep ownership of the bus while preparing data. The PHY asserts the data-on state on the serial bus during this time. When it is ready to begin transmitting a packet, the link asserts transmit on the CTL terminals along with the first bits of the packet. After sending the last bits of the packet, the link asserts either idle or hold on the CTL terminals for one cycle, and then idle for one additional cycle before asserting those terminals to a high-impedance state.

The hold state indicates to the PHY that the link needs to send another packet without releasing the bus. The PHY responds to this hold state by waiting the required minimum time and then asserting transmit as before. This function is used after sending an acknowledgement if the link intends to send a unified response, during a single cycle. The only requirement when sending multiples packet during bus ownership is that all packets must be transmitted at the same speed, since the speed of the packet transmission is set before the first packet.

As noted above, when the link has finished sending the last packet for the current bus ownership, it releases the bus by asserting idle on the CTL terminals for two SCLK cycles. The PHY begins asserting idle on the CTL terminals one clock cycle after sampling the second idle from the link. Whenever the D and CTL links change ownership between the PHY and the link, there is an extra clock period allowed so that both sides of the interface can operate on registered versions of the interface signals, rather than having to respond to a CTL state on the next cycle.

It is not required that the link enter the hold state before sending the first packet when implementation permits the link to be ready to transmit as soon as bus ownership is granted. The timing of a single packet transmit operation is shown in Figure 6–4. In the diagram, D0–Dn are the data symbols of the packet, ZZ represents the high-impedance state.

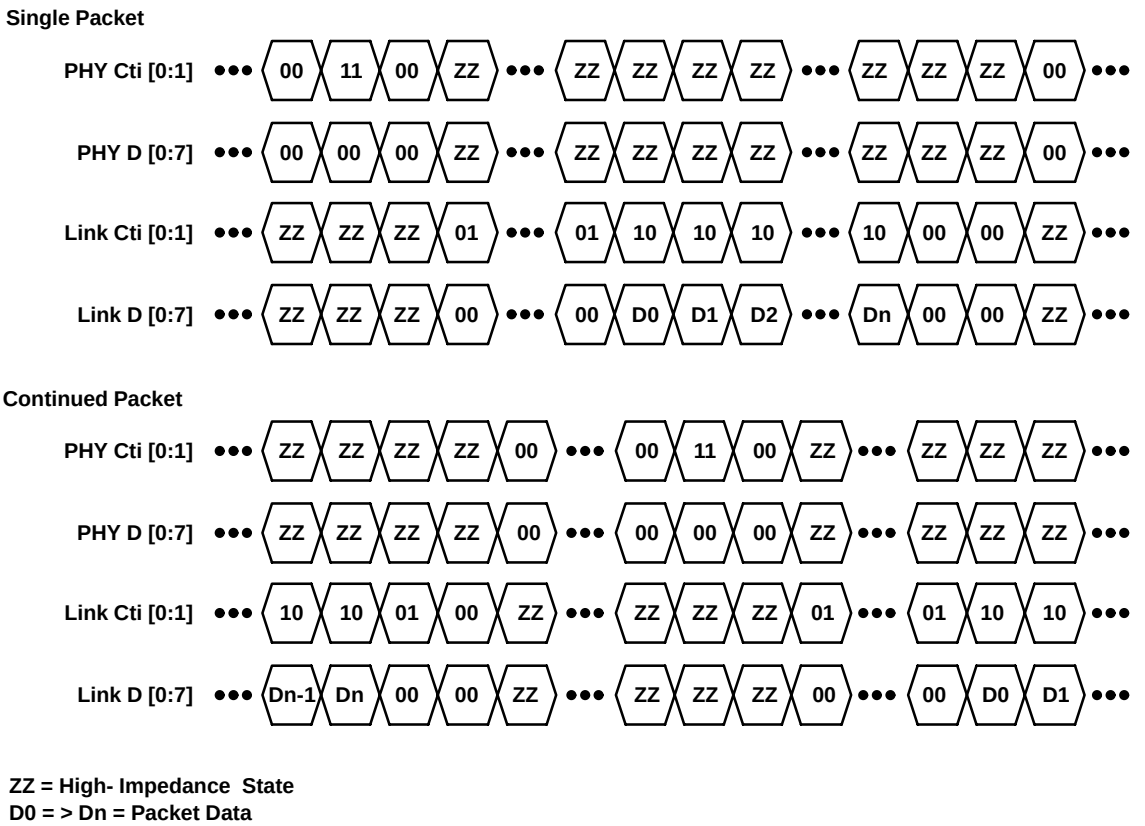
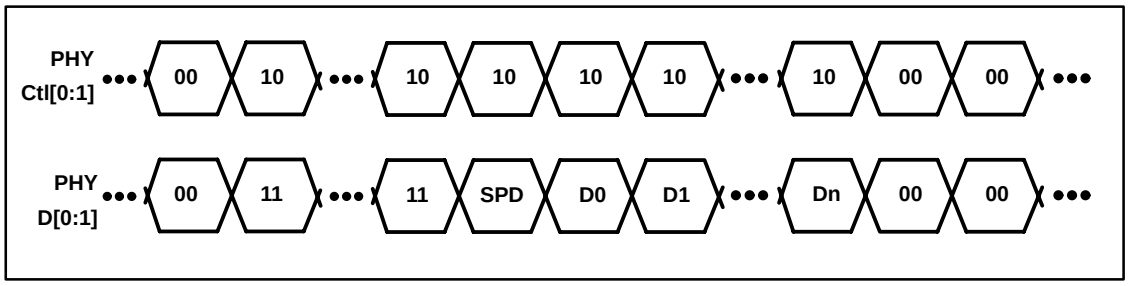


Figure 6–4. Transmit Timing

6.1.5 Receive

When data is received by the PHY from the serial bus, it transfers the data to the link for further processing. The PHY asserts receive (see Table 6–1) on the CTL lines and asserts each D terminal high. The PHY indicates the start of the packet by placing the speed code on the data bus. The PHY then proceeds with the transmission of the packet to the link on the D lines while keeping the receive status on the CTL terminals. Once the packet has been completely transferred, the PHY asserts idle on the CTL terminals, which completes the receive operation (see Figure 6–5).

NOTE: The speed code is a PHY-link protocol and is not included in the CRC.



NOTE A: SPD = Speed Code (for the backplane, this speed is fixed at D0, D1 = 00)
D0 to Dn = Packet data

Figure 6–5. Receive Timing

6.2 Backplane Environment

6.2.1 Backplane PHY Connection

Typically within a single ended signaling backplane environment, the serial bus is implemented with a pair of signals (STRB and DATA). The topology is a simple pair of bussed signals as shown in Figure 6–6.

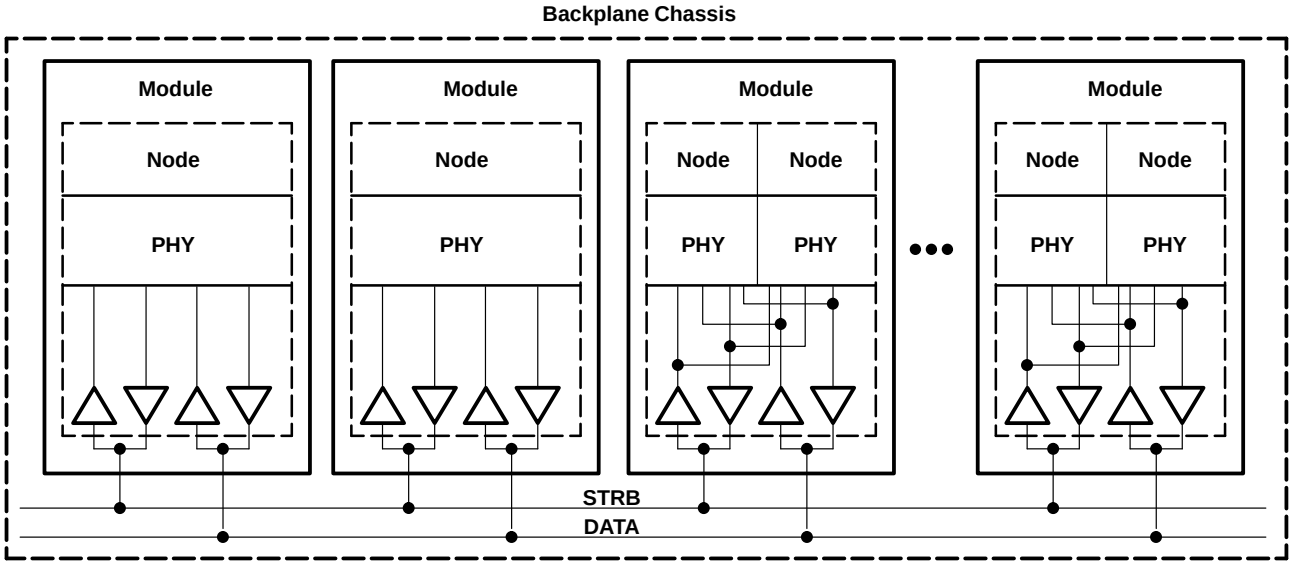


Figure 6–6. Backplane Topology

> **NOTE:** On a given bus, there can be as many as 63 nodes. There is no restriction on the distribution of nodes throughout modules on the bus. When more than one node occupies a module, they must share the same transceivers.

The backplane environment can be implemented with a number of different interface technologies. These include, but are not limited to: industry-standard gunning transistor logic plus (GTLP), industry-standard transistor-transistor logic (TTL), backplane transceiver logic (BTL) as defined by IEEE Std 1194 [10] and emitter-coupled logic (ECL).

In addition to the requirements specified by the application environment, the physical media or the serial bus should meet the requirements defined for media attachment, media signal interface, and media signal timing. Timing requirements must be met over the ranges specified in the application environment. These include temperature ranges, voltage ranges, and manufacturing tolerances.

6.2.2 Definition of Logic States

In the open collector environment, the drivers assert the bus to indicate a 1 logic state, or release the bus to indicate a 0 logic state. To assert the bus, an open collector driver sinks current. To release the bus, drivers are asserted to a high-impedance state or turned off, allowing the bus signal to be pulled to the termination voltage of the bus.

> **NOTE:** This typically results in a logical inversion of signals on GTLP, TTL and BTL buses. Signals on ECL buses typically are not inverted.

All drivers operate in a wired-ORed mode during arbitration. Drivers can operate in a totem pole mode during data packet and acknowledge transfers. In this mode, a driver can drive the bus into its released state to decrease the rise time of the bus signal (referred to as a rescinding release with TTL technology).

6.2.3 Bit Rates

Data transmission and reception occurs at 49.152 Mbit/s or 98.304 Mbit/s (±100 ppm). In normal operation, regardless of the interface technology, arbitration occurs at an arbitration clock rate of 49.152 MHz.

[10] *IEEE Std 1194.1–1991, IEEE Standard for Electrical Characteristics of Backplane Transceiver Logic (BTL) Interface Circuits*

6.2.4 Backplane Transmit Data Timing

Edge separation is the minimum required time between any two consecutive transitions of the backplane bus signals, as they appear from the output of the transmitters, whether they are transitions on the same signal or transitions on the two separate signals. A minimum edge separation is required to ensure proper operation of the data strobe bit-level encoding mechanism. TDATA and TSTRB have the relationship shown in Figure 6–7 and Table 6–10.

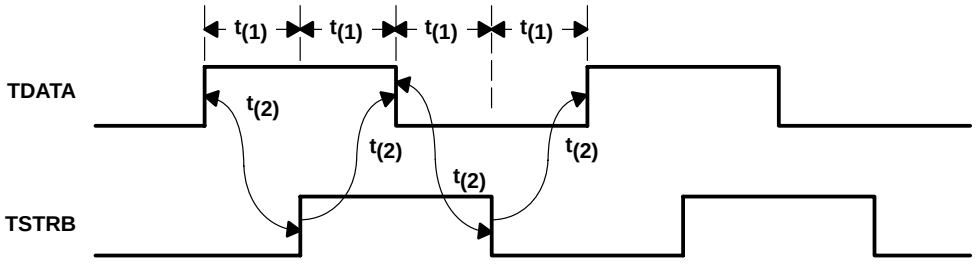


Figure 6–7. Minimum Edge Separation

Table 6–10. TSB14AA1A to Backplane Transceiver Timing

PARAMETER		98.304 MHz	49.152 MHz
$t_{(1)}$	Bit cell period for data	9.44 ns minimum	19.44 ns minimum
$t_{(2)}$†	Transmit (Tx) edge separation	8.65 ns minimum	18.65 ns minimum

† This parameter is based on a maximum total transmit skew of 2 ns.

6.2.5 Backplane Receive Data Timing

The receiver typically uses the transitions on the incoming bus signals RDATA and RSTRB to derive a clock at the code bit frequency to extract the NRZ signal on RDATA. This clock can be derived by performing an exclusive-OR (XOR) of RDATA and RSTRB.

The bus signals, as they appear from the backplane transceiver media and into the receiver, should fall within the timing constraints outlined by Figure 6–8.

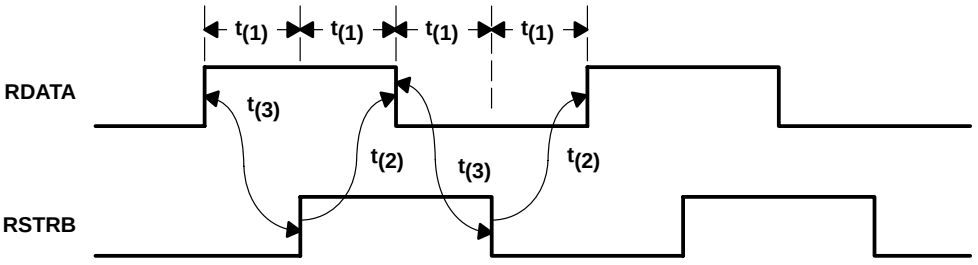


Figure 6–8. Backplane Receive Data Timing

Table 6–11. TSB14AA1A to Backplane Transceiver Timing

PARAMETER		98.304 MHz	49.152 MHz
$t_{(1)}$	Bit cell period	10.1715 ns nominal	20.34 nominal
$t_{(2)}$†	Receive (Rx) edge separation	3.4 ns minimum	3.4 ns minimum
$t_{(3)}$†		16.3 ns maximum	36.6 ns maximum

† This parameter is based on a maximum total transmit skew of 2 ns and a maximum backplane skew of 0.5 ns. This assumes total receive skew is less than receive edge separation (i.e., some skew margin exists).

6.2.6 Backplane Timing Definitions

- Logic Skew—The skew between data and strobe within the physical layer itself due to internal skews between data and strobe logic.
- Spatial Skew—The skew between data and strobe due to differences in propagation delays along the transmission line from the arbiter to the transceiver.
- Package Skew—The propagation delay difference through the transceiver between the data and strobe channels.
- Backplane Skew—The skew along the backplane itself due to impedance and/or mismatched data and strobe line length.
- Receive Setup/Hold—The setup and hold time needed to latch the incoming data within the PHY arbiter, based on the recovered clock from Data_Rx and Strb_Rx.
- Total Transmit Skew—The total skew between data and strobe in transmitting data from the PHY out to the bus. This is given by the following equation:

  Total Transmit Skew = Transmit Package Skew + Spatial Skew + Logic Skew
- Total Receive Skew—The total skew between data and strobe in receiving data from the bus into the PHY. This is given by the following equation:

  Total Receive Skew = Receive Package Skew + Spatial Skew + Receive Setup + Receive Hold
- Skew Margin—The bit cell period minus all skews. This is given by the following equation:

  Skew Margin = Bit Cell Period – Total Transmit Skew – Backplane Skew – Total Receive Skew
- Transmit Edge Separation—The minimum time required between any two consecutive transitions of the bus signals to ensure proper operation of data-strobe bit level encoding. Transmit edge separation is measured from the midpoint of the signal transition to the midpoint of the next signal transition out on the bus. Minimum transmit edge separation is the minimum bit cell period less the maximum total transmit skew.
- Receive Edge Separation—The minimum time required between any two consecutive transitions of the bus signals to ensure proper operation of data-strobe bit level decoding. Receive edge separation is measured from the midpoint of the signal transition to the midpoint of the next signal transition out on the bus. This is the minimum bit cell period reduced by the amount of maximum total transmit skew and maximum backplane skew.

6.2.7 Gap Timing

A gap is a period of time during which the bus is idle (Data_Rx and Strb_Rx are unasserted). There are three types of gaps:

- Acknowledge Gap—Appears between the end of a packet and an acknowledge, as well as between isochronous transfers. A node should detect the occurrence of an acknowledge gap after the bus has been in an unasserted state for 4 arbitration clock times (approximately 81.38 ns) but should not assert the bus until a total of 8 arbitration clock times (approximately 182.76 ns) have occurred. This requirement ensures that a node is given adequate time to detect the acknowledge gap before the bus is asserted by another node upon detecting an acknowledge gap. This includes the minimum time required to detect a Bus_Idle (4 arbitration clock times), as well as the maximum delay between the arbitration state machine within any two nodes on the bus (another 4 arbitration clock times).
- Subaction Gap—Appears before asynchronous transfers within a fairness interval. A node should detect the occurrence of a subaction gap after the bus has been in an unasserted state for at least 16 arbitration clock times (approximately 325.52 ns), but should not assert the bus until a total of 20 arbitration clock times (approximately 406.9 ns) have occurred. This requirement ensures that a node is given adequate time to

detect the subaction gap before the bus is asserted by another node (upon detecting a subaction gap). The duration of the subaction gap ensures that another node asserting the bus after an acknowledge gap has been detected by this time.

- Arbitration Reset Gap—Appears before asynchronous transfers when the fairness interval starts. A node should detect the occurrence of an arbitration reset gap after the bus has been in an unasserted state for at least 28 arbitration clock times (approximately 569.66 ns), but should not assert the bus until a total of 32 arbitration clock times (approximately 651.04 ns) have occurred. This requirement ensures that a node is given adequate time to detect the arbitration reset gap before the bus is asserted by another node (upon detecting an arbitration reset gap). The duration of the arbitration reset gap ensures that another node asserting the bus after a subaction gap or an acknowledge gap has been detected by this time.

  If a node is waiting for the occurrence of a particular gap and the bus has become idle for the specified time (e.g., 32 arbitration clock times for an arbitration reset gap), the node detects the gap and asserts the bus. An asserted signal propagates through the node decision/transceiver circuitry and onto the bus soon enough to allow arbitration to occur properly.

6.3 Arbitration Sequence

The TSB14AA1A uses a particular arbitration sequence to arbitrate the bus between competing modules. The sequence used consists of a 4-bit priority field and a 6-bit arbitration number field.

6.3.1 Priority

Within the arbitration sequence, the arbitration number is preceded by four bits that define a priority level. The method by which priority is assigned is to be determined by the system integrator with two exceptions. The lowest priority (all zeros) is reserved for fair arbitration and the highest priority (all ones) is reserved for cycle start requests. This allows 14 priority levels to be used for the urgent arbitration process.

The use of an urgent priority class allows nodes to be granted a large portion of the bandwidth on the bus. High priority nodes are granted the bus before lower priority nodes during urgent allocation of the bus, allowing such nodes to be granted more bandwidth.

In order to ensure forward progress, the lowest priority level is reserved for fair arbitration. This allows all nodes arbitrating with this priority level to be allowed one fair access to the bus for each fairness interval. For fair arbitration, the value of the arbitration number has a minimal impact on the allocation of the bus. Although nodes with higher arbitration numbers are granted the bus sooner, there is only a small decrease in latency.

6.3.2 Arbitration Number

The arbitration sequence uses a unique arbitration number for each module. This 6-bit number is the same as the node Physical_ID. When less than 6-bits are provided for the arbitration number, they occupy the MSBs of the arbitration number. The remaining bits are zero-filled. The MSBs are transmitted first.

> **NOTE:** If the serial bus is contained within a host backplane, it is expected that the arbitration number (i.e., Physical_ID) is set by the host backplane at power up (e.g., with a built-in slot identifier or configuration mechanism).

This number is software programmable to facilitate testing and to allow for consistent system operation and repeatability.

6.3.3 Arbitration Sequence Format

The following format for the arbitration sequence is used:

PRIORITY	ARBITRATION NUMBER
4-bits	6-bits

- Each module on the backplane has unique 6-bit arbitration number that is equal to the nodes Physical_ID.
- The arbitration number is preceded by four bits of priority. The MSB of the priority field is transmitted first. The LSB of the priority field is followed by the MSB of the arbitration number.
- Dynamic assignment of priority is accommodated.
- The lowest priority level (all zeroes) is reserved for fair arbitration, and the highest priority level (all ones) is reserved for the identification of the cycle start packet.

6.4 Arbitration

Unless a node is using immediate arbitration to access the bus (in which case there is no contention for the bus), it is possible that more than one node can attempt to access the bus at a given time. Consequently, it is necessary for a node to arbitrate for the bus in order to gain access to the bus.

> **NOTE:** A node uses immediate arbitration to send an acknowledge. Since there is no contention for the bus in this case, arbitration is not necessary. A node that is transmitting an acknowledge does not arbitrate for the bus, but merely waits for an acknowledge gap to be detected before it begins transmission. If a node is attempting to gain access to the bus without using immediate access, it must first arbitrate for the bus.

Arbitration occurs in response to a PHY arbitration request from the link. Nodes begin arbitrating once the bus has become idle for a predetermined amount of time (the appropriate gap indication occurs). Once this happens, nodes begin a bit-by-bit transmission of their arbitration sequence.

A node can obtain access to the bus in a limited number of ways. Since some arbitration classes allow nodes to begin arbitration before others, nodes arbitrating with certain arbitration classes can detect that the bus is busy before they can begin to arbitrate. In this way, certain arbitration classes can be bypassed, e.g., fair and urgent nodes do not get a chance to arbitrate when another node is sending an acknowledge.

The backplane environment supports the fair, urgent, and immediate arbitration classes.

6.4.1 Fairness Intervals

The fairness protocol is based on the concept of a fairness interval. A fairness interval consists of one or more periods of bus activity separated by short idle periods called subaction gaps and is followed by a longer idle period known as an arbitration reset gap. At the end of each gap, bus arbitration is used to determine the next bus owner. This concept is shown in Figure 6–9.

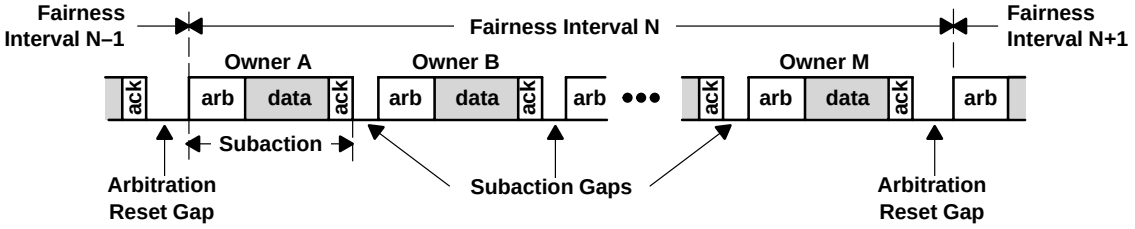


Figure 6–9. Fairness Interval

The implementation of the fair arbitration protocol is defined in terms of these fairness intervals as is discussed in the following paragraphs.

6.4.2 Fair Arbitration

When using this arbitration class, an active node can send an asynchronous packet exactly once each fairness interval. Once a subaction gap is detected, a node can begin arbitration when its Arbitration_Enable signal is set. The Arbitration_Enable signal is set at the beginning of the fairness interval and is cleared when the node successfully accesses the bus through fair arbitration. This disables further fair arbitration attempts by that node for the remainder of the fairness interval. In the absence of urgent nodes, a fairness interval ends once all of the nodes attempting fair arbitration have successfully accessed the bus. At this time, all of the fair nodes have their Arbitration_Enable signals reset and cannot arbitrate for the bus. The bus remains idle until an arbitration reset gap occurs. Once this happens, the next fairness interval begins. All of the nodes set their Arbitration_Enable signal and can begin to arbitrate for the bus. This process is illustrated in Figure 6–10.

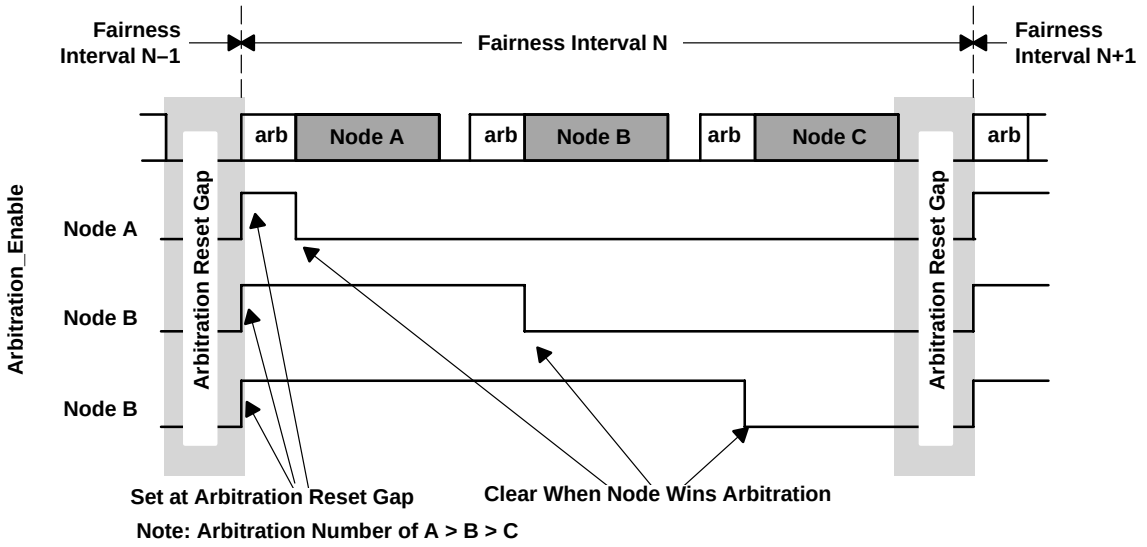


Figure 6–10. Fair Arbitration Timing

NOTE: A node sending a concatenated subaction does not reset its Arbitration_Enable bit.

6.4.3 Urgent Arbitration

The backplane environment enhances the fair priority algorithm by splitting access opportunities among nodes based on two priority classes: fair and urgent. Nodes using an urgent priority can use up to three-fourths of the access opportunities, with the remaining equally shared among nodes using the fair priority. All nodes are required to implement the fair priority class, while the urgent priority class is optional. Packets are labeled as urgent when that priority class is used.

The fair/urgent allocation uses the same fairness interval described in fair arbitration but accompanies the Arbitration_Enable flag with an Urgent_Count. The fair/urgent method works as follows:

- When the bus is idle for longer than an arbitration reset gap, a fairness interval begins and all nodes set their Arbitration_Enable flags, while nodes implementing urgent priority set their Urgent_Count to three.
- A node that is waiting to send a packet using the fair priority class should begin arbitrating after detecting a subaction gap as long as its Arbitration _Enable flag is set. When its Arbitration_Enable flag is cleared, it waits for an arbitration reset gap before it begins arbitrating. When such a node wins an arbitration contest, it sends a packet without the urgent label and its Arbitration_Enable flag is cleared.
- A node that is waiting to send a packet with urgent priority begins arbitrating after detecting a subaction gap if its Urgent_Count is nonzero. When its Urgent_Count is zero, it waits for an arbitration reset gap before it begins arbitrating. Whenever such a node wins an arbitration contest, it sends a packet with the urgent label.

- A node implementing urgent priority sets its Urgent_Count to three whenever an unlabeled (i.e., fair) packet is transmitted or received. This includes received packets that are addressed to other nodes.
- A node decrements its Urgent_Count whenever a packet with the urgent label is transmitted or received. This includes received packets that are addressed to other nodes. This ensures that there is at most three urgent packets for every fair packet. This does not ensure that every node using urgent priority obtains the bus three times for each fairness interval. The node arbitrating with the highest priority always obtains the bus before other nodes arbitrating with an urgent, but lower, priority.

In the presence of urgent nodes, a fairness interval ends after the final fair node and up to three remaining urgent nodes have successfully accessed the bus. Since all fair nodes now have their Arbitration_Enable signals reset and all urgent nodes have their Urgent_Count decremented to zero, none of the nodes can access the bus. The bus remains idle until an arbitration reset gap has occurred, re-enabling arbitration on all nodes and starting the next fairness interval. This process is illustrated in Figure 6–11, which illustrates a situation where there are three nodes arbitrating for the bus with Physical_IDs such that A has the highest priority, B is in the middle priority, and C has the lowest priority. Nodes A and C are using fair priority and node B is using urgent priority.

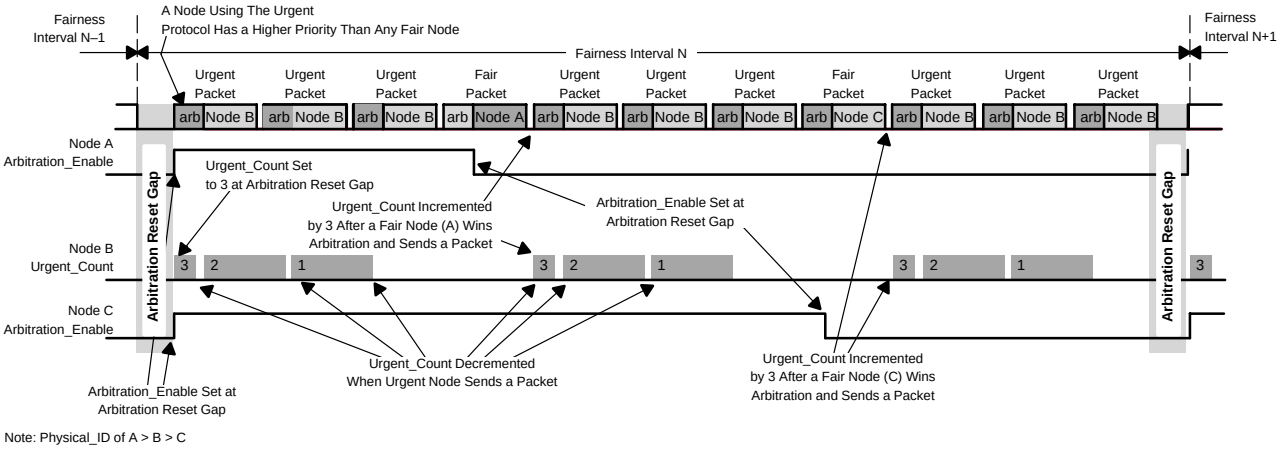


Figure 6–11. Urgent Arbitration

In the backplane environment, the natural priority is the concatenation of the 4-bit urgent priority level with the Physical_ID. These results are listed as follows.

- A node using the urgent priority always wins an arbitration contest over all nodes using the fair priority.
- The node using the highest priority level wins the arbitration level.
- When more than one node uses the highest priority level, then the one with the highest Physical_ID wins.

6.4.4 Immediate Arbitration

This arbitration class is used by nodes sending an acknowledge to a received packet. Transmission of the acknowledge (beginning with a Data_Prefix) occurs as soon as an acknowledge gap is detected. This arbitration class is referred to as immediate because an arbitration sequence is not transmitted to obtain access to the bus (i.e., the node does not actually arbitrate for the bus).

6.5 Reset

6.5.1 Backplane PHY Reset

Upon a power reset event (i.e., power up) registers and control and status registers (CSRs) associated with the operation of the PHY are initialized to their default values. State machines associated with PHY operations are initialized. The Bus_Reset signal is not transmitted on the bus by the PHY.

6.5.2 Bus Reset

Once a PHY control request of Bus_Reset is communicated from the node controller to the PHY the PHY communicates a Bus_Reset onto the bus.

> **NOTE:** Since a PHY transmitting a Bus_Reset must also react accordingly once the Bus_Reset event is detected, its state machines do have the opportunity to advance beyond those of other nodes. This ensures that all nodes are in a somewhat similar state after such a Bus_Reset event.

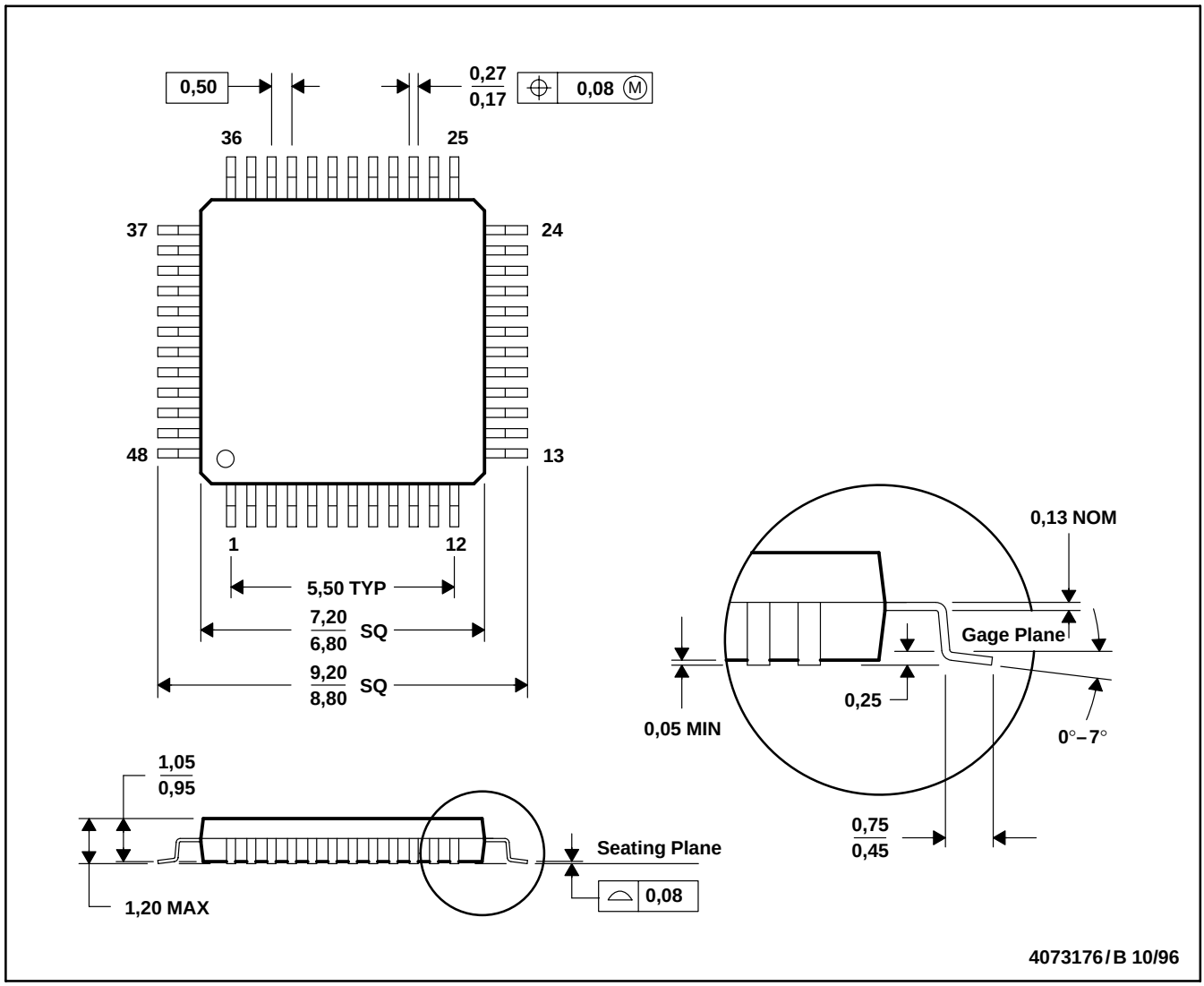
Once a PHY detects that a Bus_Reset event has occurred on the bus, it communicates a bus reset status to the LLC. The node controller initializes a bus reset by writing to the PHY control register with the IBR bit or IRBR bit set to 1. The PHY hardware resets the IBR and IRBR bit to zero on detection of its own bus reset.

6.6 Live Insertion

It is up to the user to design the node or module to safely receive power from the particular backplane they are using during a live insertion. But in principle, live insertion is supported and does not cause a bus reset event to occur.

7 Mechanical Information

PFB (S-PQFP-G48) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026