1100-MHz Twin PLL

Description

The IC U2782B is a low-power twin PLL manufactured with TEMIC Semiconductors' advanced UHF process. The maximum operating frequency is 1100 MHz for both PLLs. The device features a wide supply-voltage range from 2.7 V to 5.5 V. A prescaler 64/65 and power-down function for both PLLs are integrated. The twin PLL is designed for CT1, IS54, JDC etc applications.

Electrostatic sensitive device.
Observe precautions for handling.

Features

- Very low current consumption (typical 3 V/11 mA)
- Supply-voltage range 2.7 to 5.5 V
- Maximum input frequency: 1100 MHz for both PLLs
- 2 pins for separate power-down functions
- Output for PLL lock status
- Prescaler 64/65 for both inputs
- SSO20 package
- ESD protected according to MIL-STD 833 method 3015 cl.2

Benefits

- Low current consumption leads to extended talk time
- Twin PLL saves costs and space
- One foot print for all TEMIC Semiconductors' twin PLLs saves design-in time

Block Diagram

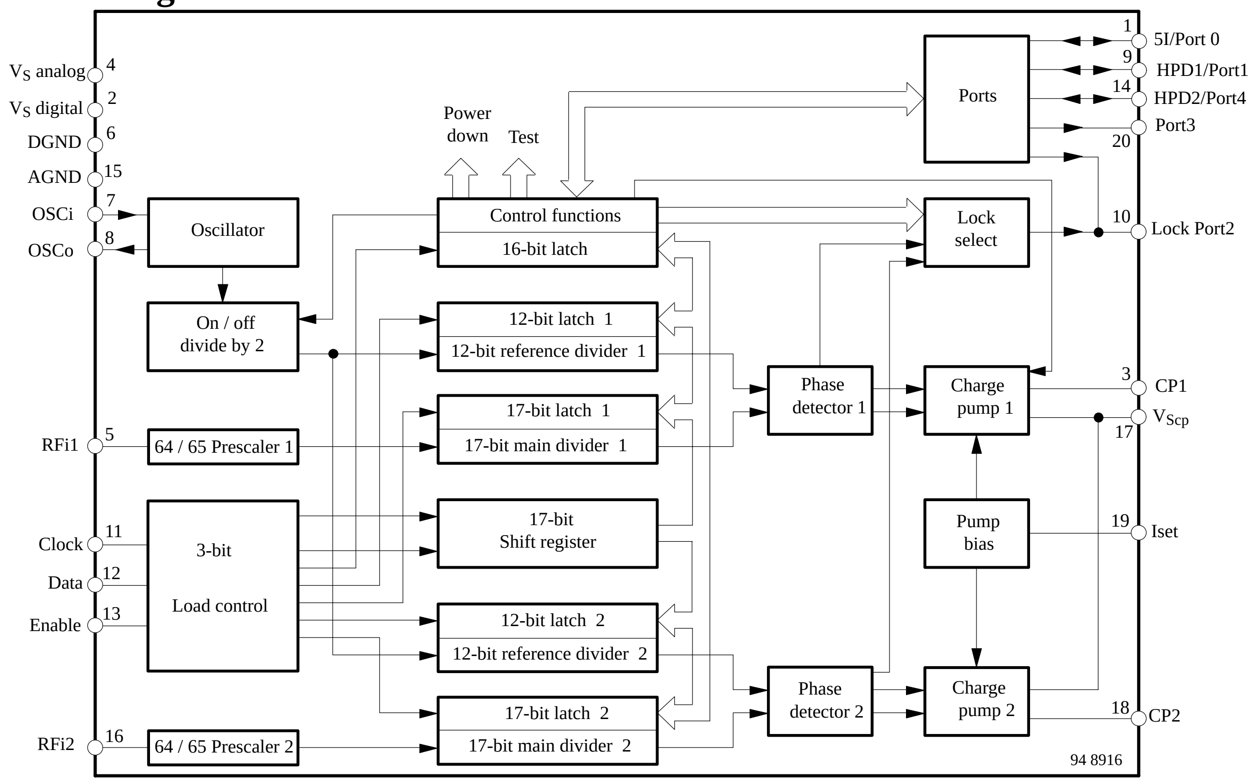


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U2782B-AFS	SSO20	Tube, MOQ 830 PCS
U2782B-AFSG3	SSO20	Taped and reeled, MOQ 4000 pcs

Pin Description

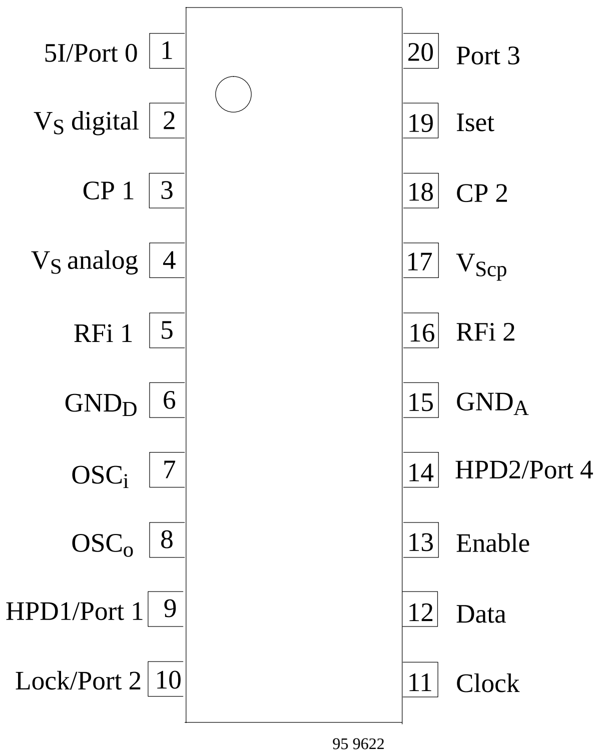


Figure 2. Pinning

Pin	Symbol	Function
1	5I/Port 0	5I – Control input / o.c.output
2	V_S digital	Power supply digital section
3	CP 1	Charge-pump output of synthesizer 1
4	V_S analog	Power supply analog section
5	RFi 1	RF divider input synthesizer
6	GND_D	Ground for digital section
7	OSC_i	Reference-oscillator input
8	OSC_o	Reference-oscillator output
9	HPD 1/ Port 1	Hardware power-down input of synthesizer 1 / o.c.output
10	Lock/ Port 2	Lock output / o.c.output / testmode output
11	Clock	3-wire bus: serial clock input
12	Data	3-wire bus: serial data input
13	Enable	3-wire bus: serial enable input
14	HPD 2/ Port 4	Hardware power-down input of synthesizer 2 / o.c.output
15	GND_A	Ground for analog section
16	RFi 2	RF divider input synthesizer 2
17	V_{Scp}	Charge-pump supply voltage
18	CP 2	Charge-pump output of synthesizer 2
19	Iset	Reference pin for charge-pump currents
20	Port 3	o.c.output

Absolute Maximum Ratings

Parameters		Symbol	Value	Unit
Supply voltage	Pins 2, 4 and 17	V_S, V_{Scp}	6	V
Input voltage	Pins 1, 3, 5, 8, 9, 10, 11, 12, 13, 14, 15, 16, 18 and 20	V_i	0 to V_S	V
Junction temperature		T_j	125	°C
Storage temperature range		T_{stg}	–40 to +125	°C

Operating Range

Parameters		Symbol	Value	Unit
Supply voltage	Pins 2, 4 and 17	V_S, V_{Scp}	2.7 to 5.5	V
Ambient temperature range		T_{amb}	–40 to +85	°C

Thermal Resistance

Parameters		Symbol	Value	Unit
Junction ambient	SSO20	R_{thja}	140	K/W

Electrical Characteristics

T_{amb} = 25°C, V_S = 2.7 to 5.5 V, V_{Scp} = 5 V, unless otherwise specified

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
DC supply						
Supply current	V_S = 3 V, SPD1 = SPD2 = 0	I_S	0.5	0.8	1.1	mA
Supply current	V_S = 3 V, SPD1 = SPD2 = 1	I_S	7	11	13	mA
Supply current CP	V_{CP} = 5 V, PLL in lock condition	I_{CP}	0	1	10	µA
PLL 1 + PLL2						
Input voltage	f_{RFi1} = 200 – 1100 MHz	V_{RFi1}	20		200	mV_{RMS}
Scaling factor prescaler		S_{PSC}		64/65		
Scaling factor main counter		S_M	5		2047	
Scaling factor swallow counter		S_S	0		63	
Reference counter		S_R	5		4096	
Reference oscillator						
Recommended crystal series resistance			10		200	Ω
External reference input frequency	AC-coupled sinewave RF/2 = 0 RF/2 = 1	OSC_i	 1 1		 20 40	MHz
External reference input amplitude	AC-coupled sinewave [2]	OSC_i		100		mV_{RMS}
Logic input levels (Clock, Data, Enable, HPD1, HPD2, 5I)						
High input level		V_{iH}	1.5			V
Low input level		V_{iL}	0		0.4	V
High input current		I_{iH}	–5		5	µA
Low input current		I_{iL}	–5		5	µA
Logic output levels (Port 0, 1, 2, 3, 4, Lock)						
Leakage current	V_{OH} = 5.5 V	I_L			10	µA
Saturation voltage	I_{OL} = 0.5 mA	V_{SL}			0.4	V
Charge-pump output (R_{set} = 10 kΩ)						
Source current	$V_{CP} \leqq V_{Scp}/2$ PLL2 5I = L PLL1 5I = H PLL1	I_{source}		– 1 –0.2 –1		mA
Sink current	$V_{CP} \leqq V_{Scp}/2$ PLL2 5I = L PLL1 5I = H PLL1	I_{sink}		1 0.2 1		mA
Leakage current	$V_{CP} \leqq V_{Scp}/2$	I_L		± 5		nA

[1] RMS voltage at 50 Ω; [2] OSC_o is open if an external reference frequency is applied

Serial Bus Programming

Reference and programmable counters can be programmed by the 3-wire bus (Clock, Data and Enable). After setting the enable signal to high condition, the data status is transfered bit by bit on the rising edge of the clock signal into the shift register, starting with the MSB bit. When the enable signal has returned to low condition the programmed information is loaded according to the address bits (last three bits) into the addressed latch. Additional leading bits are ignored and there is no check made how many clock pulses arrived during enable high condition. In power-down mode the 3-wire bus remains active and the IC can be programmed.

Data is entered with the most significant bit first. The leading bits deliver the divider or control information. The trailing three bits are the address field. There are six different addresses used. The trailing address bits are decoded upon the falling edge of the enable signal. The internal load pulse starts with the falling edge of the enable signal and ends with the falling edge of the clock signal. Therefore, a minimum holdtime clock-enable t_{HCE} is required.

Bit Allocation

MSB																			LSB
Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15	Bit 16	Bit 17	Bit 18	Bit 19	Bit 20
Data bits																	Address bits		
D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A2	A1	A0
PLL1 M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	S5	S4	S3	S2	S1	PLL1 S0	0	0	1
					PLL1 R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	PLL1 R0	0	1	0
PLL2 M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	S5	S4	S3	S2	S1	PLL2 S0	0	1	1
					PLL2 R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	PLL2 R0	1	0	0
	RF/2	Test	5IP	TRI 2	TRI 1	PS2	PS1	H2P	H1P	LPB	LPA	P4	P3	P2	P1	P0	1	0	1
														SP D 5I	SP D 2	SP D 1	1	1	0

Scaling Factors

S0 ... S5: These bits are setting the swallow counter S_S.
$T_S = S0*2^0 + S1*2^1 + ... + S4*2^4 + S5*2^5$
allowed scaling factors for S_S: 0 ... 63, $T_S < T_M$

M0 ... M10: These bits are setting the main counter S_M.
$T_M = M0*2^0 + M1*2^1 + ... + M9*2^9 + M10*2^{10}$
allowed scaling factors for S_M: 5 ... 2047

S_{PGD}: Total scaling factor of the programmable counter:
$S_{PGD} = (64*S_M) + S_S$ Condition: $S_S < S_M$

R0 ... R11: These bits are setting the reference counter S_R.
$S_R = R0*2^0 + ... + R10*2^{10} + R11*2^{11}$
allowed scaling factors for S_R: 5 ... 4096

S_{RFD}: Total scaling factor of the reference counter:

RF/2 = 1: $S_{RFD} = 2 * S_R$

RF/2 = 0: $S_{RFD} = S_R$

Serial Programming Bus

Control Bits:

P0 ... P4: o.c. output ports (1 = high impedance)

LPA, LPB: selection of P2 output or locksignal function of Pin 10

TEST	LPA	LPB	
0	0	0	o.c. output P2
0	0	1	locksignal of synthesizer 2
0	1	0	locksignal of synthesizer 1
0	1	1	wiredor locksignal of both synthesizer

H1P, H2P: selection of P1/4 output or hardware power-down input of synthesizer 1/2 (0 = Port / 1 = HPD)

5IP: selection of P0 output or high-current switching input for the charge-pump current of synthesizer 1 (0 = Port / 1 = charge-pump 1 current switch input)

PS1, PS2: phase selection of synthesizer 1 and synthesizer 2 (1 = normal / 0 = invers)

	PS-PLL1/2 = 1	PS-PLL1/2 = 0
	CP1/2	CP1/2
$f_R > f_P$	I_{sink}	I_{source}
$f_R < f_P$	I_{source}	I_{sink}
$f_R = f_P$	0	0

RF/2: divide-by-2 prescaler for reference divider (0 = off / 1 = on)

SPD1, SPD2: software power-down bit of synthesizer 1/2 (0 = powe down / 1 = power up)

5I: software switch for the charge-pump current of synthesizer 1 (0 = low current / 1 = high current)

TRI1, TRI2: enables tristate for the charge pump of synthesizer 1/2 (0 = normal / 1 = tristate)

TEST: enables counter testmode (0 = disabled / 1 = enabled)

TEST	LPA	LPB	PS1	PS2	Testsignal at pin 10
1	1	0	1	x	RFD1
1	1	0	0	x	PGD1
1	0	1	x	1	RFD2
1	0	1	x	0	PGD2

To operate the software power-down mode, the following condition must be set: HXP = 0; power up and power down will be set by SPDX = 1 (on) and SPDX = 0 (off).
To operate the hardware power-down mode, the following condition must be set: HXP = 1; SPDX = 1; power up and power down will be set by high and low state at the hardware power-down Pins 9/14.
High current of charge-pump synthesizer 1 is active when 5I = 1 and if 5IP = 1 the charge-pump current control input Pin 1 is in high state.

Application Circuit

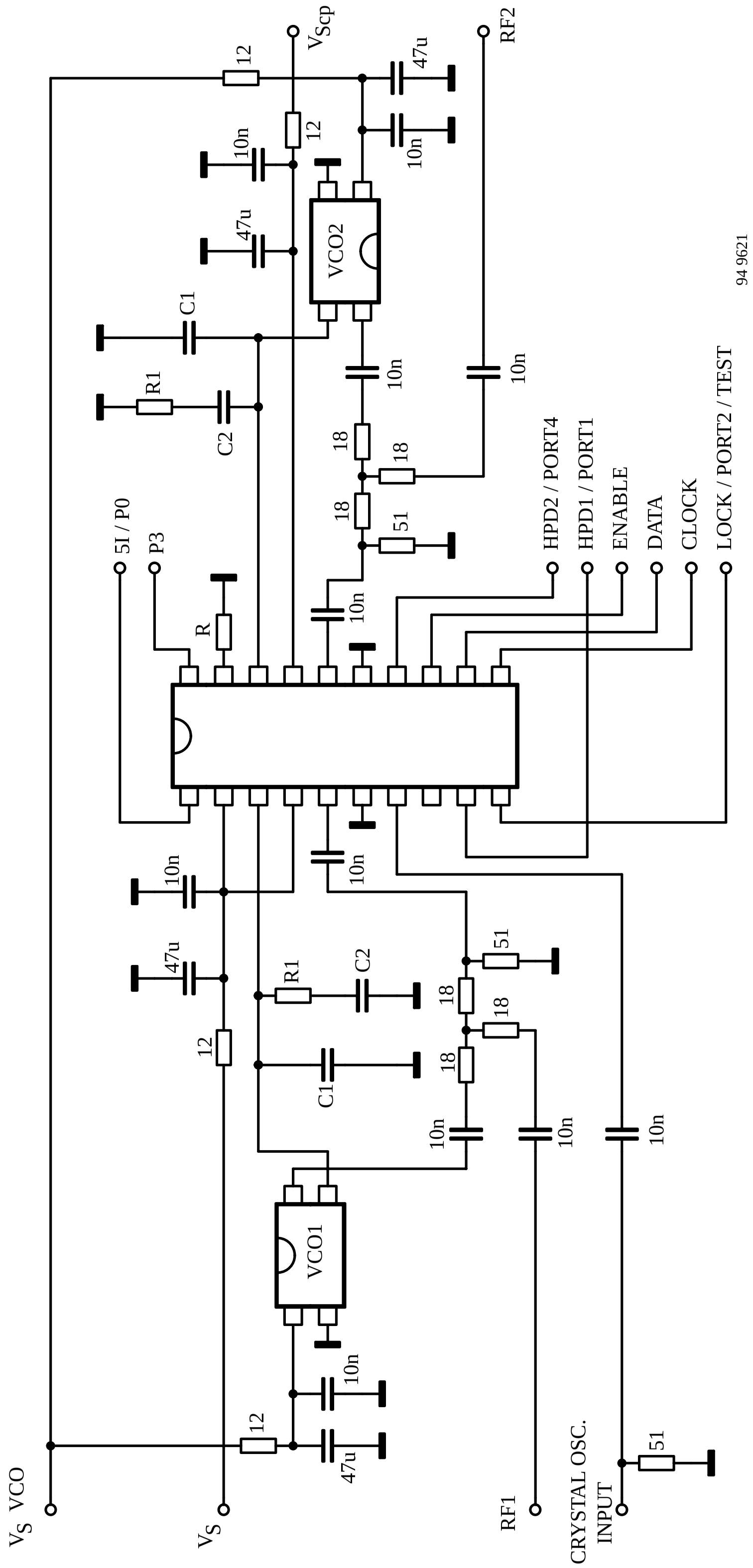


Figure 3. Application circuit

Timing Diagram Serial Bus

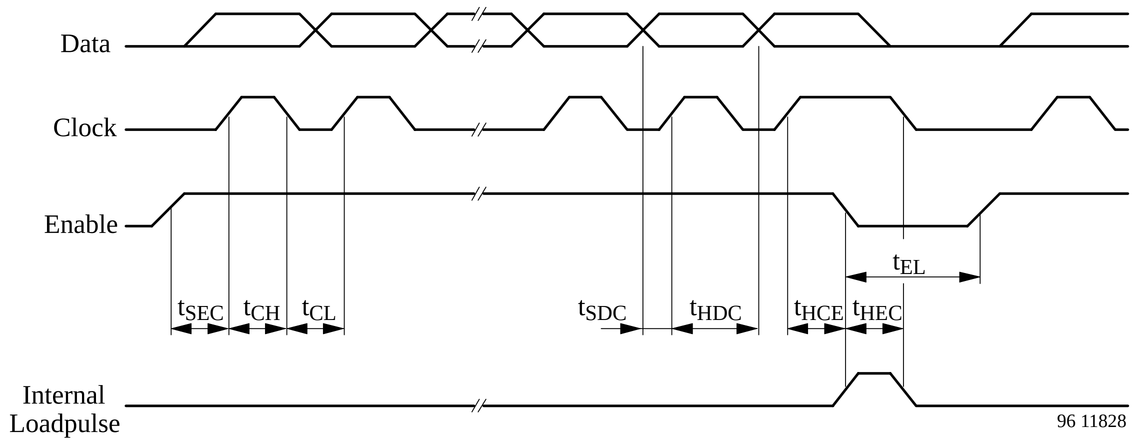


Figure 4.

Table 1. Timing

Parameters	Symbol	Value	Unit
Clock-High Time	t_{CH}	>750	ns
Clock-Low Time	t_{CL}	>350	ns
Clock Period	t_{PER}	>1100	ns
Set-up Time Clock Data to Clock	t_{SDC}	>100	ns
Hold Time Data to Clock	t_{HDC}	>400	ns
Hold Time Clock to Enable	t_{HCE}	>400	ns
Hold Time Enable to Clock	t_{HEC}	>400	ns
Enable Low Time	t_{EL}	>200	ns
Set-up Time Enable to Clock	t_{SEC}	>4000	ns

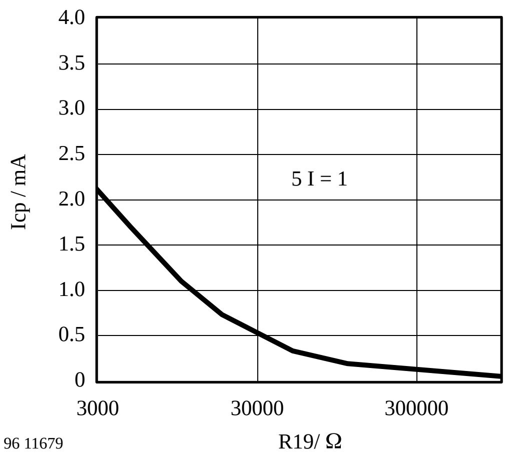


Figure 5. Charge-pump characteristics

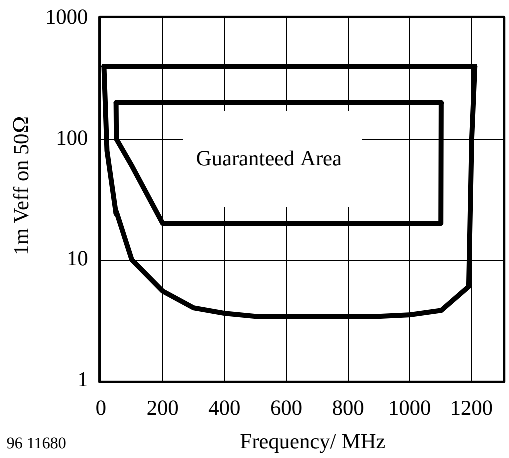


Figure 6. Input sensitivity of PLL1 and PLL2

Input Impedance of PLL1 and PLL2

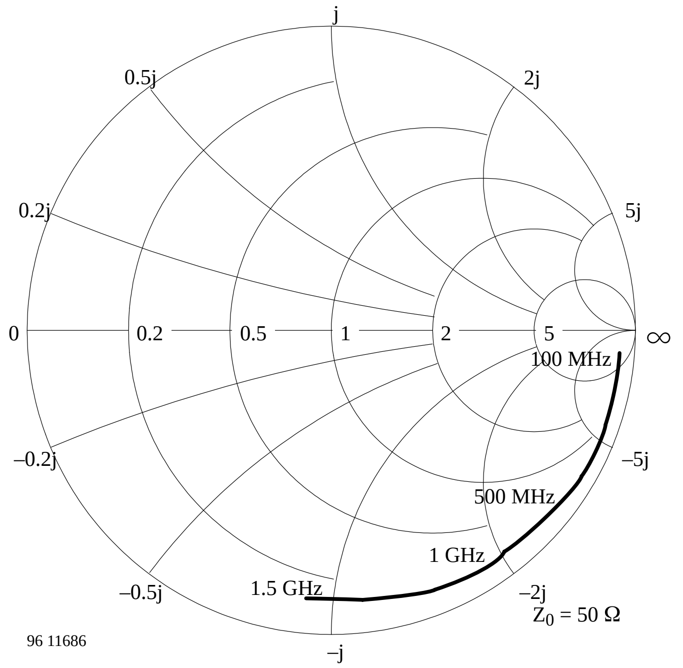
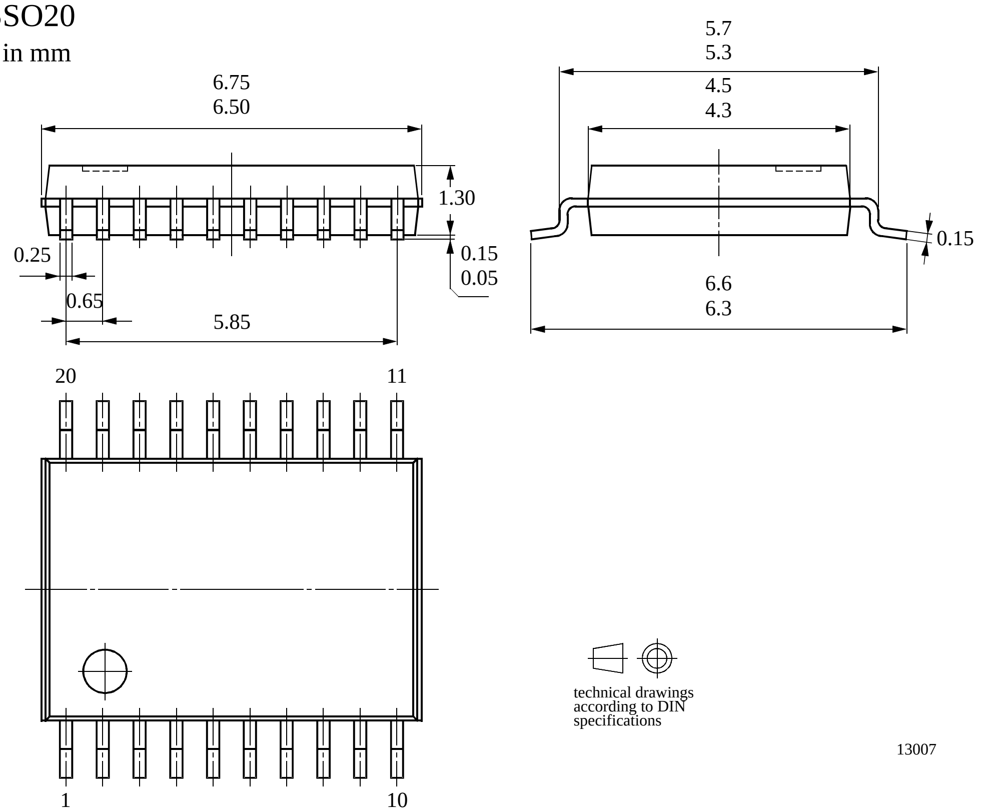


Figure 7.

Package Information

Package SSO20

Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

TEMIC Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2594, Fax number: 49 (0)7131 67 2423