

## Side-Airbag Sensor Dual Interface

### Description

The U6268B is an interface IC for remote automotive sensors. It links the crash sensors in the driver- and passenger door with the main airbag unit in the dashboard. Two identical channels supply the external sensors and receive digital information from them via one active wire each. The interface supplies the external sensors with a pre-regulated smoothed voltage, the external units transmit the digital information back to the

interface by current modulation.

As the device is for safety critical applications, highest data transmission security is mandatory. With high immunity against cross-coupling between the two channels, the U6268B is tailored for the harsh automotive environment.

### Features

- Two identical interface channels
- Provides a pre-regulated smoothed voltage and a supply current up to 50 mA for the sensors
- Receives data from the sensors by current modulation with a transmission rate of 60 kBaud (transmission bandwidth 500 kHz)
- Current modulation provides high noise immunity for data transfer
- TTL-compatible input activate the sensor
- Data output can be directly connected to a micro-controller input
- Operation supply voltage range  $5.7\text{ V} \leq V_S \leq 40\text{ V}$
- ESD protection according to MIL-STD-883C test method 3015.7
- High-level EMI protection

### Benefits

- Voltage supply and data transmission with one active wire over long distances

### Block Diagram

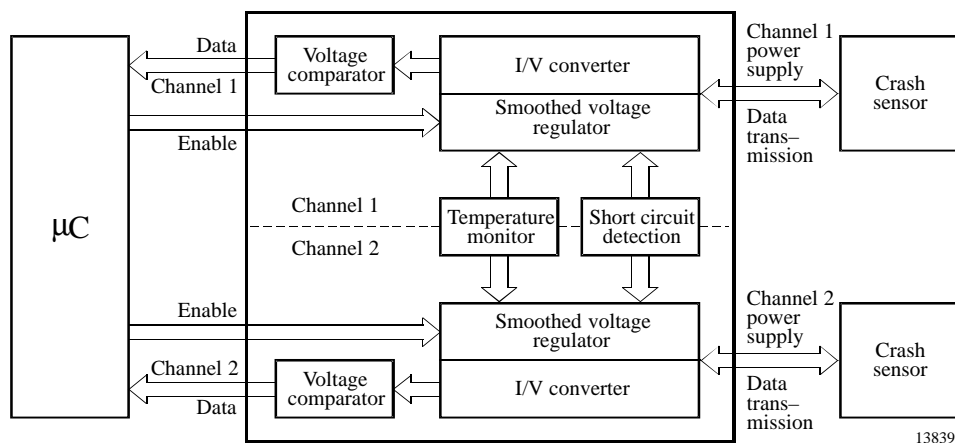


Figure 1. Block diagram

### Ordering Information

Extended Type Number	Package	Remarks
U6268B-FP	SO16	

## Pin Description

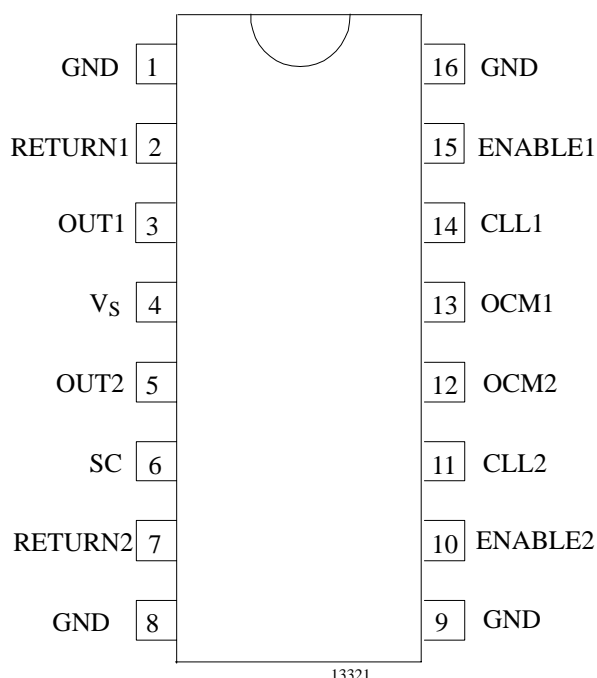


Figure 2. Pinning

Pin	Symbol	Function
1	GND	Ground and reference pin
2	RETURN1	Return line of the external unit, internally connected to GND via a line-protection transistor
3	OUT1	Voltage-stabilized supply output and current-modulation input
4	V <sub>S</sub>	Supply voltage of the IC
5	OUT2	Voltage stabilized supply output and current modulation input
6	SC	Smooth time constant for slow voltage change at both OUT pins
7	RETURN2	Return line of the external unit, internally connected to GND via a line-protection transistor
8, 9	GND	Ground and reference pin
10	ENABLE2	Controls OUT1 voltage, ENABLE1 High means OUT1 active, ENABLE1 Low or open means OUT1 switched off
11	CLL2	Current logic level output, low at high OUT2 current, monitoring via OCM2
12	OCM2	Analog current output, representing 1/10 current of OUT2
13	OCM1	Analog current output, representing 1/10 current of OUT1
14	CLL1	Current logic level output, low at high OUT1 current, monitoring via OCM1
15	ENABLE1	Controls OUT2 voltage, ENABLE2 High means OUT2 active, ENABLE1 Low or open means OUT2 switched off
16	GND	Ground and reference pin

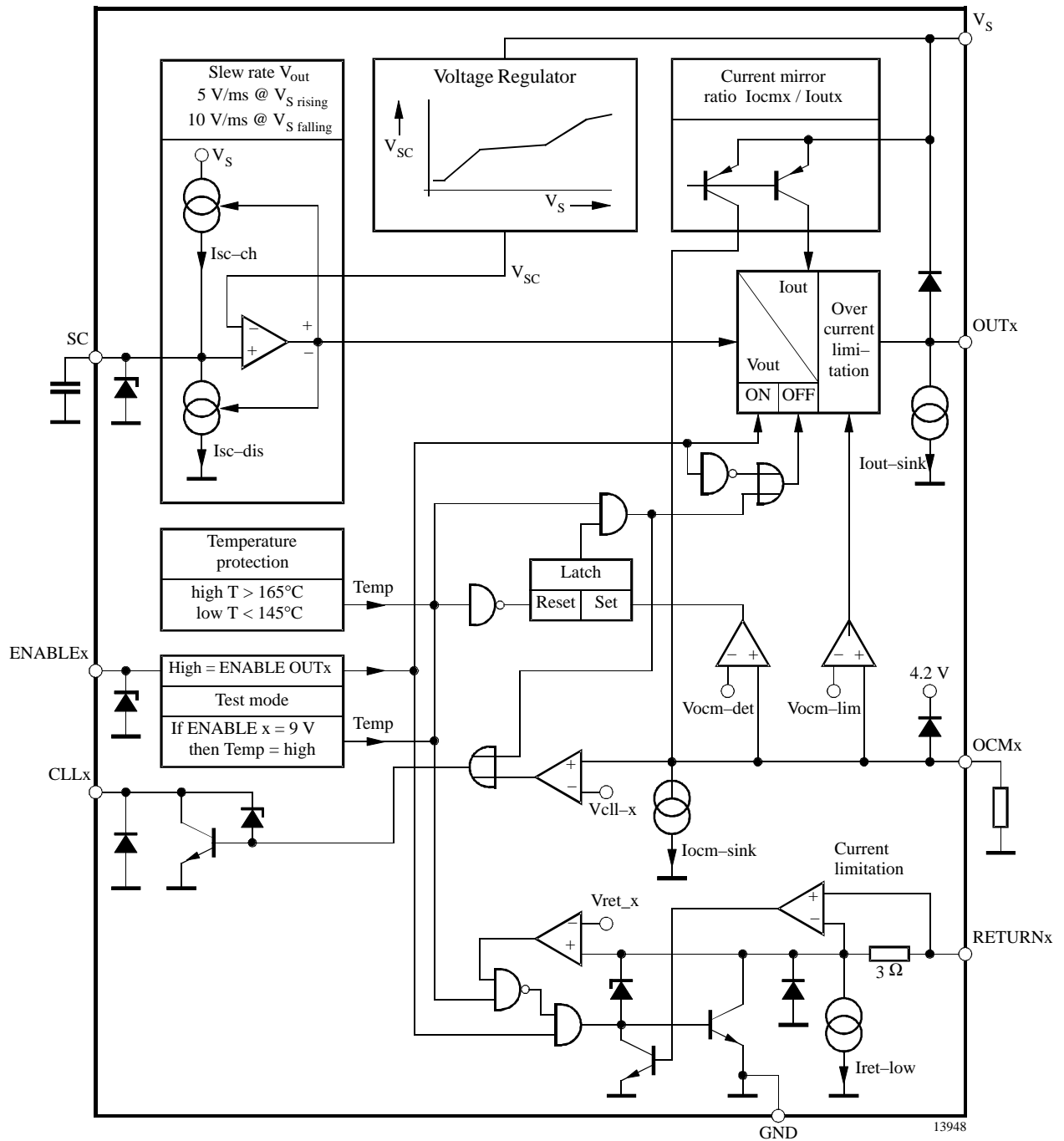


Figure 3. Functional block diagram

## Functional Description

### $V_S$

The IC and the external units are powered via the  $V_S$  Pin 4. This pin is connected to the battery via a reverse battery protection diode. An electrolytic capacitor of 22  $\mu$ F smoothes the voltage and absorbs positive and negative transients.

### OUT1, OUT2

OUTx provides a smoothed, very slowly changing supply

voltage for the external units and monitors the output current. During normal operating conditions, the OUTx voltage is typ. 3 V below  $V_S$ , and changes very slowly with a varying battery voltage in order to suppress disturbances in the data transmission. At low  $V_S$  (5.7 to 8.5 V), the OUTx voltage is typ. 0.5 V below  $V_S$ . This voltage difference is reduced in order to ensure sufficient supply voltage for the external unit between OUTx and RETURNx. The output current capability is 50 mA. The internal pull-down current at OUTx is typically 3 mA.

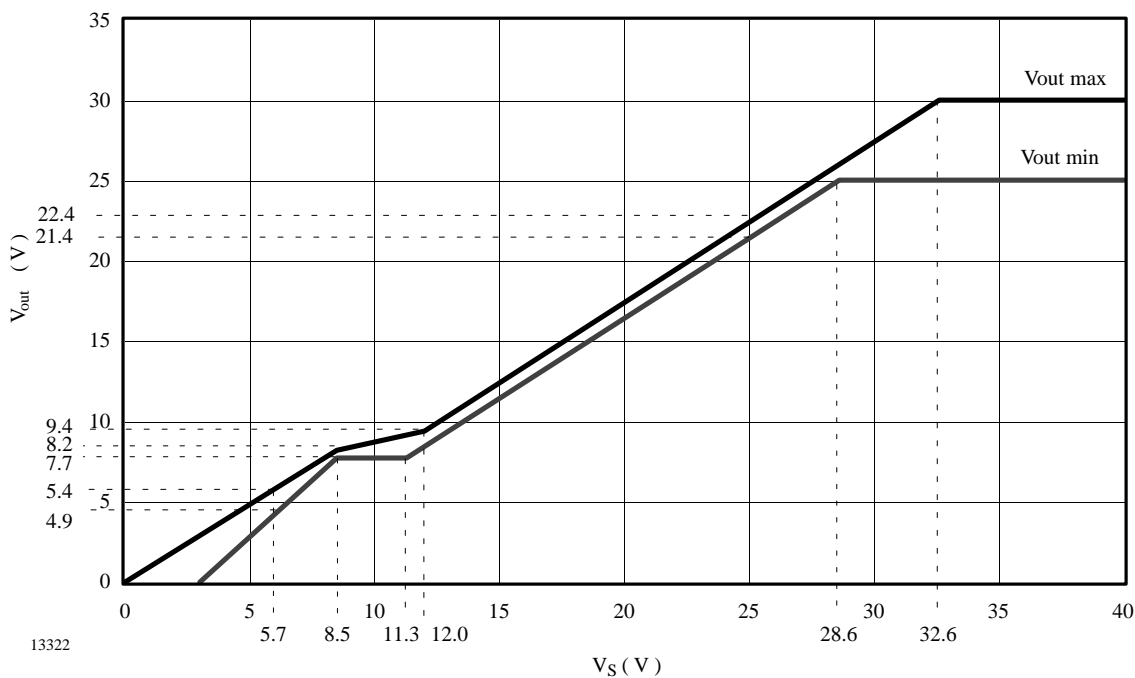


Figure 4. Output voltage with tolerances vs. supply voltage

The data transmission from the external unit to the interface IC is carried out on the same line by varying the current level. The quiescent current consumption of the external unit is about 5 to 15 mA. This current level is interpreted as logic high level at CLL-pin. The external unit can switch on an additional current of 30 mA, interpreted by the interface as logic low. The current changes within approximately 1  $\mu$ s, sufficient for a transmission rate of about 60 kBaud, requiring a transmission bandwidth of about 500 kHz for the current-monitoring subcircuit and the OCM output. For a good current transmission behaviour, the dynamic resistance of

OUTx may not exceed 12  $\Omega$  inside the bandwidth range (total of 15  $\Omega$  for OUTx and RETURN).

The OUTx- voltage can be switched off by  $ENABLEx = LOW$  to reset the external unit and to reduce power dissipation during fault conditions.

The OUT pins are overtemperature- and short-circuit protected. A reverse polarity diode at Pin  $V_S$  (Pin 4) ensures that no current is fed back to the  $V_{Batt}$ -system in the case of a short between OUTx and  $V_{Batt}$ . A minimum capacity of 33 nF is required at the pins OUTx.

## ENABLE1, ENABLE2

ENABLE<sub>x</sub> is a microcontroller-compatible input which switches the related output on or off.

- Low or open circuit applied to ENABLE<sub>x</sub> switches off the related OUT<sub>x</sub> and RETURN<sub>x</sub> (high impedance). A sink current at Pin OUT<sub>x</sub> discharges the capacitive load.
- High applied to ENABLE<sub>x</sub> switches on the related OUT<sub>x</sub> and RETURN<sub>x</sub> to supply the external unit.

## OCM1, OCM2

The output current of OUT<sub>x</sub> is monitored with a transmission factor of 0.1 to the OCM<sub>x</sub>. With a resistor from OCM to GND, the current is converted to a voltage. The electrical characteristics are specified by  $R_{OCM} = 750 \Omega$ . The CLL-current threshold, the OUT-current limitation and the OUT-current detection can be changed by varying  $R_{OCM}$  in a range from  $500 \Omega$  to  $1 \text{ k}\Omega$ .

The current monitoring enables to detect overcurrent conditions at OUT<sub>x</sub> (short circuit to GND or RETURN<sub>x</sub>) and to detect low current conditions at OUT<sub>x</sub> (short circuit to  $V_{Batt}$  or open load).

The internal pull-down current at the OUT<sub>x</sub> creates no OCM<sub>x</sub>-current. During enable, the minimum voltage at OCM<sub>x</sub> is the saturation voltage of an internal NPN-transistor with typically 0.1 V. The maximum voltage at OCM is limited by an internal clamping diode to 5.3 V.

## CLL1, CLL2

The current at Pin OUT<sub>x</sub> is evaluated logically and ready to use for a microcontroller input. With this stage, the logic data transmission from the external unit to the interface is completed.

CLL<sub>x</sub> is the output stage of a comparator with an internal threshold and with the OCM<sub>x</sub> input. A OCM<sub>x</sub>-voltage higher than 2.4 V creates a logic low at CLL<sub>x</sub>, and a OCM<sub>x</sub>-voltage lower than 1.43 V creates a logic high at CLL<sub>x</sub>. The comparator has an internal hysteresis with typically 0.4 V.

With the pull-down resistor  $R_{OCMx} = 750 \Omega$  at OCM<sub>x</sub>, the correct OUT<sub>x</sub>-current threshold related to the logical output CLL<sub>x</sub> is ensured. The CLL<sub>x</sub> is 'low' if the OUT<sub>x</sub>-current is higher than 27.3 mA, and the CLL<sub>x</sub> is 'high', if the OUT<sub>x</sub>-current is lower than 19.1 mA. The comparator has an internal hysteresis of typically 5 mA. The tolerance of the  $R_{OCM}$  resistor is assumed to be 0%.

The CLL-pin is an open-collector output and needs a pull-up resistor of typically  $2 \text{ k}\Omega$  to the 5-V supply. For ESD protection, a 7-V Zener diode is implemented.

## RETURN 1, RETURN 2

The RETURN<sub>x</sub> pin provides a low-ohmic connection to GND via a switched open-collector NPN-transistor. If ENABLE<sub>x</sub> is high, RETURN<sub>x</sub> is switched on with a saturation voltage less than 0.5 V at  $I_{RETURNx} \leq 50 \text{ mA}$ . If ENABLE<sub>x</sub> is low or open, RETURN<sub>x</sub> is a current sink with  $\leq 2 \text{ mA}$ . RETURN<sub>x</sub> is current-limited at typically 150 mA.

## SC

The smooth capacitor is designed to realize the long-time constant for the slow voltage change at OUT<sub>x</sub> for both interface channels. The capacity is typ. 22 nF. At the rising edge of  $V_{Batt}$ , the maximum slew rate is  $V_{OUTx} = 5 \text{ V/ms}$ , and at the falling edge of  $V_{Batt}$ , the maximum slew rate is  $V_{OUTx} = 10 \text{ V/ms}$ .

## GND-Pins

By means of a GND bond from the chip to Pin 1 and Pin 8, high ground breakage security is achieved and lowest voltage drop and ground shift between IC- and circuit ground is provided. The four GND pins and the die pad are directly connected to the copper leadframe, resulting in a very low thermal resistance,  $R_{thJC}$ . In order to achieve a good thermal resistance,  $R_{thJA}$ , a good copper connection from the four GND pins to the metal parts of the modul housing is also recommended.

## Power Dissipation

Worst case calculation of the supply current  $I_S$ :

$$I_S = 1,278 \times (I_{OUT1} + I_{OUT2}) + 18 \text{ mA}$$

Worst case calculation of the IC's power dissipation  $P_V$ :

$$P_V = (V_S \times I_S) - [(V_S - V_{diff} - V_{ret-sat}) \times (I_{OUT1} + I_{OUT2}) + R_{OCM} \times ((I_{OUT1}^2 + I_{OUT2}^2) / 81)]$$

$V_S$  = 5.7 to 25 V supply voltage

$V_{diff}$  =  $V_S$  to  $V_{OUTx}$  voltage difference

$V_{diff}$  = 3.6 V at  $12 \text{ V} \leq V_S \leq 25 \text{ V}$

$V_{diff}$  = 0.8 V at  $5.7 \text{ V} \leq V_S \leq 8.5 \text{ V}$

$V_{ret-sat}$  = 0.5 V saturation voltage return

$I_{OUTx}$  = output current at Pin OUT<sub>x</sub> = 0 to 60 mA

$R_{OCM}$  = resistor at Pin OCM<sub>x</sub>

An overtemperature protection is integrated which generates a switch-off signal at a chip temperature of typically  $T_j = 160^\circ\text{C}$  and a switch-on signal at typically  $T_j = 150^\circ\text{C}$ .

In case of a detected overtemperature, only the corresponding channel is disabled. The other channel stays enabled.

The RETURN<sub>x</sub> is switched off if the voltage at RETURN<sub>x</sub> is higher than 2 V (short-circuit comparator threshold) and overtemperature is detected.

The OUT<sub>x</sub> is switched off if the voltage at OCM<sub>x</sub> is higher than 4.6 V (overcurrent detection level) and overtemperature is detected. The OCM voltage monitors the output current at OUT<sub>x</sub> via the current ratio of 0.1. The overcurrent-detection level of OUT<sub>x</sub> can be varied by

changing the OCM<sub>x</sub> resistor. If OUT<sub>x</sub> is switched off by overtemperature and overcurrent detection, the CLL<sub>x</sub> output remains logic low (overcurrent).

As the IC is only overtemperature-protected for short-circuit conditions at RETURN<sub>x</sub> or OUT<sub>x</sub>, it has to be checked in each application that the chip temperature does not exceed  $T_{jmax} = 150^{\circ}\text{C}$  in normal operation.

## Test Hint

The overtemperature signal can be activated by connecting ENABLE1 or ENABLE2 to 9 V/ 10 mA.

## Absolute Maximum Ratings

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	$V_S$	-0.6		40	V
Voltage at pins CLL1, CLL2, ENABLE1, ENABLE2		-0.3		6	V
Voltage at SC	$V_{SC}$	-0.3		30	V
Voltage at OCM1, OCM2	$V_{OCMx}$	-0.3		6.8	V
Voltage at RETURN1, RETURN2	$V_{RETURNx}$	-1		27	V
Voltage at OUT1, OUT2	$V_{OUTx}$	-1		40	V
Current at supply (both channels OUT <sub>x</sub> and RETURN <sub>x</sub> shorted)	$I_S$			240	mA
Current at logical pins: CLL1, CLL2 ENABLE1, ENABLE2	$I_{CCLx}$ $I_{ENABLEx}$			3 0.1	mA mA
Current at SC (SC related to GND or $V_{Batt}$ )	$I_{SC}$	-110		220	μA
Current at pins to external unit OUT1, OUT2, RETURN1, RETURN2		internal limited			
ESD classification Human body model (100 pF, 1.5 kΩ) Machine model (200 pF, 0.0 Ω)	All pins	± 2000 ± 200			V V
Ambient temperature range	$T_{amb}$	-40		95	°C
Junction temperature range	$T_j$	-40		150	°C
Storage temperature range	$T_{stg}$	-55		125	°C

## Thermal Resistance

Parameters	Symbol	Value	Unit
Junction case	$R_{thJC}$	36	K/W

### Note:

A good thermal resistance junction ambient ( $R_{thJA} = 65 \text{ K/W}$ ) can be achieved by using a big pad size for ground connection nearby a metal component (see description of GND-pins).

## Electrical Characteristics

$T_{amb} = -40$  to  $95^{\circ}\text{C}$  and  $T_j = -40$  to  $150^{\circ}\text{C}$ ,

Operation supply-voltage range  $V_S = 5.7$  to  $18$  V continuously,  $V_S \leq 25$  V for max. 25 min,  $V_S \leq 40$  V for up to 500 ms.

The current values are based on  $R = 750\ \Omega$ , 0%-resistor at OCM1/OCM2 pins.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
<b>Supply current</b> $T_j \geq 125^{\circ}\text{C}$	Outputs disabled, $V_S \leq 18$ V	$I_S$			8	mA
	Outputs disabled, $V_S \leq 40$ V	$I_S$			14	mA
	One output enabled, $V_S \leq 18$ V	$I_S$			13	mA
	Both outputs enabled, $V_S \leq 18$ V	$I_S$			18	mA
	Output load $2 \times 15$ mA, $V_S \leq 18$ V	$I_S$			56	mA
	Output load $2 \times 28$ mA, $V_S \leq 18$ V	$I_S$			90	mA
	Output load $2 \times 50$ mA, $V_S \leq 18$ V	$I_S$			146	mA
	Output load $2 \times 60$ mA, $V_S \leq 18$ V ( $T_j > 125^{\circ}\text{C}$ )	$I_S$			171	mA
	Both channels OUTx and RETURNx shorted, $V_S \leq 18$ V	$I_S$			200	mA
<b>Function SC</b>						
Voltage at SC	$V_S = 5.7$ V	$V_{SC}$	5.1		5.3	V
Voltage at SC	$V_S = 12.5$ V	$V_{SC}$	9		9.4	V
Maximal voltage at SC	$V_S = 40$ V	$V_{SCmax}$			30	V
SC-discharge current	Voltage SC = $V_{SC} - 3$ V $5.7\text{ V} \leq V_S \leq 40\text{ V}$	$I_{SC\_dis}$	33		82	$\mu\text{A}$
SC-charge current	Voltage SC = $V_{SC} - 3$ V $5.7\text{ V} \leq V_S \leq 40\text{ V}$	$I_{SC\_ch}$	-58		-20	$\mu\text{A}$
<b>Function OUT1 and OUT2</b> (see figure 4)						
Voltage difference, $V_S$ to $V_{OUTx}$	$I_{OUTx} = 5$ to $50$ mA $5.7\text{ V} \leq V_S \leq 8.5\text{ V}$ $12\text{ V} \leq V_S \leq 25\text{ V}$	$V_{diff\_low}$	0.3		0.8	V
		$V_{diff\_high}$	2.6		3.6	V
Output voltage OUTx	$8.5\text{ V} \leq V_S \leq 11.3\text{ V}$	$V_{OUT\_med}$	7.7			V
Maximal voltage at OUTx	$V_S = 40$ V	$V_{OUT\_max}$	25		30	V
Current mirror ratio, $I_{OCMx}/I_{OUTx}$	$V_S \leq 40$ V, $I_{OUTx} = 5$ to $15$ mA $V_S \leq 25$ V, $I_{OUTx} = 15$ to $50$ mA $V_S \leq 40$ V, $I_{OUTx} = 15$ to $50$ mA	$I_{OUT\_ratio}$	0.09		0.12	
			0.10		0.11	
			0.097		0.11	
Linearity of mirror ratio $I_{OCMx}/I_{OUTx}$		Ratio_lin	-5		5	%
Dynamic resistance OUTx	$V_S \leq 40$ V $I_{OUT} = 15$ to $50$ mA	$R_{OUT}$	2		12	$\Omega$
Dynamic resistance OUTx + RETURNx	$V_S \leq 40$ V $I_{OUT} = 15$ to $50$ mA	$R_{Dyn}$	4		15	$\Omega$

## Electrical Characteristics (continued)

$T_{amb} = -40$  to  $95^{\circ}\text{C}$  and  $T_j = -40$  to  $150^{\circ}\text{C}$ ,

Operation supply-voltage range  $V_S = 5.7$  to  $18\text{ V}$  continuously,  $V_S \leq 25\text{ V}$  for max. 25 min,  $V_S \leq 40\text{ V}$  for up to 500 ms.

The current values are based on  $R = 750\ \Omega$ , 0%-resistor at OCM1/OCM2 pins.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
OUTx current limitation (OUTx short to GND)	$V_S \leq 18\text{ V}$ $V_S \leq 40\text{ V}$	$I_{OUT\_lim}$	-80 -105		-60 -60	mA mA
Overcurrent detection level general	$T_j < 125^{\circ}\text{C}$	$I_{OUT\_det}$	-70		-51	mA
Overcurrent detection level	$T_j \geq 125^{\circ}\text{C}$ Always valid: current limitation is higher than overcurrent detection	$I_{OUT\_det}$	-60		-51	mA
Maximum OUTx current (OUTx short to GND)	$V_S = 14\text{ V}$ , OCMx shorted to GND	$I_{OUT\_max}$	-140		-85	mA
Leakage current at disabled OUTx	OUTx short to GND, $V_S \leq 25\text{ V}$ OUTx short to GND, $V_S \leq 38.5\text{ V}$	$I_{OUT\_leak}$	-0.02 -12			mA mA
Leakage voltage at disabled OUTx	OUTx open, $V_S \leq 38.5\text{ V}$	$V_{OUT\_leak}$			4.3	V
Internal pull-down current	$V_S \leq 18\text{ V}$ $V_S \leq 40\text{ V}$	$I_{OUT\_sink}$	1.8 2.5		4 4.5	mA mA
Supply rejection-ratio	$V_{SC} = 7.6\text{ V}$	$V_{rej\_mV}$			80	mV
Supply rejection-ratio	Variation of $V_S = 8.4\text{ V}$ to $40\text{ V}$ in $10\ \mu\text{s}$	$V_{rej\_dB}$	51.9			dB
Minimum capacity at OUTx for phase margin		$C_{OUT\_min}$	33			nF
Delay time with $C_{out} = 47\text{ nF}$	Switching on ENABLE = 1 to 90% $V_{OUT}$ reached	Enable_on	3		30	$\mu\text{s}$
	Switching off ENABLE = 0 to 10% $V_{OUT}$ reached	Enable_off	30		100	$\mu\text{s}$
<b>Function OCM1, OCM2</b>						
Voltage threshold CLL-comparator	CLLx low-level voltage threshold	$V_{CLL\_L}$	1.75		2.4	V
	CLLx high-level voltage threshold	$V_{CLL\_H}$	1.43		1.9	V
	Voltage hysteresis	$V_{CLL\_hys}$	0.26		0.6	V
Minimum voltage at OCMx	$I_{OUT} = 0$ to $5\text{ mA}$	$V_{OCM\_min}$			0.5	V
Current-limitation level	$V_S \leq 40\text{ V}$ , OUTx short to GND	$V_{OCM\_lim}$	4.3		5.3	V
Overcurrent-detection level	$V_S \leq 40\text{ V}$	$V_{OCM\_det}$	4.2		4.9	V
Current limitation minus overcurrent detection	$V_{OCM\_lim} - V_{OCM\_over}$	$\Delta_{lim\_OCM}$	0.15		0.5	V
Intern. pull-down current		$I_{OCM\_sink}$	0.1		0.45	mA
<b>Function RETURN1, RETURN2</b>						
Enable high saturation voltage	$I_{RETURN} = 50\text{ mA}$	$V_{ret\_sat}$			0.5	V



## Electrical Characteristics (continued)

$T_{amb} = -40$  to  $95^{\circ}\text{C}$  and  $T_j = -40$  to  $150^{\circ}\text{C}$ ,

Operation supply-voltage range  $V_S = 5.7$  to  $18$  V continuously,  $V_S \leq 25$  V for max. 25 min,  $V_S \leq 40$  V for up to 500 ms.

The current values are based on  $R = 750\ \Omega$ , 0%-resistor at OCM1/OCM2 pins.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Dynamic resistance	$dI \geq 10\text{ mA}$	$R_{ret}$	2		8	$\Omega$
Current limitation RETURNx is always higher than current limitation OUTx	Enable high, $V_{RETURNx} = 2\text{ V}$	$I_{ret\_lim}$	60		150	mA
	Enable high, $V_{RETURNx} \leq 18\text{ V}$	$I_{ret\_lim}$	70		200	mA
	Enable low $V_{RETURNx} \leq 18\text{ V}$	$I_{ret\_low}$	0.8		2	mA
Overcurrent-detection level	Threshold comparator, switch-off return	$V_{ret\_low}$	1.4		2	V
	Threshold comparator, switch-on return	$V_{ret\_high}$	1.1		1.5	V
	Hysteresis	$V_{ret\_hys}$	0.2		0.7	V
Delay time $C_{RETURN} = 47\text{ nF}$	Switching on $I_{RETURN}$ at 50 mA	$t_{dRet\_on}$	3		30	$\mu\text{s}$
	Switching off $I_{RETURN}$ at 1 mA	$t_{dRet\_off}$	30		90	$\mu\text{s}$
<b>Function CLL1, CLL2 (CLLx with 2 k<math>\Omega</math> to 5 V)</b>						
$I_{OUT}$ threshold CLL comparator	$R_{OCM} = 750\ \Omega$					
	CLL low-level threshold	$I_{CLL\_L}$	23.3		27.3	mA
	CLL high-level threshold	$I_{CLL\_H}$	19.1		22.3	mA
	Hysteresis	$I_{CLL\_hys}$	3.5		8.2	mA
CLL saturation voltage	$I_{CLL} \leq 2.5\text{ mA}$	$V_{CLL\_sat}$			0.4	V
CLL leakage current	$V_{CLL} \leq 6.5\text{ V}$	$I_{CLL\_leak}$			1	$\mu\text{A}$
Response time to current change	$I_{OUT}$ to CLL rise	$t_{Cil\_rise}$	0.1		2	$\mu\text{s}$
	$I_{OUT}$ to CLL fall	$t_{Cil\_fall}$	0.1		2	$\mu\text{s}$
	Max. difference between rise and fall time	$t_{\Delta\text{-rise-fall}}$			1	$\mu\text{s}$
CLL output switching speed	Rise	$t_{CLL\_rise}$			1	$\mu\text{s}$
	Fall	$t_{CLL\_fall}$			1	$\mu\text{s}$
Current transmission rate			60			kHz
Current transmission 3 dB bandwidth			500			kHz
<b>Function ENABLE1, ENABLE2</b>						
Enable high-level threshold		$V_{Enable\_on}$	2		6.5	V
Enable low-level threshold		$V_{Enable\_off}$	-0.3		0.8	V
Enable input pull-down current (to ensure output disabled during power-off and reset of micro- controller)		$I_{Enable}$	10		100	$\mu\text{A}$

## Electrical Characteristics (continued)

$T_{amb} = -40$  to  $95^{\circ}\text{C}$  and  $T_j = -40$  to  $150^{\circ}\text{C}$ ,

Operation supply-voltage range  $V_S = 5.7$  to  $18\text{ V}$  continuously,  $V_S \leq 25\text{ V}$  for max. 25 min,  $V_S \leq 40\text{ V}$  for up to 500 ms.

The current values are based on  $R = 750\ \Omega$ , 0%-resistor at OCM1/OCM2 pins.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
<b>Power dissipation</b>						
Power dissipation 1 $T_j \geq 125^{\circ}\text{C}$	$V_S = 18\text{ V}$ , $I_{OUT1} = 28\text{ mA}$ , $I_{OUT2}$ at overcurrent detection level or $I_{OUT2} = 28\text{ mA}$ , $I_{OUT1}$ at overcurrent detection level	$P_{dis1}$			1	W
Power dissipation 2 $T_j \geq 125^{\circ}\text{C}$	$V_S = 18\text{ V}$ , $I_{OUT1} = I_{OUT2} = 28\text{ mA}$	$P_{dis2}$			0.75	W
<b>Selective overtemperature protection</b>						
Logic AND connected with overcurrent detec- tion (RETURNx, OUTx)	Switch off	Temp_off	155		165	$^{\circ}\text{C}$
	Switch on	Temp_on	145		155	$^{\circ}\text{C}$
	Hysteresis	Temp_hys	5		20	$^{\circ}\text{C}$
Time delay until over- temperature shut-down	$V_S = 25\text{ V}$ , $T_{amb} = 125^{\circ}\text{C}$ $OUT1 = OUT2 = \text{GND}$	$t_{del}$	100			ms

## Timing Diagrams

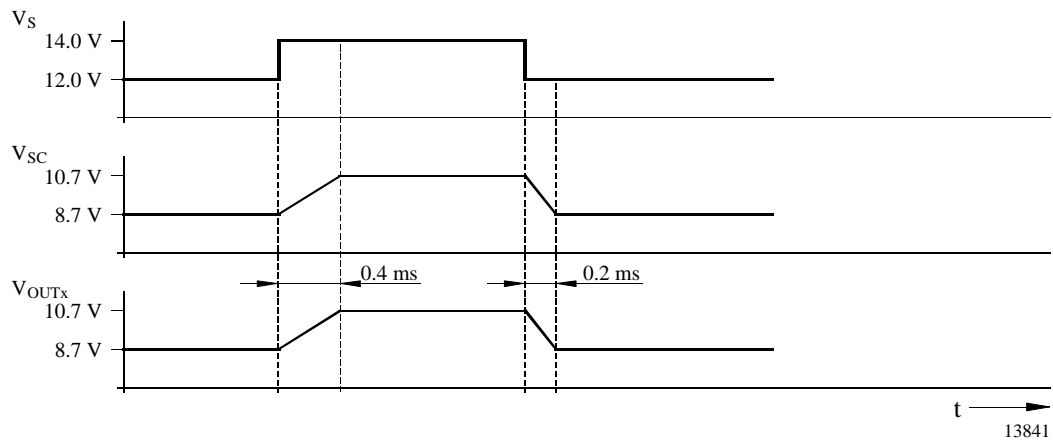


Figure 5. Variation of power supply

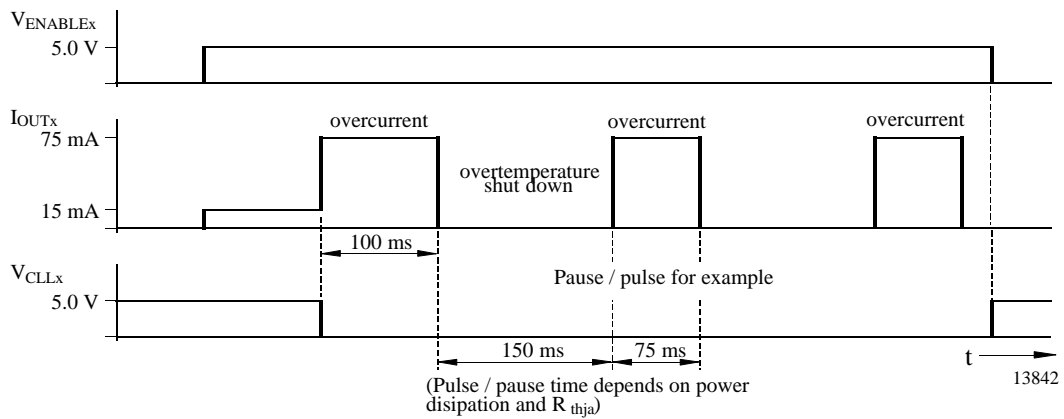


Figure 6. Overcurrent protection

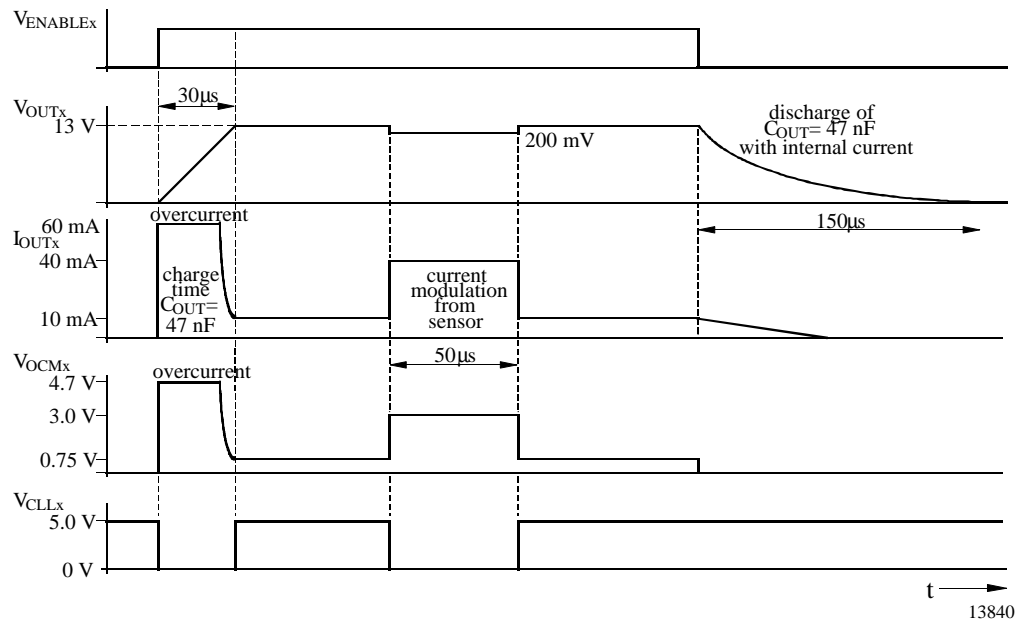
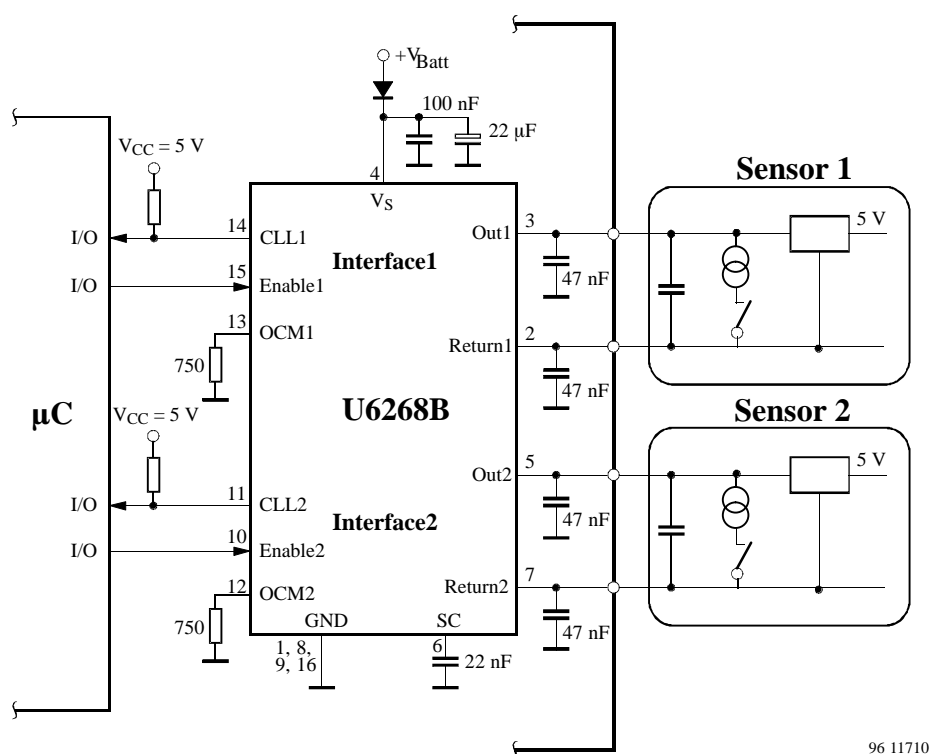


Figure 7. Data transmission

## Application Circuit



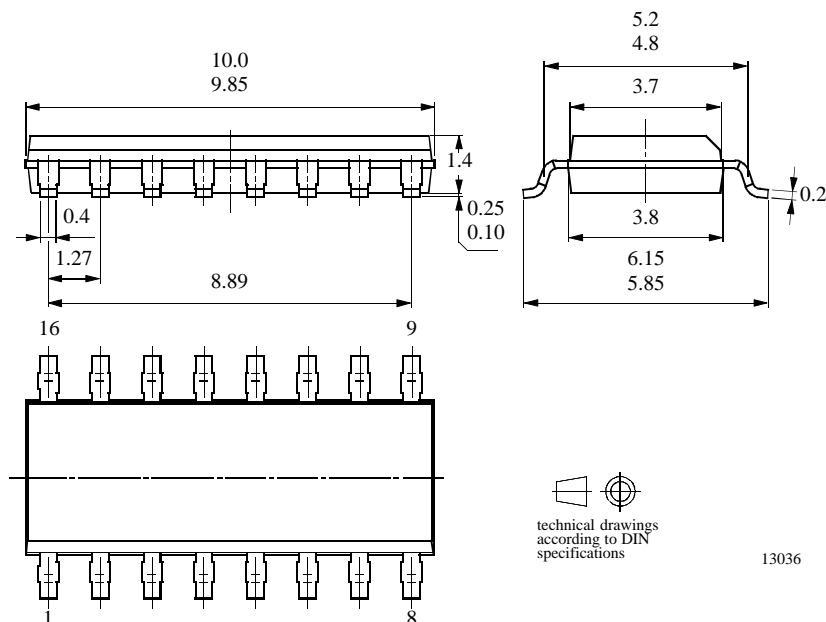
96 11710

Figure 8. Application circuit

## Package Information

Package SO16

Dimensions in mm



13036

## **Ozone Depleting Substances Policy Statement**

It is the policy of **Atmel Germany GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

**Atmel Germany GmbH** has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

**Atmel Germany GmbH** can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

**We reserve the right to make changes to improve technical design and may do so without further notice.**

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use Atmel Wireless & Microcontrollers products for any unintended or unauthorized application, the buyer shall indemnify Atmel Wireless & Microcontrollers against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

**Data sheets can also be retrieved from the Internet:    <http://www.atmel-wm.com>**

Atmel Germany GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany  
Telephone: 49 (0)7131 67 2594, Fax number: 49 (0)7131 67 2423