

Special Fail-Safe IC

Description

The U6808B is designed to support the fail-safe function of a safety critical system e.g. ABS. It includes a relay driver, a watchdog controlled by an external R/C-network

and a reset circuit initiated by an over- and undervoltage condition of the 5-V supply providing a positive and a negative reset signal.

Features

- Digital self-supervising watchdog with hysteresis
- One 250-mA output driver for relay
- Enable output open collector 10 mA
- Over-/undervoltage detection
- ENABLE- and RELAY outputs protected against standard transients and 40 V load dump
- ESD protection according to MIL-STD-883 D test method 3015.7
 - Human body model: ± 2 kV (100 pF, 1.5 k Ω)
 - Machine model: ± 200 V (200 pF, 0 Ω)

Block Diagram

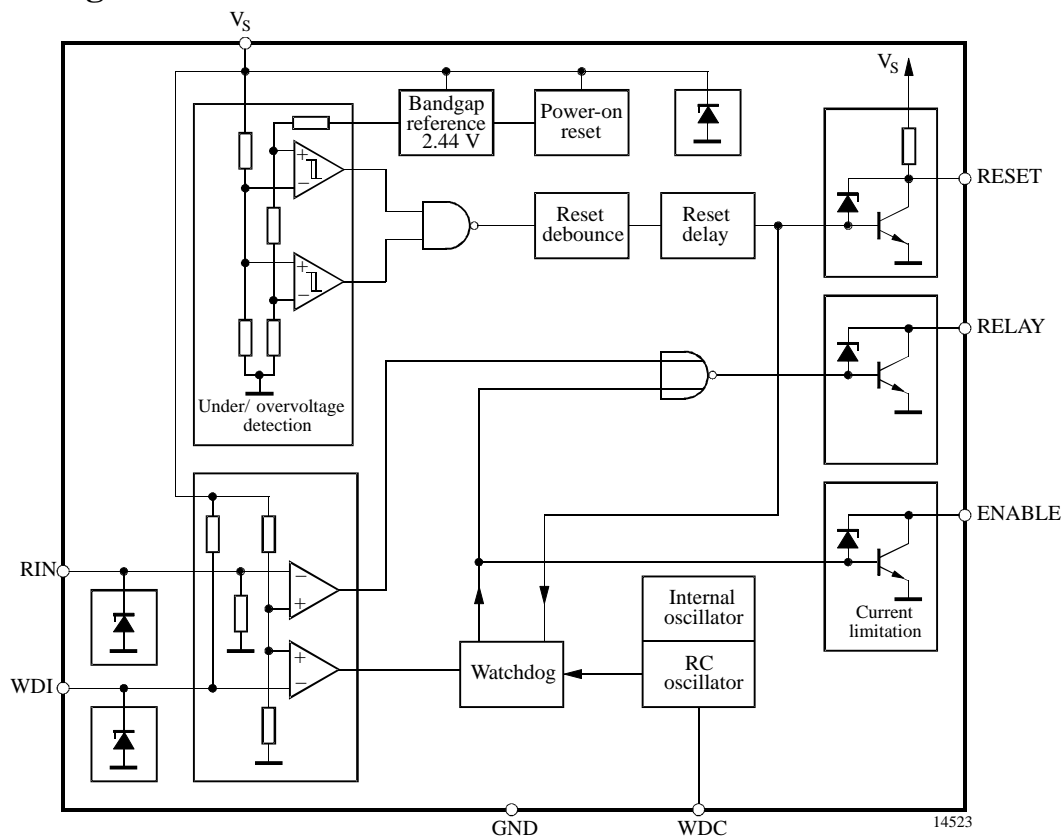
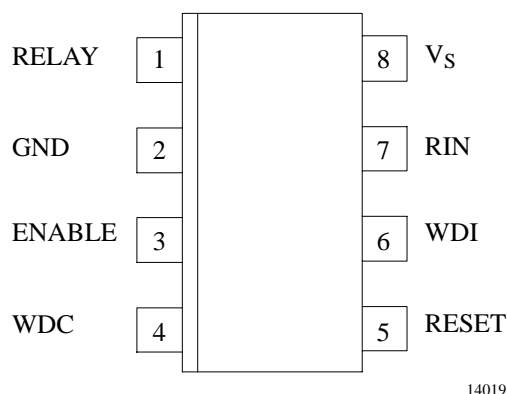


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U6808B	SO8	

Pin Description



14019

Figure 2. Pinning U6808B

Table 1 Pin description

Pin	Name	Type	Function	Logic
1	RELAY	Open collector driver output	Fail-safe relay driver	Driver off: — driver on: L
2	GND	Supply	Standard ground	
3	ENABLE	Digital output	Negative reset signal	Reset: L
4	WDC	Analog input	External RC for watchdog timer	
5	RESET	Digital output	Negative reset signal	Reset: L
6	WDI	Digital input	Watchdog trigger signal	Pulse sequence
7	RIN	Digital input	Activation of relay driver	H: driver on L: driver off
8	V _S	Supply	5-V supply	

Fail-Safe Functions

A fail-safe IC has to maintain its monitoring function even if there is a fault condition at one of the pins (e.g. short circuit). This ensures that a microcontroller system would not be brought into a critical status. A critical status

is reached if the system is not able to switch off the relay and to give a signal to the μ C via ENABLE- and RESET outputs. The following table shows the fault conditions for the pins.

Table 2 Table of fault conditions

Pin	Function	Short to V _S	Short to V _{Bat}	Short to GND	Open Circuit
RIN	Digital input to activate the fail-safe relay	Relay on	Relay on	Relay off	Relay off
WDI	Watchdog trigger input	Watchdog reset	Watchdog reset	Watchdog reset	Watchdog reset
OSC	Capacitor and resistor of watchdog	Watchdog reset	Watchdog reset	Watchdog reset	Watchdog reset
RELAY	Driver of the fail-safe relay			Relay on	Relay off

Truth Tables

Table 3 Truth table the over- and under voltage conditions

Inputs		Outputs		
Supply Voltage (Vs)	Relay Input (RIN)	Relay Output Driver (RELAY)	RESET Output (RESET)	Enable Output Driver (ENABLE)
Normal	Low	Off	High	Off
	High	On	High	Off
Too low	Low	Off	Low	On
	High	Off	Low	On
Too high	Low	Off	Low	On
	High	Off	Low	On

Table 4 Truth table for watchdog failures (RESET output don't care)

Inputs		Outputs	
Watchdog Input (WDI)	Relay Input (RIN)	Relay Output Driver (RELAY)	Enable Output Driver (ENABLE)
Normal	Low	Off	Off
	High	On	Off
Too slow	Low	Off	On
	High	Off	On
Too fast	Low	Off	On
	High	Off	On

Description of the Watchdog

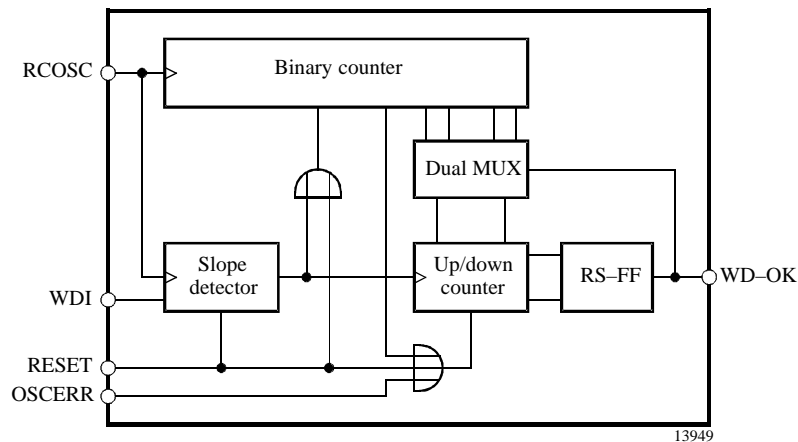


Figure 3. Watchdog block diagram

Abstract

The microcontroller is monitored by a digital window watchdog which accepts an incoming trigger signal of a constant frequency for correct operation. The frequency of the trigger signal can be varied in a broad range as the

watchdog's time window is determined by external R/C components. The following description refers to the block diagram (Fig. 3)

WDI Input (Pin 6)

The microcontroller has to provide a trigger signal with the frequency f_{WDI} which is fed to the WDI input. A positive edge of f_{WDI} detected by a slope detector resets the binary counter and clocks the up/down counter additionally. The latter one counts only from 0 to 3 or reverse. Each correct trigger increments the up/down counter by 1, each wrong trigger decrements it by 1. As soon as the counter reaches status 3 the RS flip-flop is set; see Fig. 4 (WD state diagram). A missing incoming trigger signal is detected after 250 clocks of the internal watchdog frequency f_{RC} (see WD OK output) and resets the up/down counter directly.

RCOSC Input

With an external R/C circuitry the IC generates a time base (frequency f_{WDC}) independent from the microcontroller. The watchdog's time window refers to a frequency of

$$f_{WDC} = 100 \times f_{WDI}$$

OSCERR Input

A smart watchdog has to ensure that internal problems with its own time base are detected and do not lead to an undesired status of the complete system. If the RC oscillator stops oscillating a signal is fed to the OSCERR input after a timeout delay. It resets the up/down counter and disables the WD-OK output.

Without this reset function the watchdog would freeze its current status when f_{RC} stops.

RESET Input

During power-on and under-/ overvoltage detection a reset signal is fed to this pin. It resets the watchdog timer and sets the initial state.

WD-OK Output

After the up/down counter is incremented to status 3 (see Fig. 4, WD state diagram) the RS flip-flop is set and the WD-OK output becomes logic "1". This information is available for the microcontroller at the open-collector output ENABLE. If on the other hand the up/down counter is decremented to 0 the RS flip-flop is reset, the WD-OK output and the ENABLE output are disabled. The WD-OK output also controls a dual MUX stage which shifts the time window by one clock after a successful trigger thus forming a hysteresis to provide stable conditions for the evaluation of the trigger signal 'good' or 'false'. The WD-OK signal is also reset in the case the watchdog counter is not reset after 250 clocks (missing trigger signal).

Watchdog State Diagram

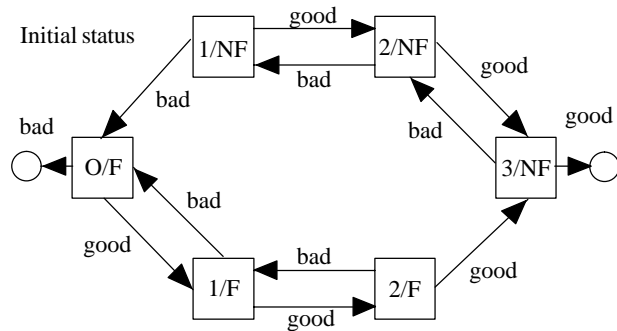


Figure 4. Watchdog state diagram

Explanation

In each block, the first character represents the state of the counter. The second notation indicates the fault status of the counter. A fault status is indicated by an "F" and a no fault status is indicated by an "NF". When the watchdog is powered up initially, the counter starts out at the O/F block (initial state). "Good" indicates that a pulse has been received whose width resides within the timing window. "Bad" indicates that a pulse has been received whose width is either too short or too long.

Watchdog-Window Calculation

Example with recommended values

$$C_{osc} = 3.3 \text{ nF} \quad (\text{should be preferably } 10\%, \text{ NPO})$$

$$R_{osc} = 39 \text{ k}\Omega \quad (\text{may be } 5\%, R_{osc} < 100 \text{ k}\Omega \text{ due to leakage current and humidity})$$

RC Oscillator

$$t_{WDC} \text{ (s)} = 10^{-3} \times [C_{osc} \text{ (nF)} \times [(0.00078 \times R_{osc} \text{ (k}\Omega)) + 0.0005]]$$

$$f_{WDC} \text{ (Hz)} = 1 / (t_{WDC})$$

Watchdog WDI

$$f_{WDI} \text{ (Hz)} = 0.01 \times f_{WDC}$$

$$t_{WDC} = 100 \text{ }\mu\text{s} \quad \rightarrow \quad f_{WDC} = 10 \text{ kHz}$$

$$f_{WDI} = 100 \text{ Hz} \quad \rightarrow \quad t_{WDI} = 10 \text{ ms}$$

WDI pulse width for fault detection after 3 pulses:

Upper watchdog window

Minimum: $169 / f_{WDC} = 16.9 \text{ ms} \rightarrow f_{WDC} / 169 = 59.1 \text{ Hz}$

Maximum: $170 / f_{WDC} = 17.0 \text{ ms} \rightarrow f_{WDC} / 170 = 58.8 \text{ Hz}$

Lower watchdog window

Minimum: $79 / f_{WDC} = 7.9 \text{ ms} \rightarrow f_{WDC} / 79 = 126.6 \text{ Hz}$

Maximum: $80 / f_{WDC} = 8.0 \text{ ms} \rightarrow f_{WDC} / 80 = 125.0 \text{ Hz}$

WDI dropouts for immediate fault detection:

Minimum: $250 / f_{WDC} = 25 \text{ ms}$

Maximum: $251 / f_{WDC} = 25.1 \text{ ms}$

Time/s	$79 / f_{WDC}$	$80 / f_{WDC}$	$169 / f_{WDC}$	$170 / f_{WDC}$	$250 / f_{WDC}$	$251 / f_{WDC}$
		Watchdog window update rate is good				
Update rate is too fast	Update rate is either too fast or good		Update rate is either too slow or good	Update rate is too slow	Update rate is either too slow or pulse has dropped out	Pulse has dropped out

Figure 5. Watchdog timing diagram with tolerances

Remark to Reset Delay

The duration of the over- or undervoltage pulses determines the enable- and reset output. A pulse duration shorter than the debounce time has no effect on the

outputs. A pulse longer than the debounce time results in the first reset delay. If a pulse appears during this delay, a 2nd delay time is triggered. Therefore, the total reset delay time can be longer than specified in the data sheet.

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply-voltage range	V_S	- 0.2 to 16	V
Power dissipation $V_S = 5 \text{ V}; T_{amb} = -40^\circ\text{C}$	P_{tot}	250	mW
$V_S = 5 \text{ V}; T_{amb} = 125^\circ\text{C}$	P_{tot}	150	mW
Thermal resistance	R_{thja}	160	K/W
Junction temperature	T_j	150	$^\circ\text{C}$
Ambient temperature range	T_{amb}	-40 to 125	$^\circ\text{C}$
Storage temperature range	T_{stg}	-55 to 155	$^\circ\text{C}$

Electrical Characteristics

$V_S = 5\text{ V}$, $T_{\text{amb}} = -40\text{ to } +125^\circ\text{C}$; reference pin is GND;
 $f_{\text{intern}} = 100\text{ kHz} + 50\% - 45\%$, $f_{\text{WDC}} = 10\text{ kHz} \pm 10\%$; $f_{\text{WDI}} = 100\text{ Hz}$

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage						
Operation range general		V_S	4.5		5.5	V
Operation range reset		V_S	1.2		16.0	V
Supply current						
Relay off	$T_{\text{amb}} = -40^\circ\text{C}$ $T_{\text{amb}} = 125^\circ\text{C}$				6	mA
Relay on	$T_{\text{amb}} = -40^\circ\text{C}$ $T_{\text{amb}} = 125^\circ\text{C}$				15	mA
Digital input WDI						
Detection low			-0.2		$0.2 \times V_S$	V
Detection high			$0.7 \times V_S$		$V_S + 0.5\text{ V}$	V
Resistance to V_S			10		40	k Ω
Input current low	Input voltage = 0 V		100		550	μA
Input current high	Input voltage = V_S		-5		5	μA
Zener clamping voltage		V_{ZWDI}	20		24	V
Digital input RIN						
Detection low			-0.2		$0.2 \times V_S$	V
Detection high			$0.7 \times V_S$		$V_S + 0.5\text{ V}$	V
Resistance to GND			10		40	k Ω
Input current low	Input voltage = 0 V		-5		+5	μA
Input current high	Input voltage = V_S		100		550	μA
Zener clamping voltage		V_{ZRIN}	20		24	V
Digital output RESET with internal pull-up						
Voltage high	Pull-up = 6 k Ω		$0.7 \times V_S + 0.1$		V_S	V
Voltage low	$I \leq 1\text{ mA}$ $1.2\text{ V} < V_S < 16\text{ V}$		0		0.3	V
Zener clamping voltage		$V_{\text{ZRESE T}}$	26		30	V
Reset debounce time	Switch to 'low'	t_{deb}	120	320	500	μs
Reset delay time	Switch back to 'high'	t_{del}		50		ms
Digital output ENABLE with open collector						
Saturation voltage low	$I \leq 10\text{ mA}$		0.01		0.5	V
Zener clamping voltage		V_{ZEN}	26		30	V

Electrical Characteristics (continued)

$V_S = 5\text{ V}$, $T_{\text{amb}} = -40\text{ to } +125^\circ\text{C}$; reference pin is GND;

$f_{\text{intern}} = 100\text{ kHz} + 50\% - 45\%$, $f_{\text{WDC}} = 10\text{ kHz} \pm 10\%$; $f_{\text{WDI}} = 100\text{ Hz}$

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Current limitation		I_{lim}	10			mA
Leakage current	$V_{\text{EN}} = 5\text{ V}$ $V_{\text{EN}} = 16\text{ V}$ $V_{\text{EN}} = 26\text{ V}$	$I_{\text{EN}5}$ $I_{\text{EN}16}$ $I_{\text{EN}26}$			20 100 200	μA μA μA
Reset debounce time	Switch to 'low'	t_{deb}	120	320	500	μs
Reset delay time	Switch back to 'high'	t_{del}		85		ms
Relay driver output RELAY						
Saturation voltage	$I \leq 250\text{ mA}$ $I \leq 130\text{ mA}$	V_{Rsat} V_{Rsat}			0.5 0.3	V V
Maximum load current	$T_{\text{amb}} -40\text{ to } 90^\circ\text{C}$ $T_{\text{amb}} > 90^\circ\text{C}$	I_{R} I_{R}	250 200			mA mA
Zener clamping voltage		V_{ZR}	26		30	V
Turn-off energy			30			mJ
Leakage current	$V_{\text{R}} = 16\text{ V}$ $V_{\text{R}} = 26\text{ V}$	$I_{\text{R}16}$ $I_{\text{R}26}$			20 200	μA μA
Reset and V_S control						
Lower reset level		V_S	4.5		4.7	V
Upper reset level		V_S	5.35		5.6	V
Hysteresis			25		100	mV
Reset debounce time			120	320	500	μs
Reset delay			20	50	80	ms
RC oscillator WDC						
Oscillator frequency	$R_{\text{OSC}} = 39\text{ k}\Omega$ $C_{\text{OSC}} = 3.3\text{ nF}$	f_{WDC}	9	10	11	kHz
Watchdog timing						
Power-on-reset prolongation time		t_{POR}	34 .3		103.1	ms
Detection time for RC-oscillator fault	$V_{\text{RC}} = \text{const.}$	t_{RCerror}	81.9		246	ms
Time interval for over-/under voltage detection		$t_{\text{D,OUV}}$	0.16		0.64	ms
Reaction time of RESET output over/ under voltage		$t_{\text{R,OUV}}$.187		0.72	ms
Nominal frequency for WDI	$f_{\text{RC}} = 100 \times f_{\text{WDI}}$	f_{WDI}	10		130	Hz
Nominal frequency for WDC	$f_{\text{WDI}} = 1/100 \times f_{\text{WDC}}$	f_{WDC}	1		13	kHz
Minimum pulse duration for a securely WDI input pulse detection		$t_{\text{p,WDI}}$	182			μs

Electrical Characteristics (continued)

$V_S = 5\text{ V}$, $T_{\text{amb}} = -40\text{ to } +125^\circ\text{C}$; reference pin is GND;
 $f_{\text{intern}} = 100\text{ kHz} + 50\% - 45\%$, $f_{\text{WDC}} = 10\text{ kHz} \pm 10\%$; $f_{\text{WDI}} = 100\text{ Hz}$

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Frequency range for a correct WDI signal		f_{WDI}	64.7		112.5	Hz
Number of incorrect WDI trigger counts for locking the outputs		n_{lock}		3		
Number of correct WDI trigger counts for releasing the outputs		n_{release}		3		
Detection time for a stucked WDI signal	$V_{\text{WDI}} = \text{const.}$	t_{WDIerror}	24.5		25.5	ms
Watchdog timing relative to f_{WDC}						
Minimum pulse duration for a securely WDI input pulse detection				2		cycles
Frequency range for a correct WDI signal			80		169	cycles
Hysteresis range at the WDI ok margins				1		cycle
Detection time for a dropped out WDI signal	$V_{\text{WDI}} = \text{const.}$		250		251	cycles

Protection against transient voltages according to ISO TR 7637–3 level 4 (except pulse 5)

Pulse	Voltage	Source Resistance *	Rise Time	Duration	Amount
1	– 110 V	10	100 V/s	2 ms	15.000
2	+ 110 V	10	100 V/s	0.05 ms	15.000
3a	– 160 V	50	30 V/ns	0.1 s	1 h
3b	+ 150 V	50	20 V/ns	0.1 s	1 h
5	40 V	2	10 V/ms	250 ms	20

* Relay driver: relay coil with $R_{\text{min}} = 70\ \Omega$ to be added to the source resistance.

Timing Diagrams

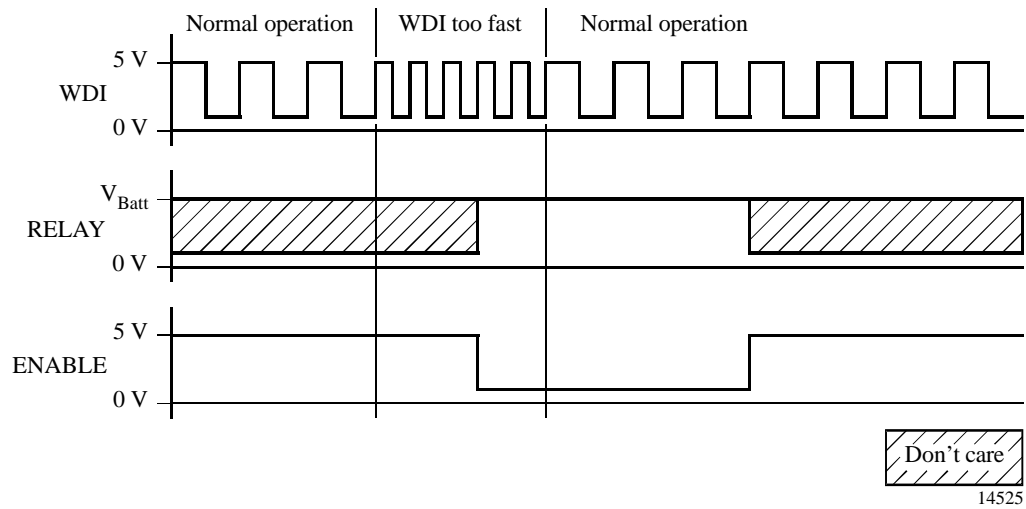


Figure 6. Watchdog in too-fast condition

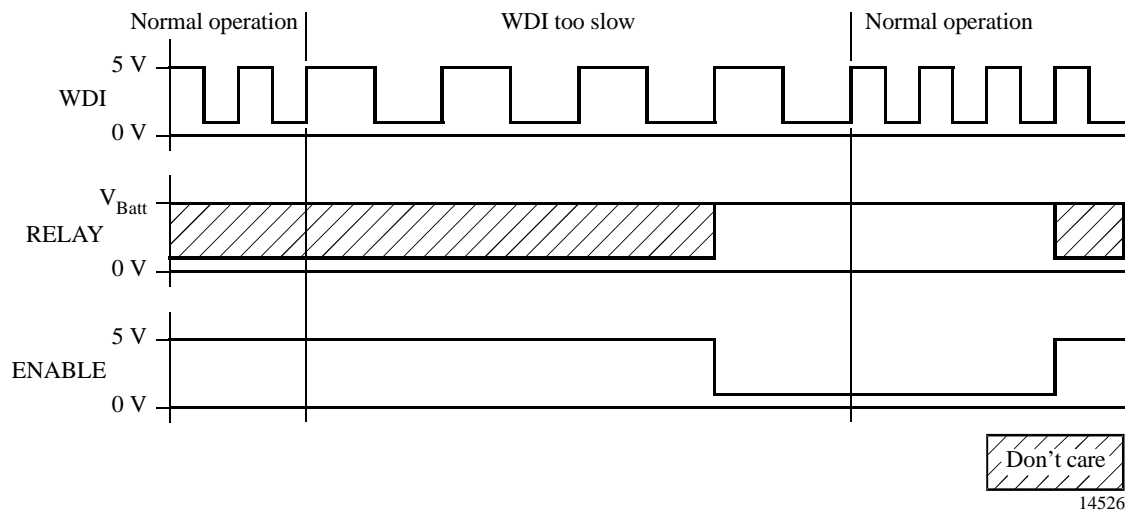


Figure 7. Watchdog in too-slow condition

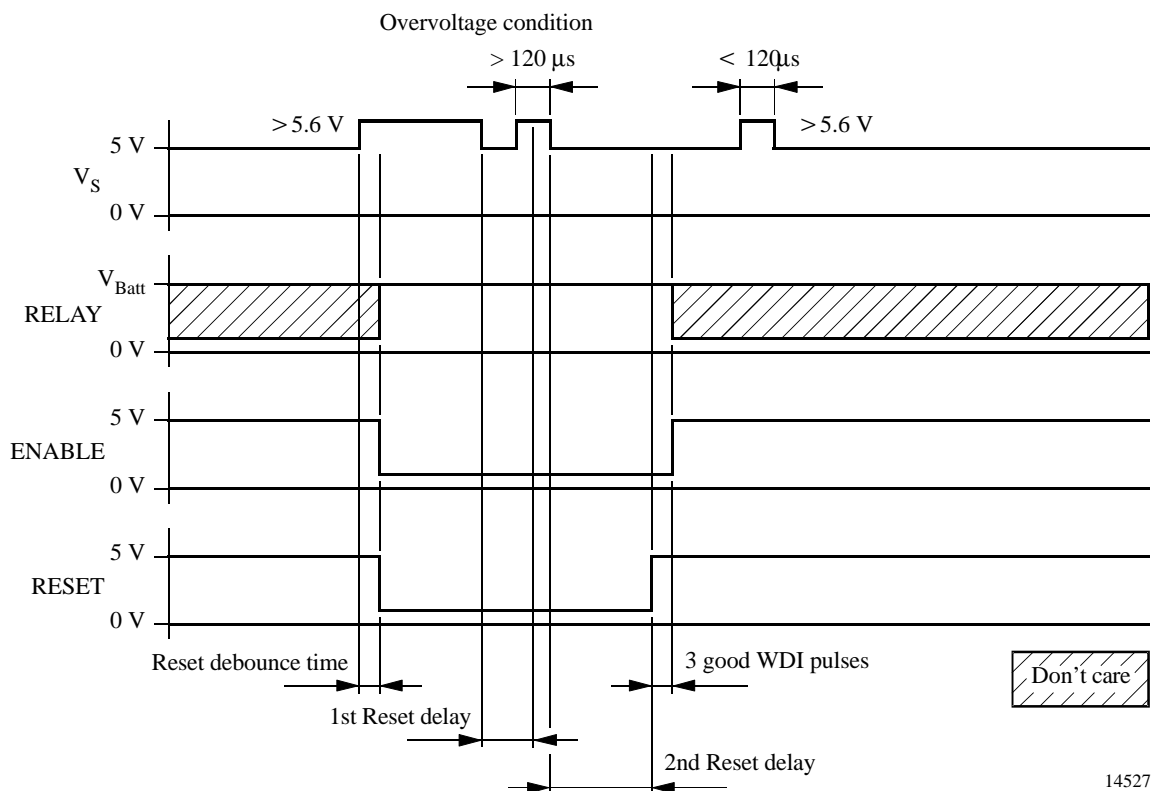


Figure 8. Overvoltage condition

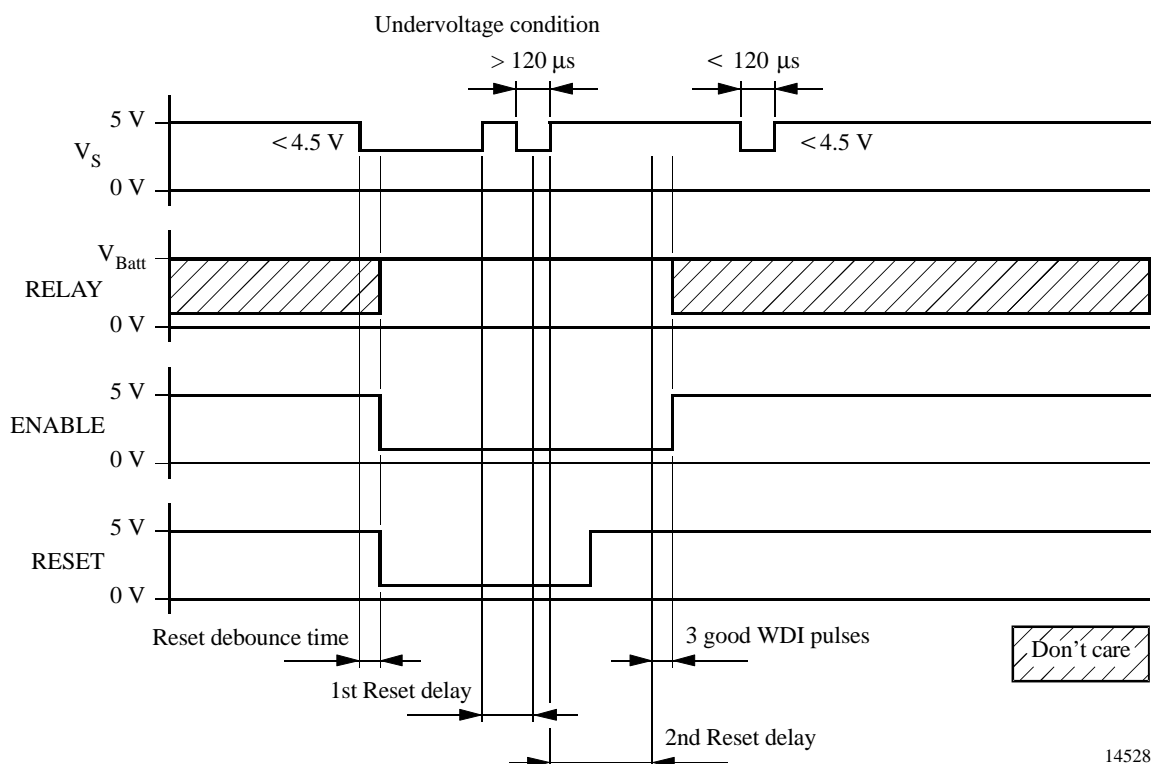


Figure 9. Undervoltage condition

Application Circuit

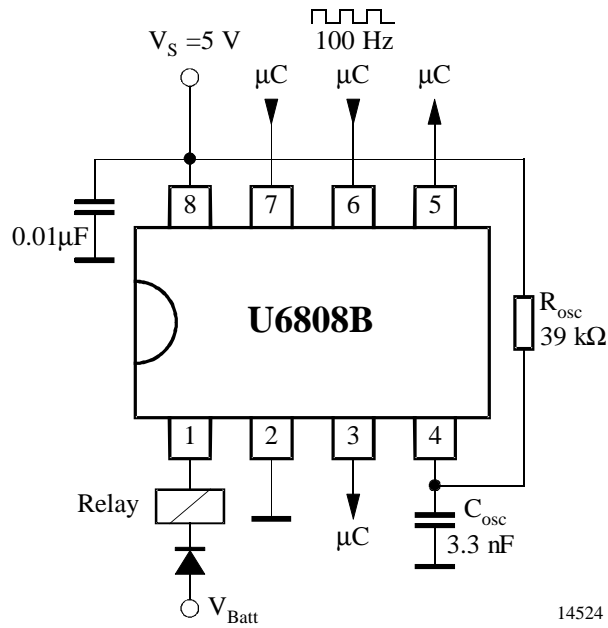
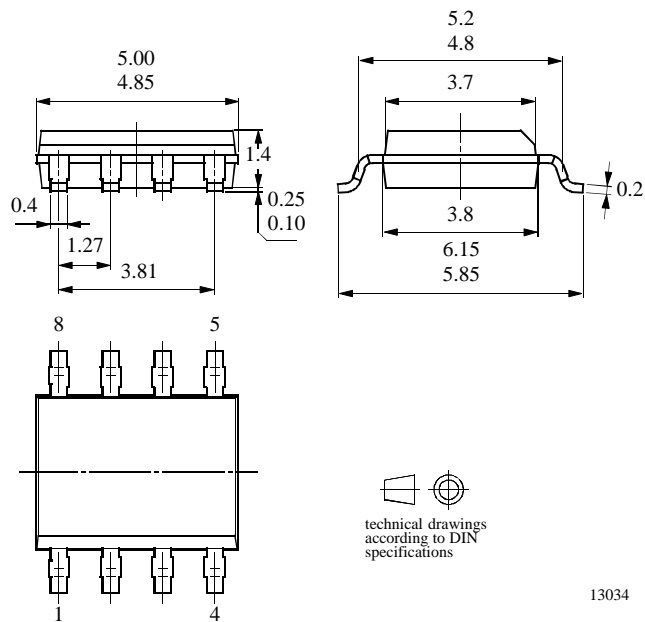


Figure 10. Application circuit

Package Information

Package SO8

Dimensions in mm



Ozone Depleting Substances Policy Statement

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1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Atmel Germany GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Atmel Germany GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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Data sheets can also be retrieved from the Internet: <http://www.atmel-wm.com>

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