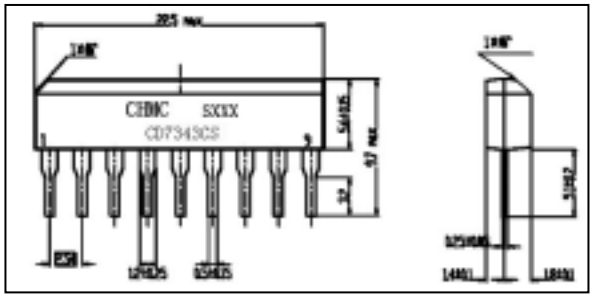
FM STEREO MULTIPLEX DECODER CD7343CS

GENERAL DESCRIPTION

The CD7343CS is a monolithic integrated circuit consisting of a phase locked loop FM stereo demodulator. It is designed for car stereo, cassette recorder and other equipment.

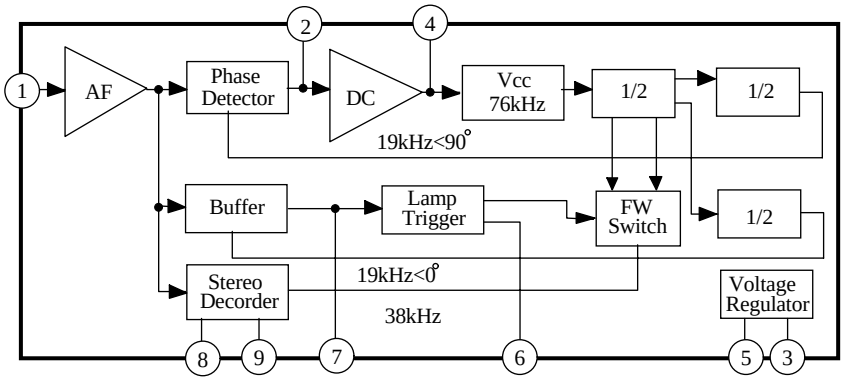
Outline Drawing



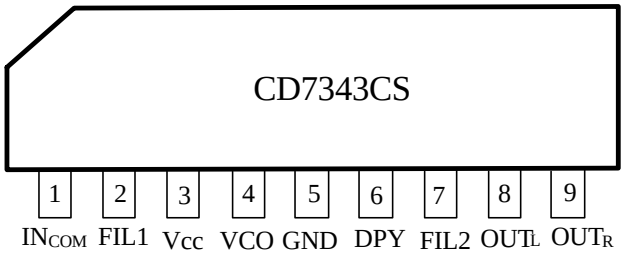
FEATURES

- Wide operating supply voltage: Vcc=3.5V~12V
- High pilot lamp ON sensitivity ($V_{L(ON)}$=9mV)
- Built-in indicator lamp drive circuit
- Low distortion THD=0.08% at Vi=200mV

BLOCK DIAGRAM



PIN CONNECTION



MAXIMUM RATINGS

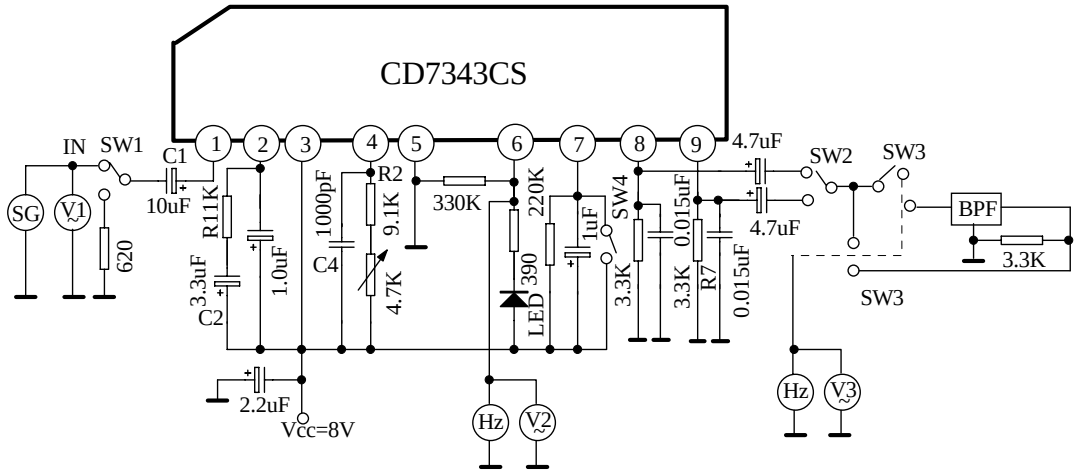
Characteristics	Symbol	Value	Unit
Supply Voltage	Vcc	12	V
Lamp Voltage	VLAMP	16	V
Lamp Current (Continuous)	ILAMP	20	mA
Power Dissipation	P_D	500	mW
Operating Ambient Temperature Range	Topr	-25~75	°C
Storage Temperature Range	Tstg	-55~150	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified Vcc=8V,Tamb=25°C,f=1kHz)

Characteristic	Symbol	Test Condition		Min.	Typ.	Max.	Unit
Quiescent Circuit Current	ICCQ	Vi=0			11	18	mA
Maximum Input Voltage	Vi(max)	L+R=90%, P=10%,THD=1%			900		mV
Channel Separation	Sep	L+R=180mV,Vp=20mV		36	45		dB
Total Harmonic Distortion (mono)	THD1	Vi=200mV			0.08	0.3	%
Total Harmonic Distortion (stereo)	THD2	L+R=180mV,Vp=20mV			0.08		%
Voltage Gain	Av	Vi=200mV		-2.0	0	2.0	dB
Channel Balance	CB	Vi=200mV			0	1.5	dB
Lamp ON level	$V_{L(ON)}$	Pilot only			9	15	mV
Lamp OFF level	$V_{L(OFF)}$	Pilot only		2	6		mV
Lamp Hysteresis	V_{HY}				3		mV
Carrier Leakage	CL	L+R=180mV Vp=20mV	19kHz		34		dB
			38kHz		42		dB

TEST CIRCUIT



BPF: 19kHz≦55dB 38kHz≦55dB L.P.F

APPLICATION INFORMATION (refer to test circuit)

External Components

1. Input coupling capacitor (C1)

The recommended value is 10μF. If smaller values than 10μF are used, low frequency separation will worsens, and if large values are used ,POP noise occurs strongly.

2. Low Pass Filter (C2, C1, R1)

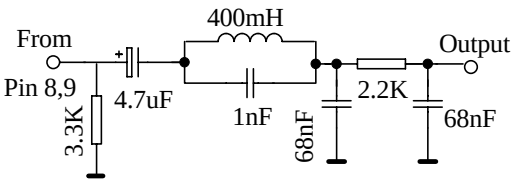
This is the low Pass filter for the PLL, which is determined the capture range and THD at low frequency.

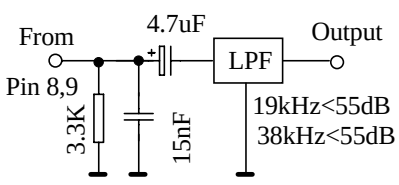
3. VCO network (C4, R2, R7)

The VCO free running frequency is adjusted by connecting a frequency counter to monitor the 38kHz output of Pin6 .

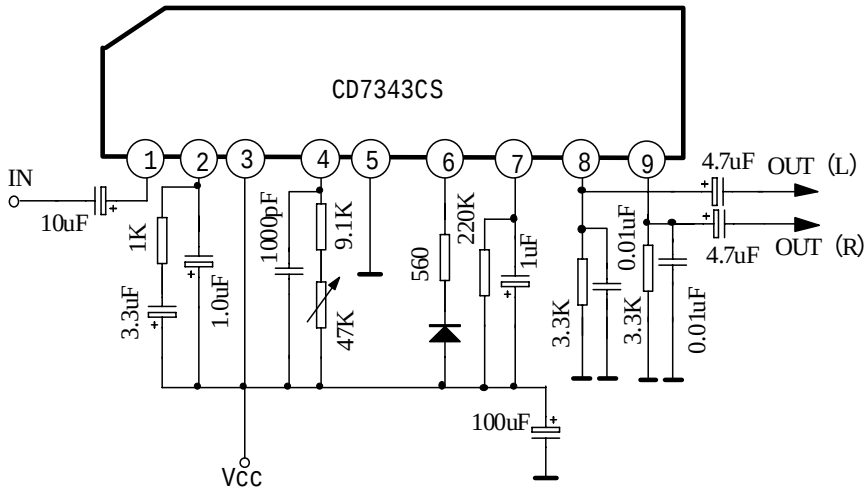
4. Decoder Output (Pin8,9)

These components provide Right and Left channel Output load circuits . The recommended circuits as follows:

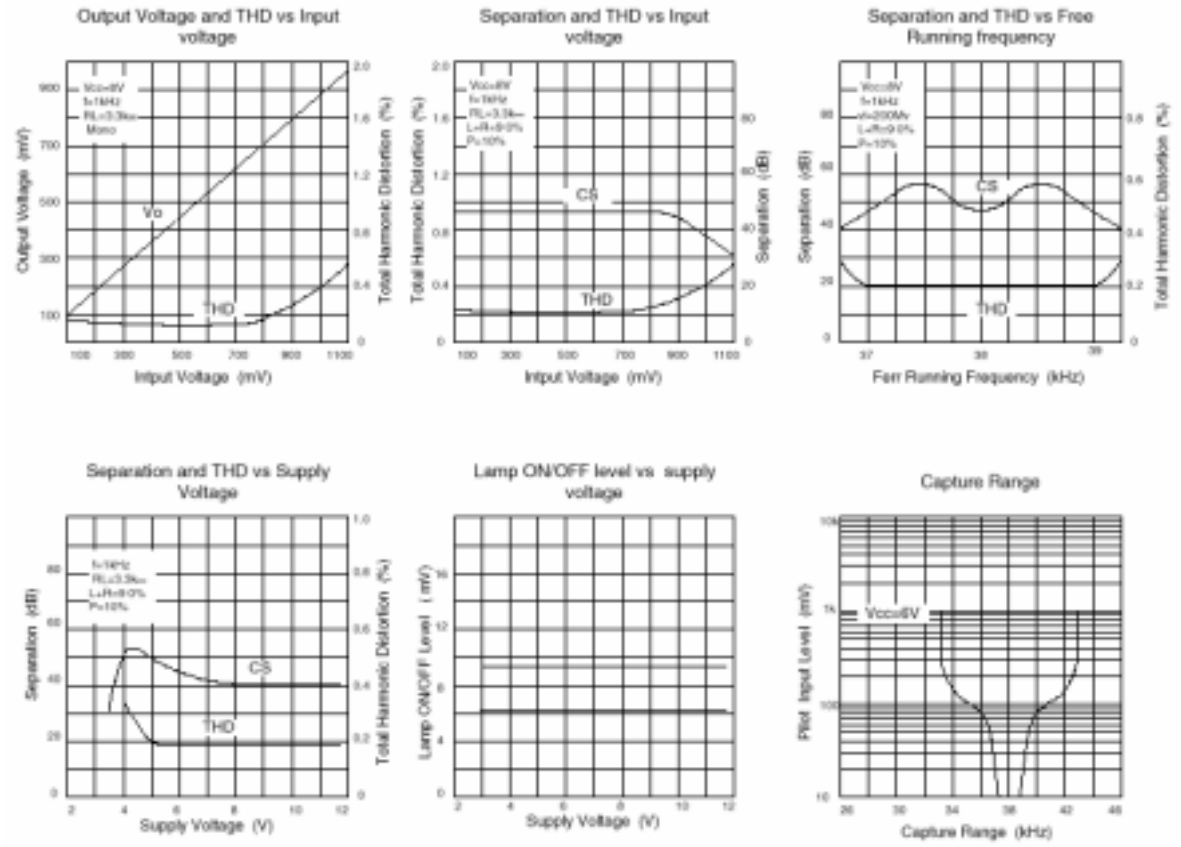


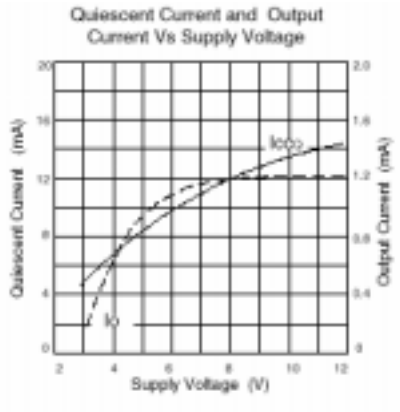


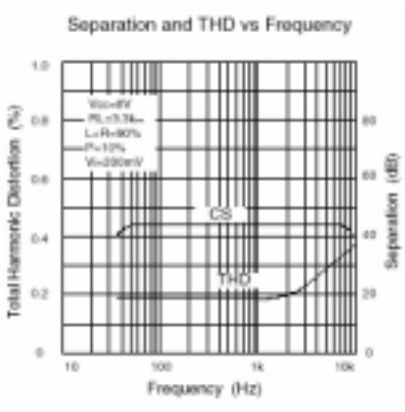
APPLICATION CIRCUIT



CHARACTERISTICS CURVES




Quiescent Current and Output Current Vs Supply Voltage
Quiescent Current (mA)
Output Current (mA)
Supply Voltage (V)
Icc
Io


Separation and THD vs Frequency
Total Harmonic Distortion (%)
Separation (dB)
Frequency (Hz)
CS
THD