DATA SHEET

CX77112 PA Module for CDMA PCS (1850–1910 MHz)

Applications

- Personal Communications Services (PCS)
- Wireless Local Loop (WLL)

Features

- Low voltage positive bias supply
  - 3.2 V to 4.2 V
- Low VREF
  - 2.85 V, nominal
- Good linearity
- High efficiency
- Large dynamic range
- 10-pin package
  - 4 mm x 4 mm x 1.5 mm
- Power down control
- Low power-state control
- InGaP
- IS95/CDMA2000
- Full U.S. PCS coverage

Description

The CX77112 Power Amplifier Module (PAM) is a fully matched 10-pin surface mount module developed for Personal Communications Service (PCS) and Wireless Local Loop (WLL) applications. This small and efficient Power Amplifier packs full 1850–1910 MHz bandwidth coverage into a single compact package. The CX77112 meets the stringent spectral linearity requirements of Code Division Multiple Access (CDMA) PCS transmission, with high power added efficiency for power output of up to 29 dBm. A low current (VCONT) pin is provided to improve efficiency for the low RF power range of operation.

The single Gallium Arsenide (GaAs) Microwave Monolithic Integrated Circuit (MMIC) contains all active circuitry in the module. The MMIC contains on-board bias circuitry, as well as input and interstage matching circuits. Output match is realized off-chip within the module package to optimize efficiency and power performance into a 50 Ω load. This device is manufactured with Skyworks' GaAs Heterojunction Bipolar Transistor (HBT) process that provides for all positive voltage DC supply operation while maintaining high efficiency and good linearity. Primary bias to the CX77112 is supplied directly from a three-cell Ni-Cd, a single-cell Li-Ion, or other suitable battery with an output in the 3 to 4 volt range. Power down is accomplished by setting the voltage on the low current reference pin to zero volts. No external supply side switch is needed as typical "off" leakage is a few microamperes with full primary voltage supplied from the battery.

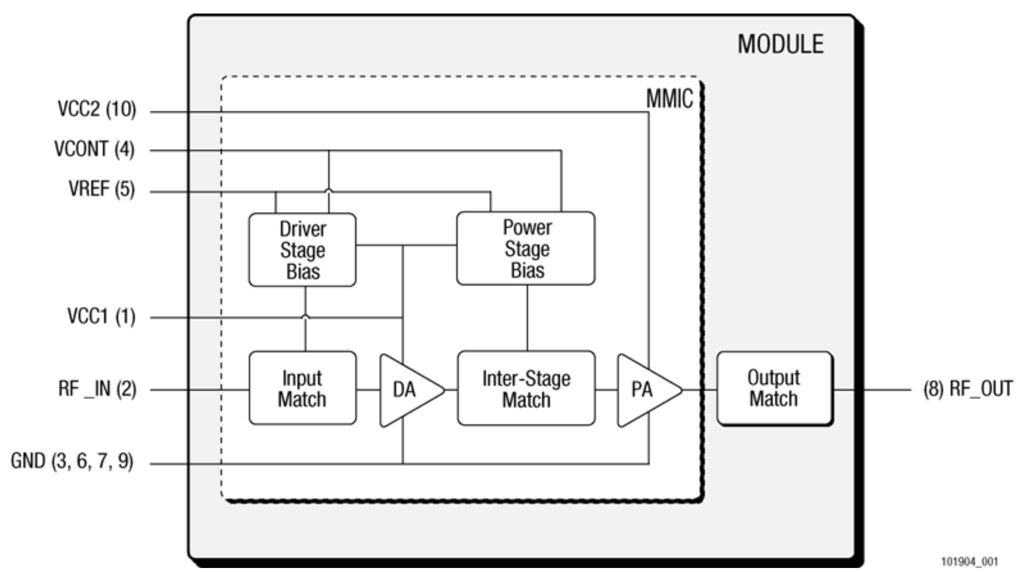


Figure 1. Functional Block Diagram

Electrical Specifications

The following tables list the electrical characteristics of the CX77112 Power Amplifier Module. Table 1 lists the absolute maximum ratings, while Table 2 shows the recommended operating conditions to achieve the performance characteristics listed in Table 4. Table 3 presents a truth table for the power ranges.

Table 1. Absolute Maximum Ratings (1)

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
RF Input Power	P_{IN}	—	1.0	6.0	dBm
Supply Voltage	V_{CC}	—	3.4	6.0	Volts
Reference Voltage	V_{REF}	—	2.85	3.1	Volts
Case Operating Temperature	T_C	–30	25	+110	°C
Storage Temperature	T_{STG}	–55	—	+125	°C

(1) No damage assuming only one parameter is set at limit at a time with all other parameters set at nominal value.

Table 2. Recommended Operating Conditions

Parameter		Symbol	Minimum	Nominal	Maximum	Unit
Supply Voltage		V_{CC}	3.2	3.4	4.2	Volts
Reference Voltage		V_{REF}	2.75	2.85	2.95	Volts
Control voltage	Low Power Mode	V_{CONT}	2.0	2.5	3.0	Volts
	High Power Mode	V_{CONT}	0.0	0.5	1.0	Volts
Operating Frequency		F_O	1850.0	1880.0	1910.0	MHz
Operating Temperature		T_O	–30	+25	+85	°C

Table 3. Power Range Truth Table

	V_{REF}	V_{CONT}	Range
High Power	2.85 V	0.5 V	16 dBm to 29 dBm
Low Power	2.85 V	2.5 V	≤ 16 dBm
Shut Down	0.00 V	0.0 V	—

Table 4. Electrical Specifications for CDMA Nominal Operating Conditions (1)

Characteristics		Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain conditions	Digital Mode	G_{LOW}	V_{CONT} = 2.5 V P_O = 16 dB	24.0	25.0	26.3	dB
		G_{HIGH}	V_{CONT} = 0.5 V P_O = 29 dBm	27.0	28.5	30.0	
Power Added Efficiency	Digital Mode	PAE_{LOW}	V_{CONT} = 2.5 V P_O = 16 dB	7.0	8.5	—	%
		PAE_{HIGH}	V_{CONT} = 0.5 V P_O = 29 dBm	37.0	40.0	—	
Total Supply current		I_{CC_LOW} I_{CC_HIGH}	P_O = 16 dBm P_O = 29 dBm	— —	135 580	160 625	mA
Quiescent current		I_{Q_LOW} I_{Q_HIGH}	V_{CONT} = 2.5 V V_{CONT} = 0.5 V	35 80	50 95	65 115	mA
Reference current		I_{REF}	—	—	6.0	10.0	mA
Control current		I_{CONT}	V_{CONT} = 2.5 V	—	140	250	μA
Total Supply current in Power-down Mode		I_{PD}	V_{CC} = 3.4 V V_{REF} = 0 V	—	3.0	4.0	μA
Adjacent Channel Power (2)(3)	1.25 MHz offset	$ACP1_{LOW}$	V_{CONT} = 2.5 V P_O = 16 dB	—	–50	–48	dBc
		$ACP1_{HIGH}$	V_{CONT} = 0.5 V P_O = 29 dBm	—	–51	–49	
	2.25 MHz offset	$ACP3_{LOW}$	V_{CONT} = 2.5 V P_O = 16 dB	—	–68	–60	
		$ACP3_{HIGH}$	V_{CONT} = 0.5 V P_O = 29 dBm	—	–60	–57	
Harmonic Suppression	Second Third	F_O2 F_O3	$P_O \leq$ 29 dBm $P_O \leq$ 29 dBm	— —	–35 –55	–32 –40	dBc
Noise Power in RX Band 1930-1990 MHz		RxBN	$P_O \leq$ 29 dBm	—	–136	–135	dBm/Hz
Noise Figure		NF	—	—	5.5	6.0	dB
Input Voltage Standing Wave Ratio		VSWR	—	—	—	2.0:1	—
Stability (Spurious output)		S	5:1 VSWR All phases	—	—	–65	dBc
Ruggedness – No damage (4)		Ru	$P_O \leq$ 29 dBm	10:1	—	—	VSWR

(1) V_{CC} = +3.4 V, V_{REF} = +2.85 V, Freq = 1880 MHz, T_C = 25 °C, unless otherwise specified

(2) ACP is specified per IS95 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW.

(3) CDMA2000 is configured as DCHH = 9600, SCHO = 9600, PCH (Walsh 0) = –3.75 dB, and Peak-to-Average Ratio (CCDF = 1%) = 4.45 dB. For CDMA2000, back off output power 0.5 dB is required.

(4) All phases, time = 10 seconds.

Table 5. Electrical Specifications for CDMA Recommended Operating Conditions (1)

Characteristics		Symbol	Condition	Minimum	Maximum	Unit
Gain conditions	Digital Mode	G_{LOW}	V_{CONT} = 2.5 V P_O = 16 dBm	21.0	29.0	dB
		G_{HIGH}	V_{CONT} = 0.5 V P_O = 29 dBm	24.5	33.0	
Adjacent Channel Power (2)(3)(4)	1.25 MHz offset	$ACP1_{LOW}$	V_{CONT} = 2.5 V $P_O \leq$ 16 dBm	—	–44	dBc
		$ACP1_{HIGH}$	V_{CONT} = 0.5 V $P_O \leq$ 29 dBm	—	–43	
	2.25 MHz offset	$ACP3_{LOW}$	V_{CONT} = 2.5 V $P_O \leq$ 16 dBm	—	–56	
		$ACP3_{HIGH}$	V_{CONT} = 0.5 V $P_O \leq$ 29 dBm	—	–56	
Harmonic Suppression	Second	F_O2	$P_O \leq$ 29 dBm	—	–30	dBc
	Third	F_O3	$P_O \leq$ 29 dBm	—	–40	
Noise Power in RX Band 1840-1895 MHz		RxBN	$P_O \leq$ 29 dBm	—	–132.0	dBm/Hz
Noise Figure		NF	—	—	7.0	dB
Input Voltage Standing Wave Ratio (VSWR)		VSWR	—	—	2.5:1	—
Stability (Spurious output)		S	5:1 VSWR All phases	—	–65.0	dBc
Ruggedness – No damage (5)		Ru	$P_O \leq$ 29 dBm	10:1	—	VSWR

(1) Per Table 2, unless otherwise specified.

(2) ACP is specified per IS95 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW.

(3) CDMA2000 is configured as DCCH = 9600, SCHO = 9600, PCH (Walsh 0) = –3.75 dB, and Peak-to-Average Ratio (CCDF = 1%) = 4.5 dB. For CDMA2000, back off output power 0.5 dB is required.

(4) Worst case ACPR is –43 dBc at +85 °C, V_{CC} = 3.2 V.

(5) All phases, time = 10 seconds.

Characterization Data

The following graphs illustrate the characteristics of a typical CX77112 Power Amplifier Module designed for operation in the PCS frequency band (1850–1910 MHz). This amplifier was selected by characterizing a group of devices and choosing a part with average electrical performance for both nominal and the full range of recommended operating conditions, including worst case limits.

Figure 2 through Figure 8 illustrate the digital signal characteristics of the CX77112. Shown are power sweep characteristics for key performance parameters over temperature and frequency, up to 28.5 dBm output power. The data was taken up to and including 16 dBm output power with the bias mode control pin setting of VCONT = 2.5 volts. Beyond 16 dBm output power, the VCONT was set to 0 volts.

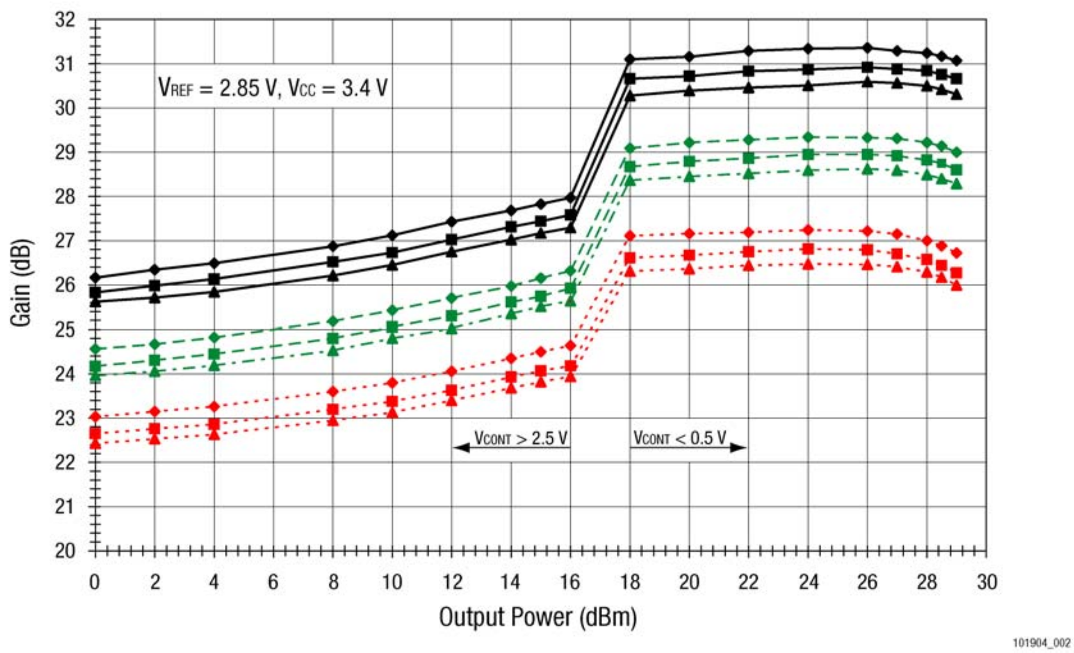
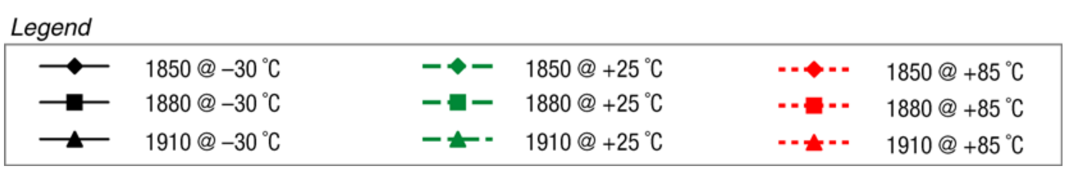


Figure 2. Digital Mode Gain vs. Output Power



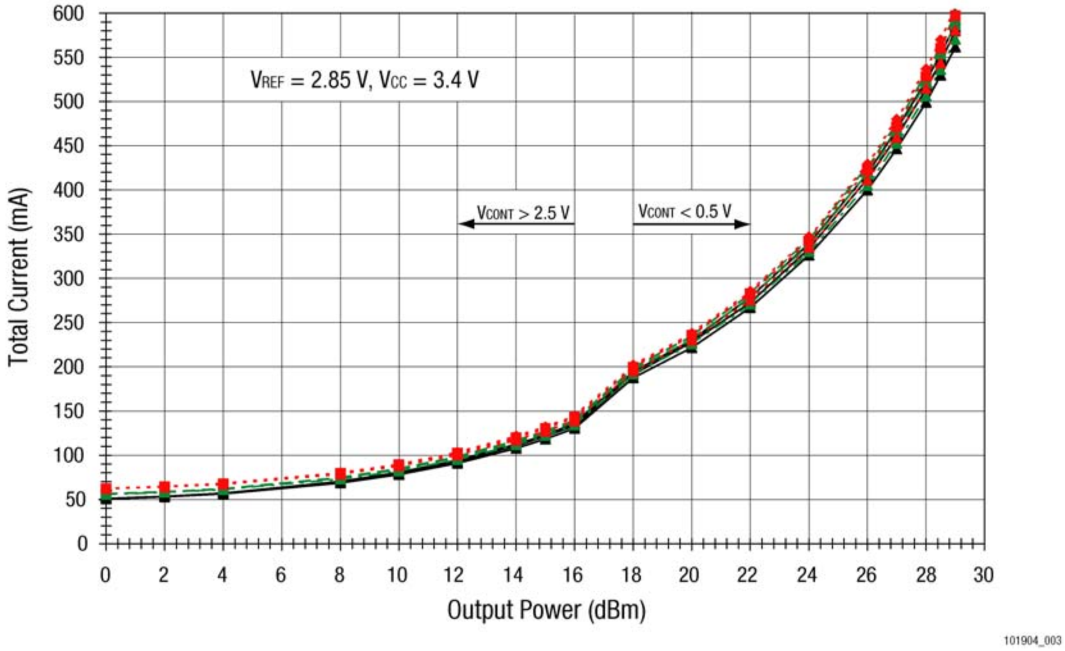


Figure 3. Primary Bias Current vs. Output Power

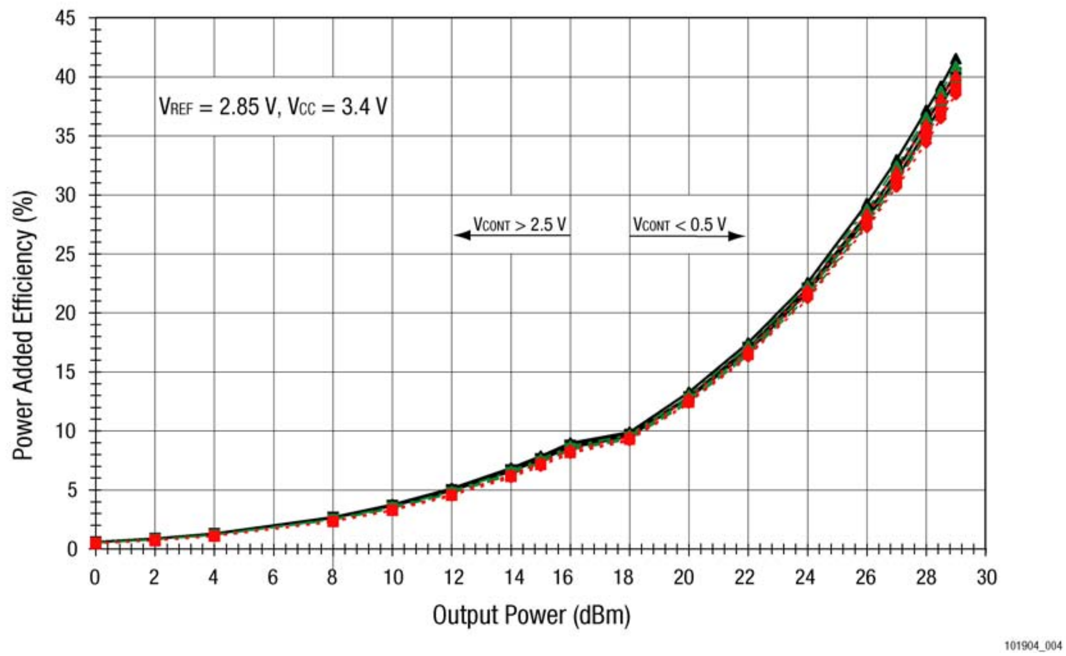
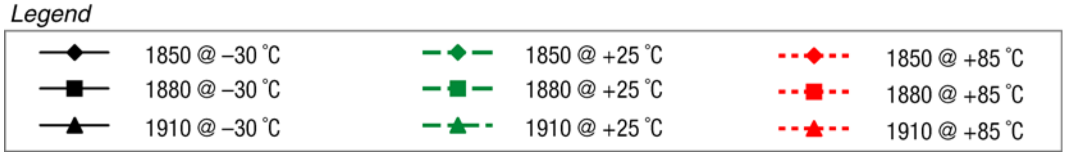


Figure 4. Power Added Efficiency vs. Output Power

Legend



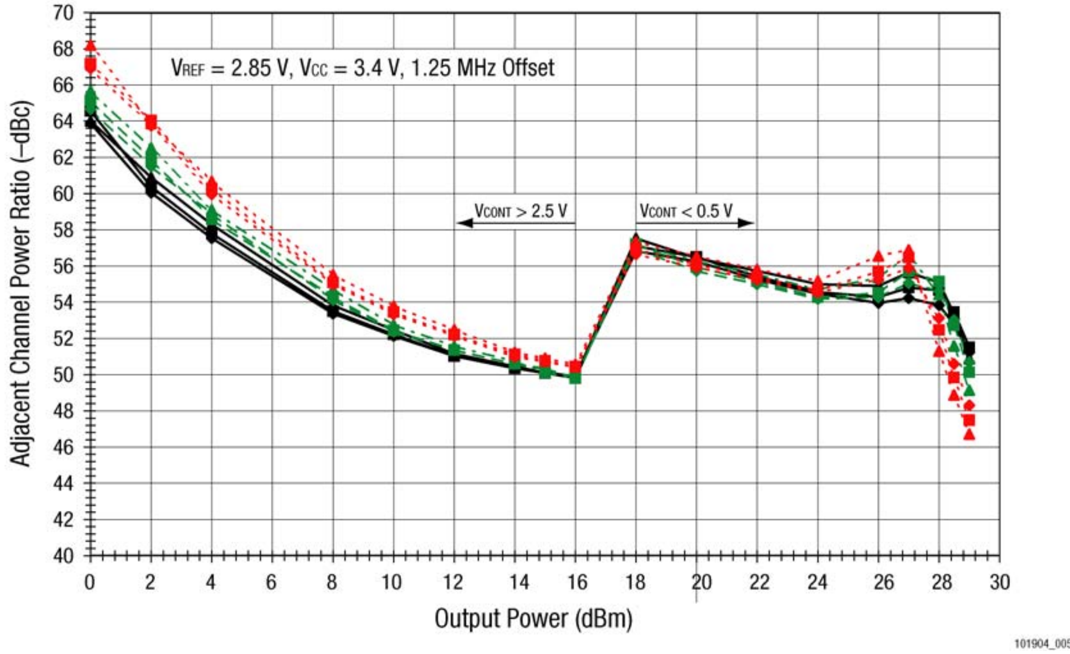


Figure 5. Adjacent Channel Power for 1.25 MHz Offset vs. Output Power

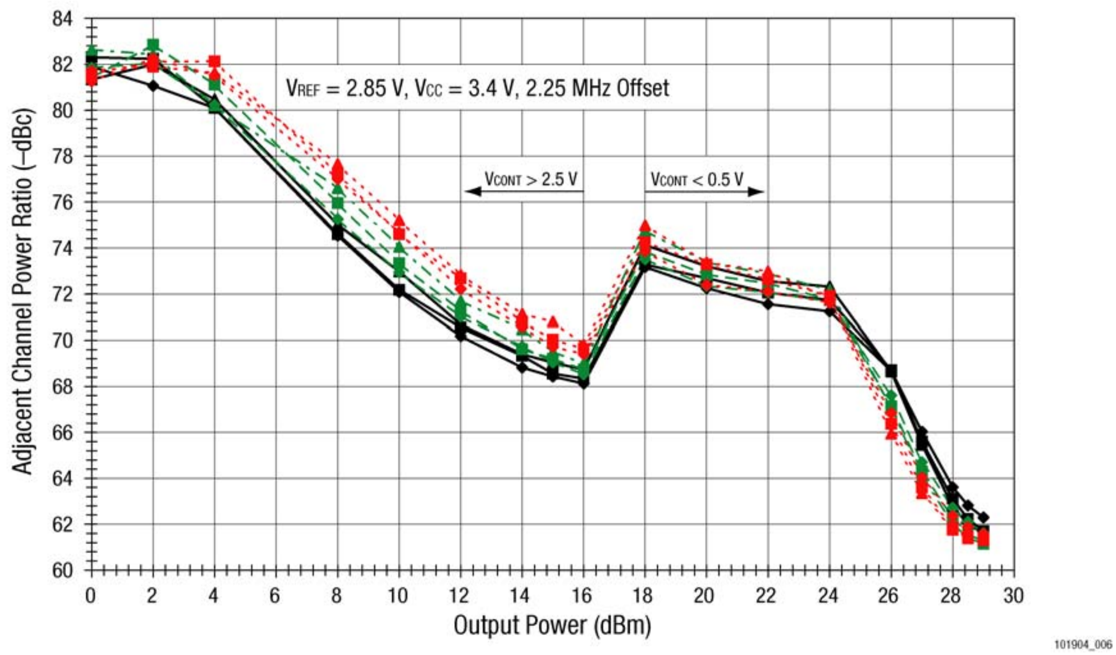
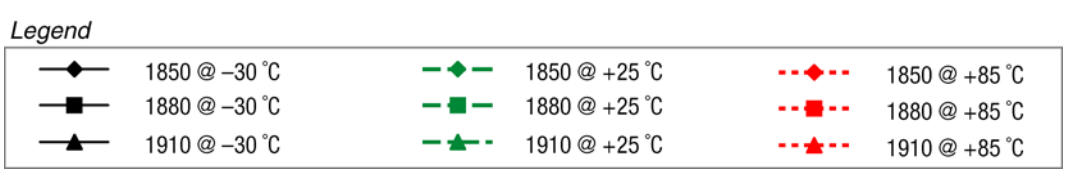


Figure 6. Adjacent Channel Power for 2.25 MHz Offset vs. Output Power



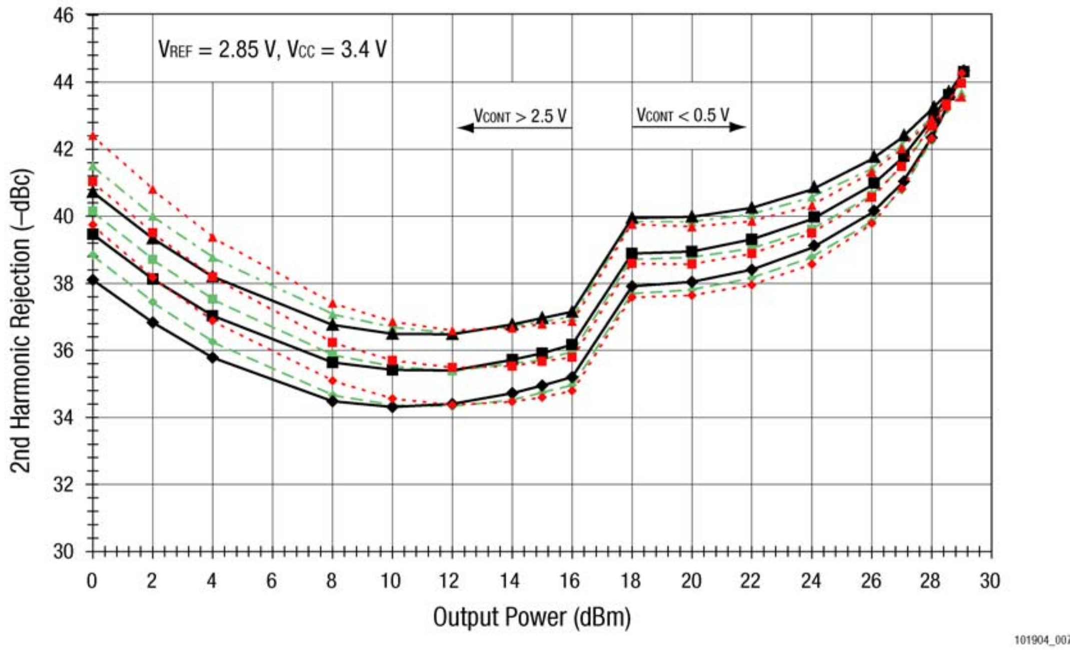


Figure 7. Second Harmonic Rejection vs. Output Power

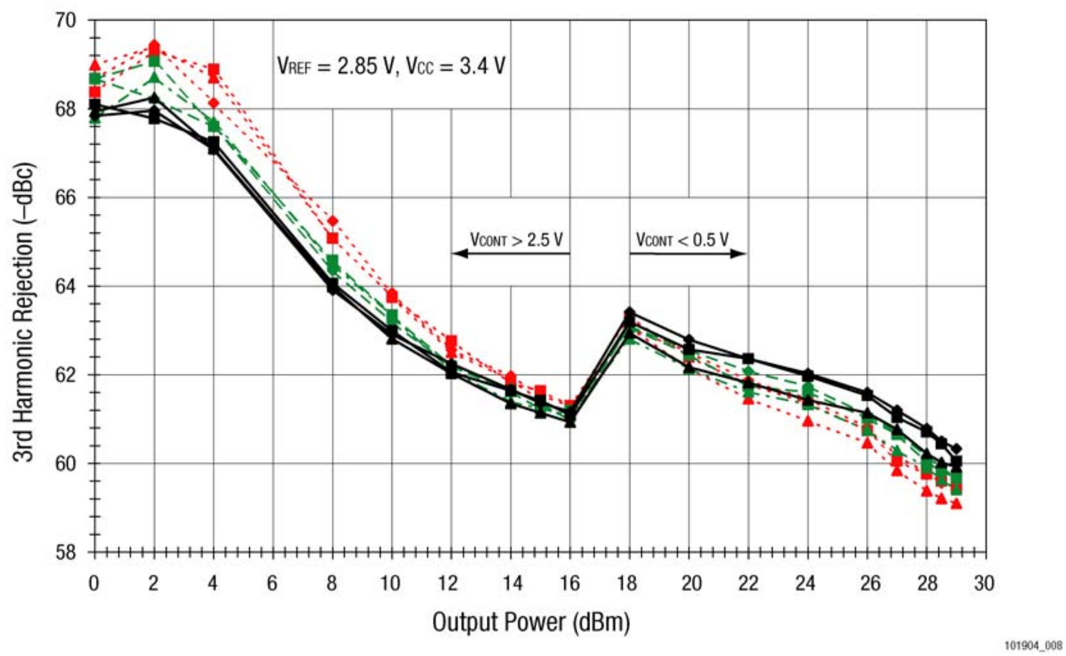
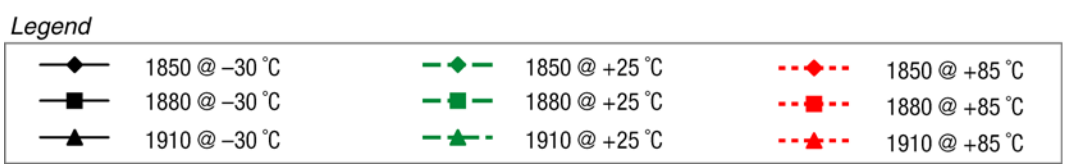


Figure 8. Third Harmonic Rejection vs. Output Power



Evaluation Board Description

The evaluation board is a platform for testing and interfacing design circuitry. To accommodate the interface testing of the CX77112, the evaluation board schematic and diagrams are included for preliminary analysis and design. Figure 9 shows the basic schematic of the board for the 1850 MHz to 1910 MHz range.

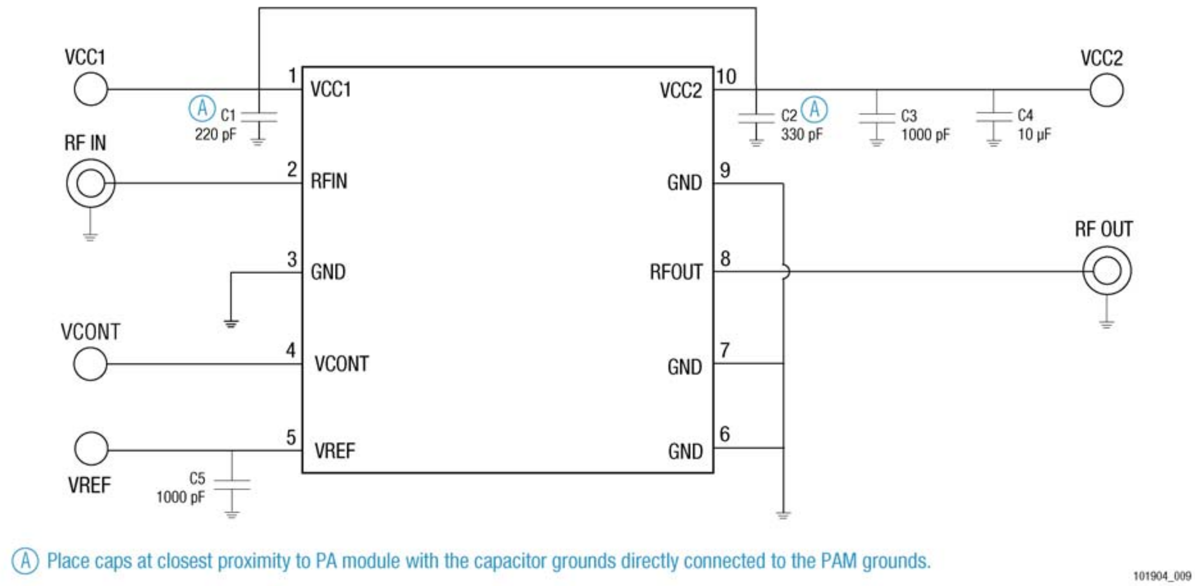


Figure 9. Evaluation Board Schematic

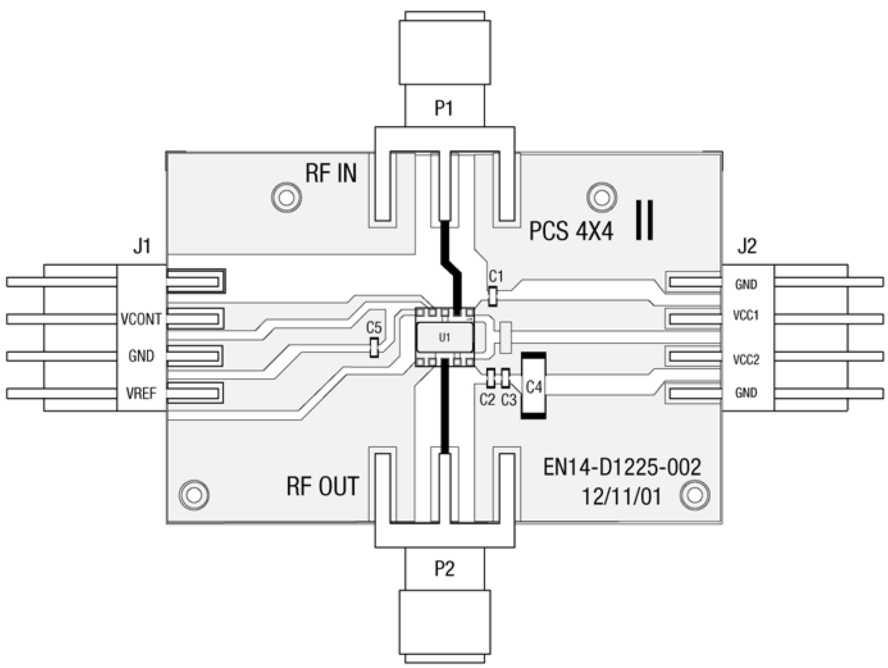


Figure 10. Evaluation Board Assembly Diagram

Package Dimensions and Pin Descriptions

The CX77112 is a multi-layer laminate base, overmold encapsulated modular package designed for surface mount solder attachment to a printed circuit board. Figure 11 is a mechanical drawing of the pad layout for this package. Figure 12 provides a recommended phone board layout footprint for the PAM to help the designer attain optimum thermal conductivity, good grounding, and minimum RF discontinuity for the 50-ohm terminals. Figure 13 illustrates the pin configuration and numbering convention, which starts with pin 1 in the upper left and increments counter-clockwise around the package. Table 6 describes each pin function. Figure 14 shows typical case markings.

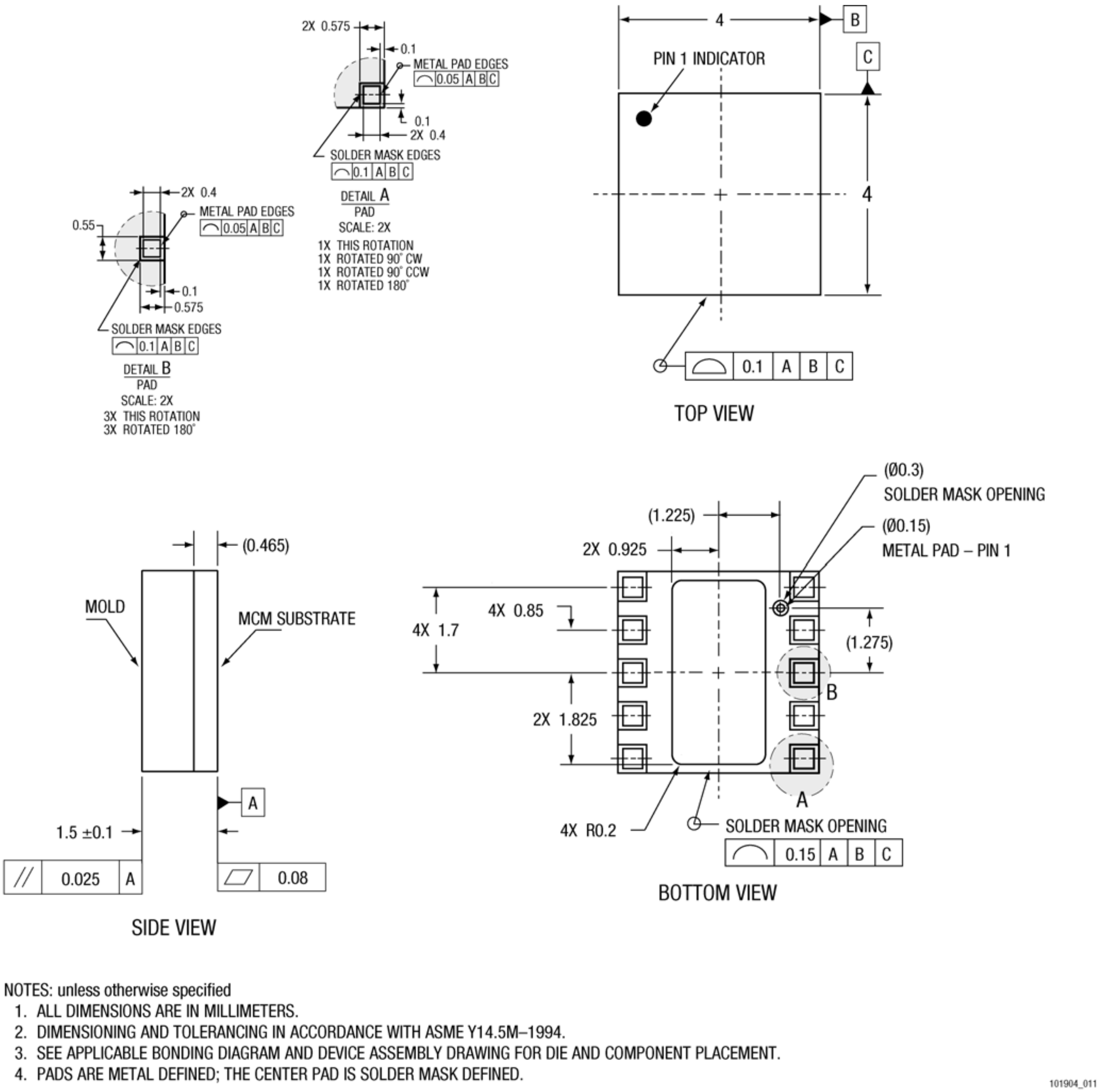


Figure 11. CX77112 Package Drawing

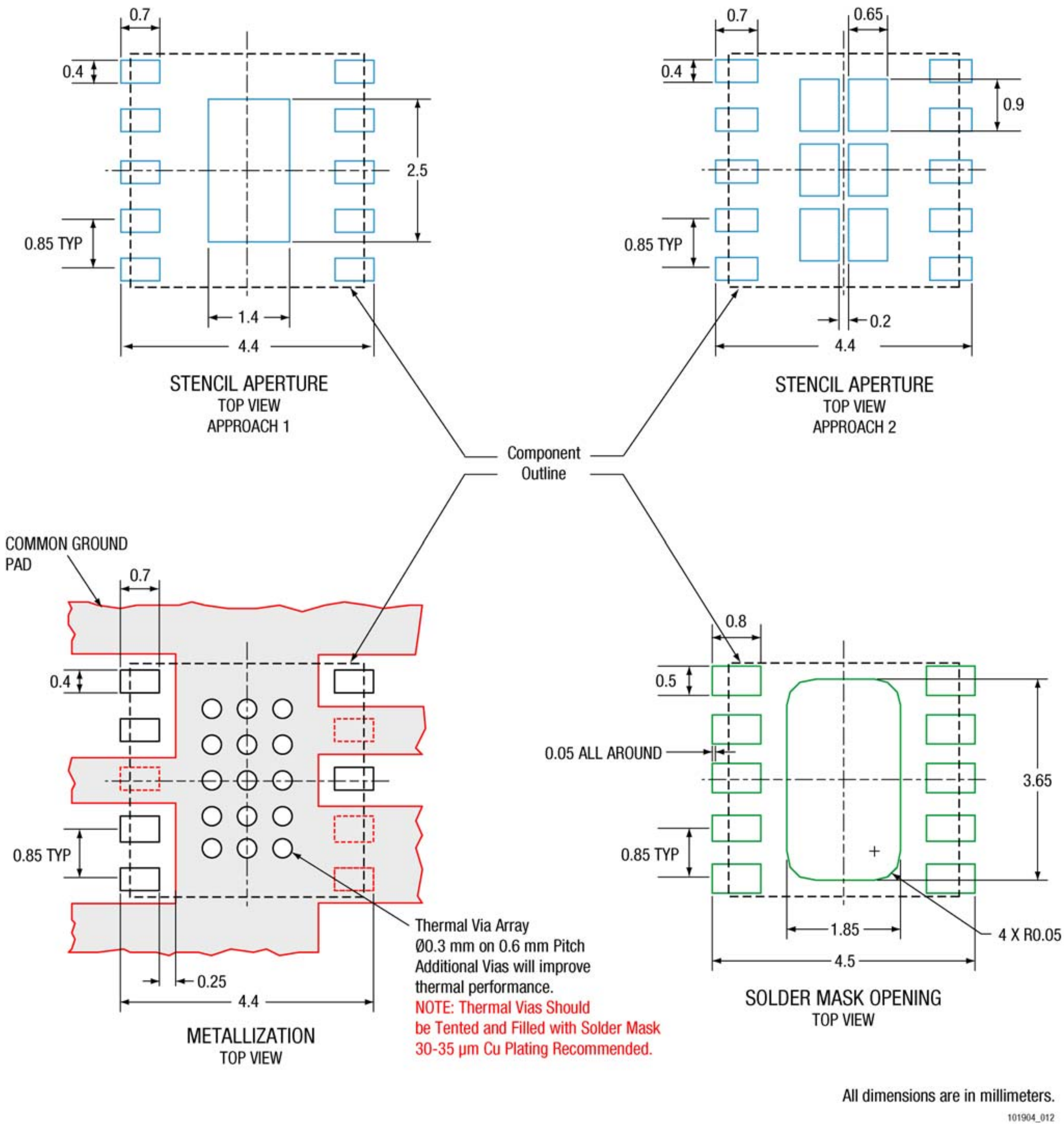


Figure 12. Phone PCB Layout Footprint for 4 x 4 mm, 10-Pin Package – CX77112

Table 6. CX77112 Pin Configuration and Descriptions

PIN Number	Function	Description
1	VCC1 (1)	Connect to battery or DC supply
2	RF IN	RF Input
3	GND	Ground
4	VCONT	Control voltage
5	VREF	Reference voltage
6	GND	Ground
7	GND	Ground
8	RF OUT	RF Output
9	GND	Ground
10	VCC2 (1)	Connect to battery or DC supply
GND PAD	GND (2)	Ground pad on underside of package

(1) All supply pins may be connected together at the supply.

(2) Package underside is GND.

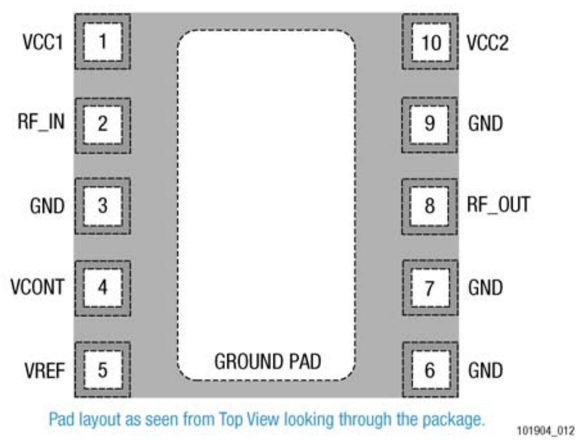


Figure 13. CX77112 Pin Configuration

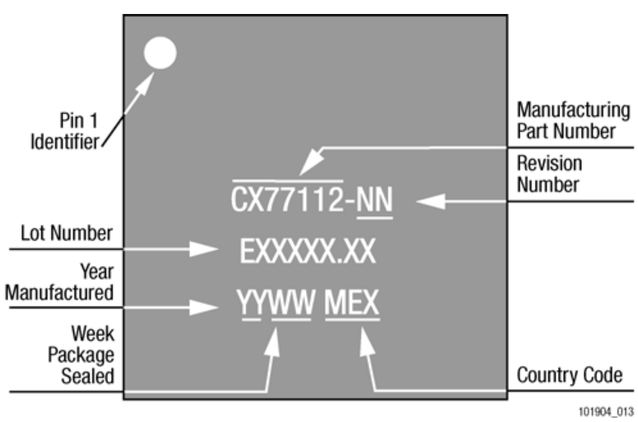


Figure 14. Typical Case Markings

Package and Handling Information

Because of its sensitivity to moisture absorption, this device package is baked and vacuum-packed prior to shipment. Instructions on the shipping container label must be followed regarding exposure to moisture after the container seal is broken, otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The CX77112 is capable of withstanding an MSL3/240 °C solder reflow. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 5 °C per second; maximum temperature should not exceed 240 °C. If the part is manually attached, precaution should be taken to insure that the part is not subjected to temperatures exceeding 240 °C for more than 10 seconds. For details on attachment techniques, precautions, and handling procedures recommended by Skyworks, please refer to Skyworks Application Note: *PCB Design and SMT Assembly/Rework*, Document Number 101752. Additional information on standard SMT reflow profiles can also be found in the *JEDEC Standard J-STD–020*.

Production quantities of this product are shipped in the standard tape-and-reel format. For packaging details, refer to Skyworks Application Note: *Tape and Reel Information –RF Modules*, Document Number 101568.

Electrostatic Discharge Sensitivity

The CX77112 is a Class 2 device. Figure 15 lists the Electrostatic Discharge (ESD) immunity level for each non-ground pin of the CX77112 product. ESD testing was performed in compliance with MIL-STD-883E Method 3015.7 using the Human Body Model. The numbers in Figure 15 specify the ESD threshold level for each pin where the I-V curve between the pin and ground starts to show degradation.

Various failure criteria can be utilized when performing ESD testing. Many vendors employ relaxed ESD failure standards that fail devices only after “the pin fails the electrical specification limits” or “the pin becomes completely non-functional”. Skyworks employs most stringent criteria to fail devices as soon as the pin begins to show any degradation on a curve tracer. If ESD damage threshold magnitude is found to consistently exceed 2000 volts on a given pin, this so is indicated. If ESD damage threshold below 2000 volts is measured for either polarity, numbers are indicated that represent worst case values observed in product characterization.

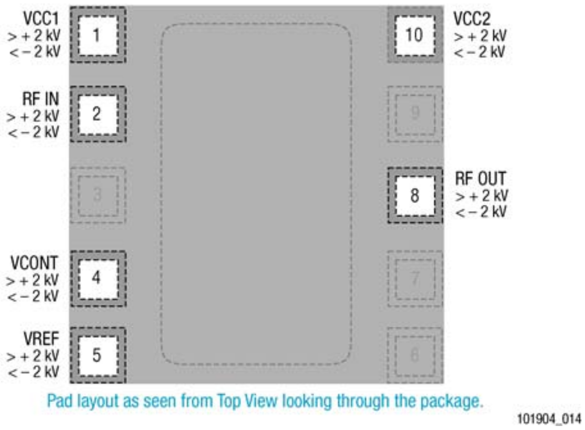


Figure 15. CX77112 ESD Sensitivity Areas (Top View)

To avoid ESD damage, both latent and visible, it is very important that the product assembly and test areas observe these Class 2 ESD handling precautions for GaAs IC-based products to avoid induced damage.

- Personnel Grounding
  - Wrist Straps
  - Conductive Smocks, Gloves and Finger Cots
  - Antistatic ID Badges
- Facility
  - Relative Humidity Control and Air Ionizers
  - Dissipative Floors (less than 10^9 Ω to GND)
- Protective Workstation
  - Dissipative Table Tops
  - Protective Test Equipment (Properly Grounded)
  - Grounded Tip Soldering Irons
  - Conductive Solder Suckers
  - Static Sensors
- Protective Packaging & Transportation
  - Bags and Pouches (Faraday Shield)
  - Protective Tote Boxes (Conductive Static Shielding)
  - Protective Trays
  - Grounded Carts
  - Protective Work Order Holders

Skyworks Ordering Information

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
CX77112	CX77112		4x4LM–10	–30 °C to +85 °C

Revision History

Revision	Level	Date	Description
A		June 17, 2003	Initial Release
B		July 14, 2003	Revise: Table 2, 3, 4, 5
C		August 22, 2003	Revise: Table 1
D		November 25, 2003	Revise: Table 5
E		May 19, 2004	Revise: Figure 1
F		June 1, 2005	Add: Figure 12

References

Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752.

Application Note: Tape and Reel, Document Number 101568.

JEDEC Standard J-STD-020