DATA SHEET

Low Voltage 1:18 Clock Distribution Chip

MPC942P

The MPC942 is a 1:18 low voltage clock distribution chip with 2.5V or 3.3V LVCMOS output capabilities. The device is offered in two versions; the MPC942C has an LVCMOS input clock while the MPC942P has a LVPECL input clock. The 18 outputs are 2.5V or 3.3V LVCMOS compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output–to–output skews of 200ps, the MPC942 is ideal as a clock distribution chip for the most demanding of synchronous systems. The 2.5V outputs also make the device ideal for supplying clocks for a high performance Pentium II™ microprocessor based design.

LOW VOLTAGE 1:18 CLOCK DISTRIBUTION CHIP

- LVPECL Clock Input
- 2.5V LVCMOS Outputs for Pentium II Microprocessor Support
- 200ps Maximum Targeted Output–to–Output Skew
- Maximum Output Frequency of 250MHz @ 3.3 V_{CC}
- 32–Lead LQFP Packaging
- Single 3.3V or 2.5V Supply

FA SUFFIX
32–LEAD LQFP PACKAGE
CASE 873A–02

With a low output impedance (≈12Ω), in both the HIGH and LOW logic states, the output buffers of the MPC942 are ideal for driving series terminated transmission lines. With an output impedance of 12Ω the MPC942 can drive two series terminated transmission lines from each output. This capability gives the MPC942 an effective fanout of 1:36. The MPC942 provides enough copies of low skew clocks for most high performance synchronous systems.

The differential LVPECL inputs of the MPC942P allow the device to interface directly with a LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The OE pins will place the outputs into a high impedance state. The OE pin has an internal pullup resistor.

The MPC942 is a single supply device. The V_{CC} power pins require either 2.5V or 3.3V. The 32–lead LQFP package was chosen to optimize performance, board space and cost of the device. The 32–lead LQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

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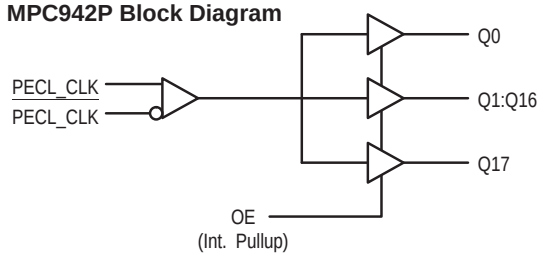
LOGIC DIAGRAM

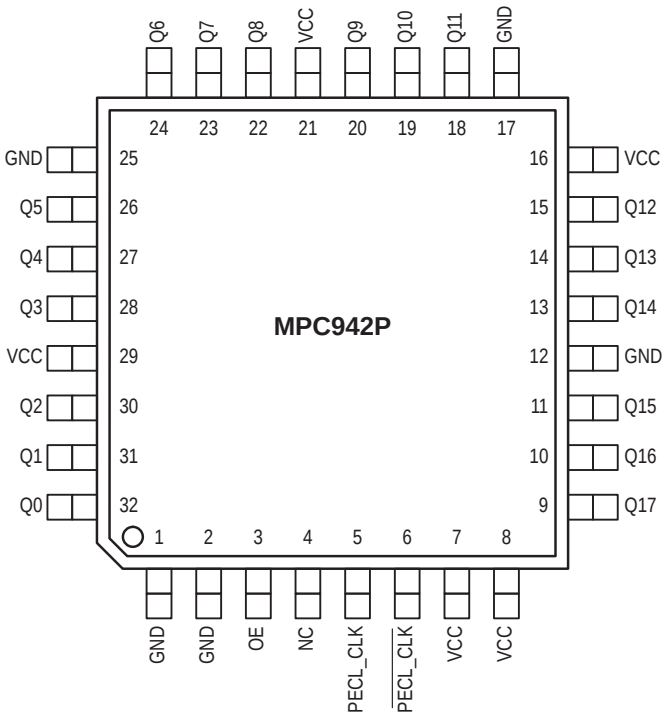
MPC942P Block Diagram



FUNCTION TABLE

OE	Output
0	HIGH IMPEDANCE
1	OUTPUTS ENABLED

Pinout: 32–Lead (Top View)



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	3.6	V
V_I	Input Voltage	–0.3	V_{CC} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 2.5V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{PP}	Input Swing PECL_CLK	0.6		1.0	V	
V_X	Input Crosspoint PECL_CLK	V_{CC}–1.0		V_{CC}–0.6	V	
V_{OH}	Output HIGH Voltage	2.0			V	I_{OH} = –16 mA
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 16 mA
I_{IN}	Input Current			±200	µA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		14		pF	Per Output
Z_{OUT}	Output Impedance		12		Ω	
I_{CC}	Maximum Quiescent Supply Current		0.5	5.0	mA	

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 2.5V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Frequency			200	MHz	
t_{PLH}	Propagation Delay	1.8		4.0	ns	
t_{PHL}	Propagation Delay	2.0		4.3	ns	
$t_{sk(o)}$	Output–to–Output Skew			200	ps	
$t_{sk(pr)}$	Part–to–Part Skew			2.2	ns	Note 2
$t_{sk(pr)}$	Part–to–Part Skew			1.3	ps	Note 1
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	

1. For a specific temperature and voltage, includes output skew.
2. Across temperature and voltage ranges, includes output skew.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.4		V_{CC}	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{PP}	Input Swing PECL.CLK	0.6		1.0	V	
V_X	Input Crosspoint PECL_CLK	V_{CC}–1.0		V_{CC}–0.6	V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –20 mA
V_{OL}	Output LOW Voltage			0.6	V	I_{OL} = 20 mA
I_{IN}	Input Current			±200	µA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		14		pF	Per Output
Z_{OUT}	Output Impedance		12		Ω	
I_{CC}	Maximum Quiescent Supply Current		0.5	5.0	mA	

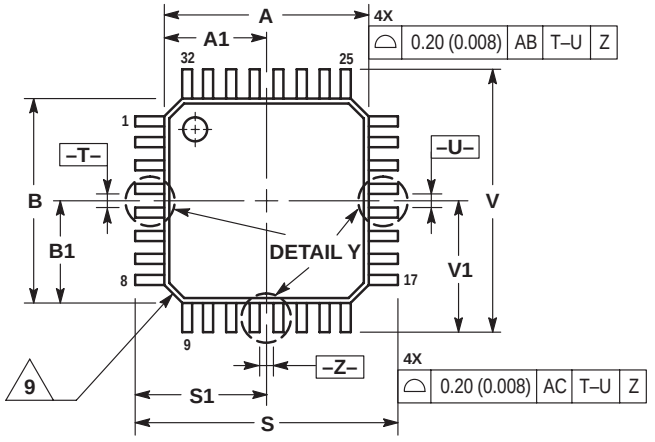
AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

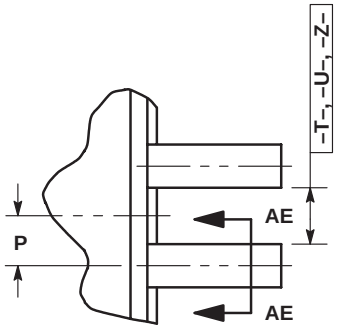
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Frequency			250	MHz	
t_{PLH}	Propagation Delay	1.5		3.2	ns	
t_{PHL}	Propagation Delay	1.5		3.6	ns	
$t_{sk(o)}$	Output–to–Output Skew			200	ps	
$t_{sk(pr)}$	Part–to–Part Skew			1.7	ns	Note 2
$t_{sk(pr)}$	Part–to–Part Skew			1.0	ps	Note 1
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	

1. For a specific temperature and voltage, includes output skew.
2. Across temperature and voltage ranges, includes output skew.

OUTLINE DIMENSIONS

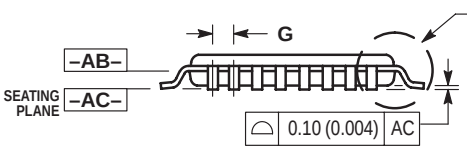
FA SUFFIX
LQFP PACKAGE
CASE 873A–02
ISSUE A

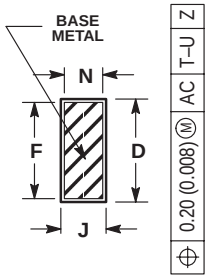




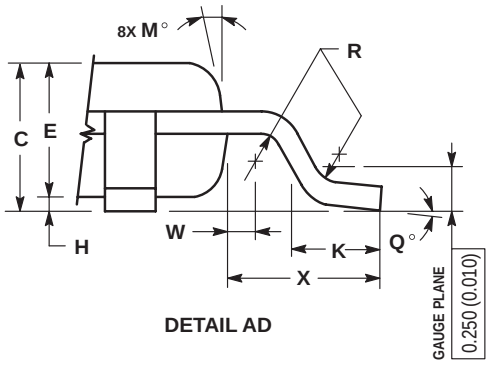
DETAIL Y

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.





SECTION AE–AE



DETAIL AD

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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