

Single Digitally-Controlled (XDCP™) Potentiometer

FEATURES

- 1024 Resistor Taps – 10-Bit Resolution
- 2-Wire Serial Interface for Write, Read, and Transfer Operations of the Potentiometer
- Wiper Resistance, 40Ω Typical @ $V_{CC} = 5V$
- Four Non-Volatile Data Registers
- Non-Volatile Storage of Multiple Wiper Positions
- Power-on Recall. Loads Saved Wiper Position on Power-up.
- Standby Current < 3μA Max
- V_{CC} : 2.7V to 5.5V Operation
- 100kΩ End to End Resistance
- 100 yr. Data Retention
- Endurance: 100,000 Data Changes Per Bit Per Register
- 14 Ld TSSOP
- Low Power CMOS
- Single Supply Version of the X9118
- Pb-Free Plus Anneal Available (RoHS Compliant)

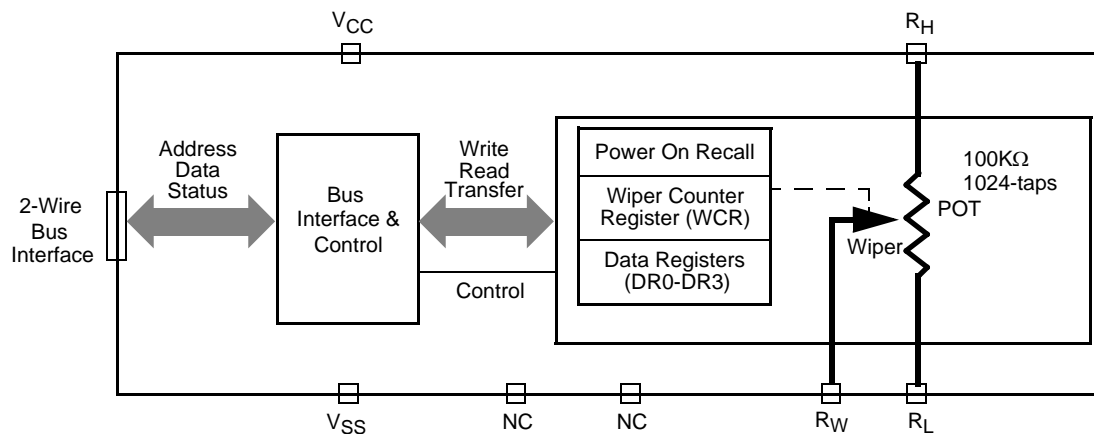
DESCRIPTION

The X9119 integrates a single digitally controlled potentiometer (XDCP) on a monolithic CMOS integrated circuit.

The digital controlled potentiometer is implemented using 1023 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the 2-wire bus interface. The potentiometer has associated with it a volatile Wiper Counter Register (WCR) and a four non-volatile Data Registers that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array through the switches. Powerup recalls the contents of the default data register (DR0) to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

FUNCTIONAL DIAGRAM



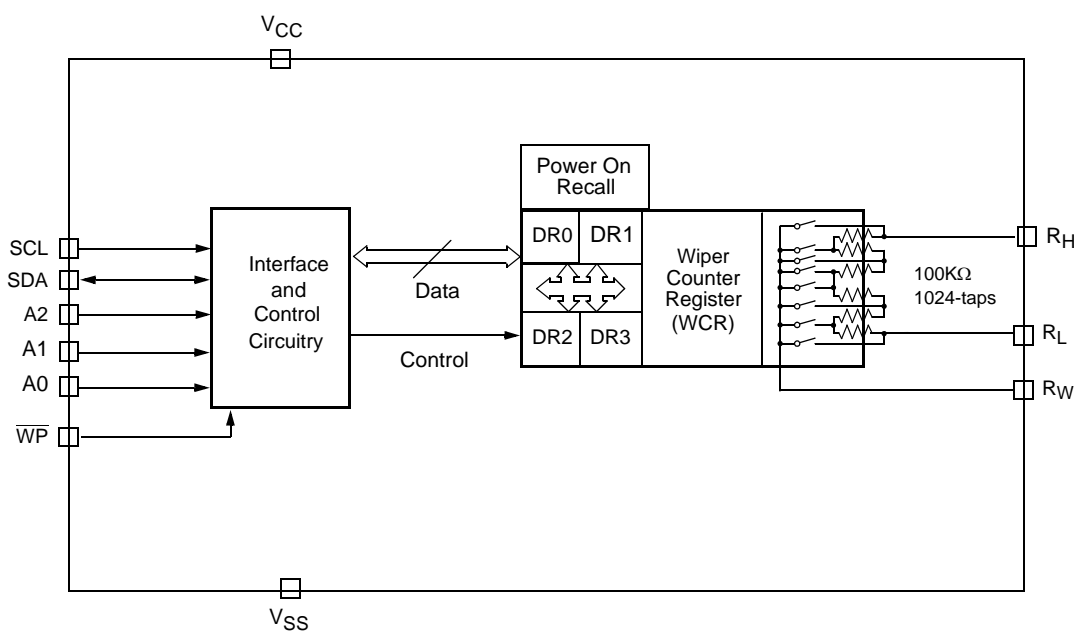
Ordering Information

| PART NUMBER | PART MARKING | V _{CC} LIMITS (V) | POTENTIOMETER ORGANIZATION (k Ω) | TEMP RANGE (°C) | PACKAGE |
|-------------------------|--------------|----------------------------|--|-----------------|-------------------------------|
| X9119TV14I | X9119TV I | 5 \pm 10% | 10 | -40 to 85 | 14 Ld TSSOP (4.4mm) |
| X9119TV14 | X9119TV | | | 0 to 70 | 14 Ld TSSOP (4.4mm) |
| X9119TV14-2.7* | X9119TV F | -2.7 to 5.5 | | 0 to 70 | 14 Ld TSSOP (4.4mm) |
| X9119TV14I-2.7 | X9119TV G | | | -40 to 85 | 14 Ld TSSOP (4.4mm) |
| X9119TV14IZ-2.7* (Note) | | | | -40 to 85 | 14 Ld TSSOP (4.4mm) (Pb-free) |

*Add "T1" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

DETAILED FUNCTIONAL DIAGRAM



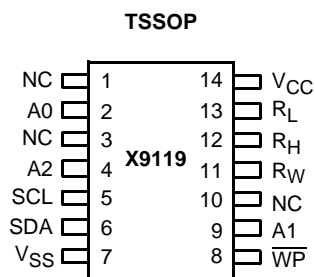
CIRCUIT LEVEL APPLICATIONS

- Vary the gain of a voltage amplifier
- Provide programmable dc reference voltages for comparators and detectors
- Control the volume in audio circuits
- Trim out the offset voltage error in a voltage amplifier circuit
- Set the output voltage of a voltage regulator
- Trim the resistance in Wheatstone bridge circuits
- Control the gain, characteristic frequency and Q-factor in filter circuits
- Set the scale factor and zero point in sensor signal conditioning circuits
- Vary the frequency and duty cycle of timer ICs
- Vary the dc biasing of a pin diode attenuator in RF circuits
- Provide a control variable (I, V, or R) in feedback circuits

SYSTEM LEVEL APPLICATIONS

- Adjust the contrast in LCD displays
- Control the power level of LED transmitters in communication systems
- Set and regulate the DC biasing point in an RF power amplifier in wireless systems
- Control the gain in audio and home entertainment systems
- Provide the variable DC bias for tuners in RF wireless systems
- Set the operating points in temperature control systems
- Control the operating point for sensors in industrial systems
- Trim offset and gain errors in artificial intelligent systems

PIN CONFIGURATION



PIN ASSIGNMENTS

| Pin (TSSOP) | Symbol | Function |
|-------------|-----------------|---|
| 1 | NC | No Connect |
| 2 | A0 | Device Address for 2-wire bus |
| 3 | NC | No Connect |
| 4 | A2 | Device Address for 2-wire bus |
| 5 | SCL | Serial Clock for 2-wire bus |
| 6 | SDA | Serial Data Input/Output for 2-wire bus |
| 7 | V _{SS} | System Ground |
| 8 | \overline{WP} | Hardware Write Protect |
| 9 | A1 | Device Address for 2-wire bus |
| 10 | NC | No Connect |
| 11 | R _W | Wiper terminal of the Potentiometer |
| 12 | R _H | High terminal of the Potentiometer |
| 13 | R _L | Low terminal of the Potentiometer |
| 14 | V _{CC} | System Supply Voltage |

PIN DESCRIPTIONS

Bus Interface Pins

SERIAL DATA INPUT/OUTPUT (SDA)

The SDA is a bidirectional serial data input/output pin for a 2-wire slave device and is used to transfer data into and out of the device. It receives device address, opcode, wiper register address and data sent from an 2-wire master at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock SCL.

It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the guidelines for calculating typical values on the bus pull-up resistors graph.

SERIAL CLOCK (SCL)

This input is used by 2-wire master to supply 2-wire serial clock to the X9119.

DEVICE ADDRESS (A₂-A₀)

The Address inputs are used to set the least significant 3 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the Address input in order to initiate communication with the X9119. A maximum of 8 devices may occupy the 2-wire serial bus.

Hardware Write Protect Input (\overline{WP})

The \overline{WP} pin when LOW prevents nonvolatile writes to the Data Registers.

Potentiometer Pins

R_H, R_L

The R_H and R_L pins are equivalent to the terminal connections on a mechanical potentiometer.

R_W

The wiper pin are equivalent to the wiper terminal of a mechanical potentiometer.

Bias Supply Pins

SYSTEM SUPPLY VOLTAGE (V_{CC}) AND SUPPLY GROUND (V_{SS})

The V_{CC} pin is the system supply voltage. The V_{SS} pin is the system ground.

Other Pins

NO CONNECT

No connect pins should be left open. These pins are used for Intersil manufacturing and testing purposes.

PRINCIPLES OF OPERATION

The X9119 is an integrated microcircuit incorporating a resistor array and its associated registers and counters and the serial interface logic providing direct communication between the host and the digitally controlled potentiometer. This section provides detail description of the following:

- Resistor Array Description
- Serial Interface Description
- Instruction and Register Description

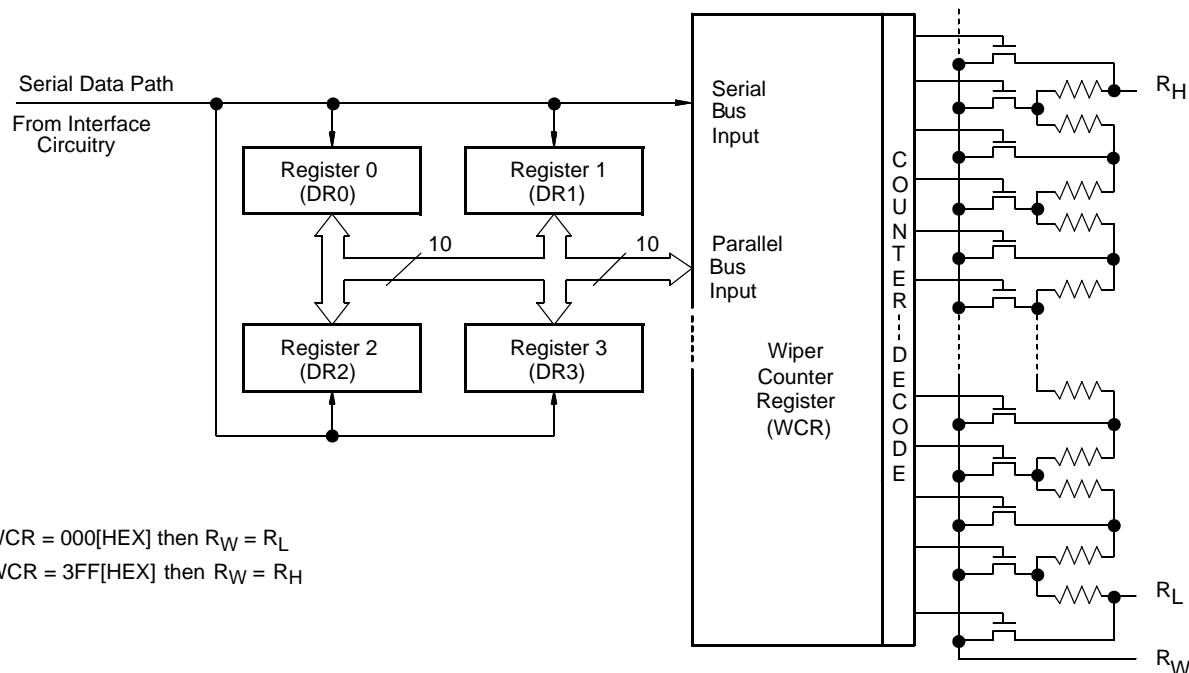
Resistor Array Description

The X9119 is comprised of a resistor array. The array contains, in effect, 1023 discrete resistive segments that are connected in series (see Figure 1). The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L inputs).

At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper (R_W) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by the Wiper Counter Register (WCR). The 10-bits of the WCR (WCR[9:0]) are decoded to select, and enable, one of 1024 switches.

The WCR may be written directly. The Data Registers and the WCR can be read and written by the host system.

Figure 1. Detailed Potentiometer Block Diagram



Serial Interface Description

SERIAL INTERFACE

The X9119 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9119 will be considered a slave device in all applications.

CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. See Figure 3.

START CONDITION

All commands to the X9119 are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The X9119 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met. See Figure 3.

STOP CONDITION

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA while SCL is HIGH. See Figure 3.

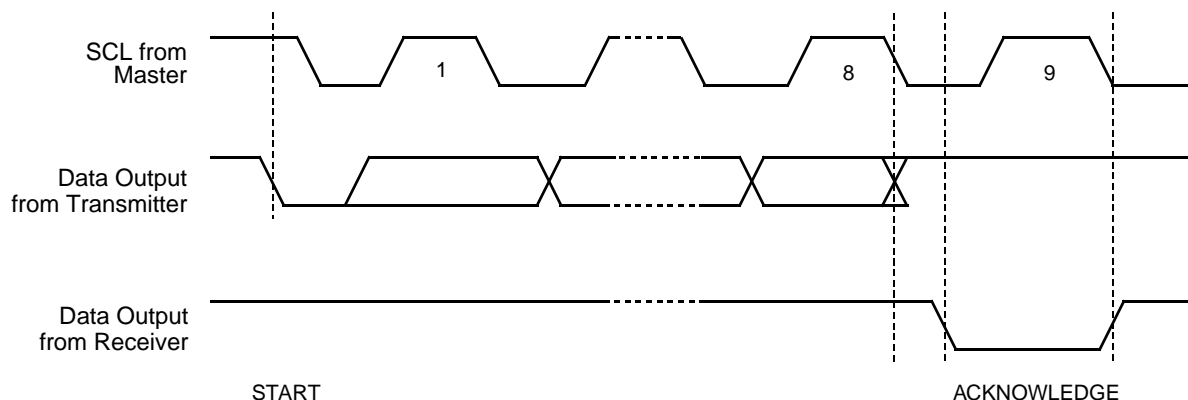
ACKNOWLEDGE

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting eight

bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the eight bits of data.

The X9119 will respond with an acknowledge after recognition of a start condition and its slave address and once again after successful receipt of the command byte. If the command is followed by a data byte the X9119 will respond with a final acknowledge. See Figure 2.

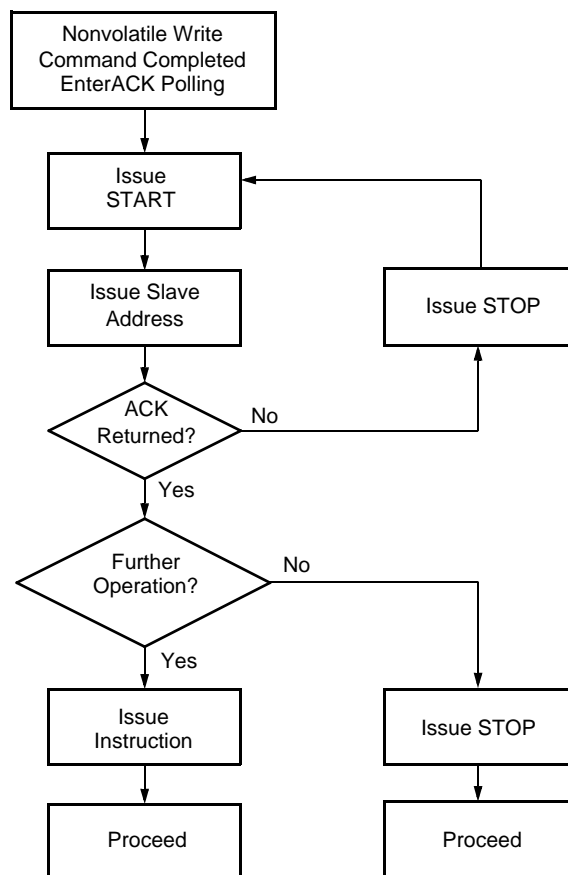
Figure 2. Acknowledge Response from Receiver



ACKNOWLEDGE POLLING

The disabling of the inputs, during the internal nonvolatile write operation, can be used to take advantage of the typical 5ms EEPROM write cycle time. Once the stop condition is issued to indicate the end of the nonvolatile write command the X9119 initiates the internal write cycle. ACK polling, Flow 1, can be initiated immediately. This involves issuing the start condition followed by the device slave address. If the X9119 is still busy with the write operation no ACK will be returned. If the X9119 has completed the write operation an ACK will be returned and the master can then proceed with the next operation.

FLOW 1. ACK Polling Sequence



Instruction and Register Description

DEVICE ADDRESSING: IDENTIFICATION BYTE (ID AND A)

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier. The ID[3:0] bits is the device id for the X9119; this is fixed as 0101[B] (refer to Table 1).

The A2–A0 bits in the ID byte is the internal slave address. The physical device address is defined by the state of the A2–A0 input pins. The slave address is externally specified by the user. The X9119 compares the serial data stream with the address input state; a successful compare of both address bits is required for the X9119 to successfully continue the command

sequence. Only the device which slave address matches the incoming device address sent by the master executes the instruction. The A2–A0 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}. The R/W bit is the LSB and is be used to program the device for read or write operations.

INSTRUCTION BYTE AND REGISTER SELECTION

The next byte sent to the X9119 contains the instruction and register pointer information. The three most significant bits are used provide the instruction opcode (IOP[2:0]). The RB and RA bits point to one of the four registers. The format is shown below in Table 2.

Table 3 provides a complete summary of the instruction set opcodes.

Table 1. Identification Byte Format

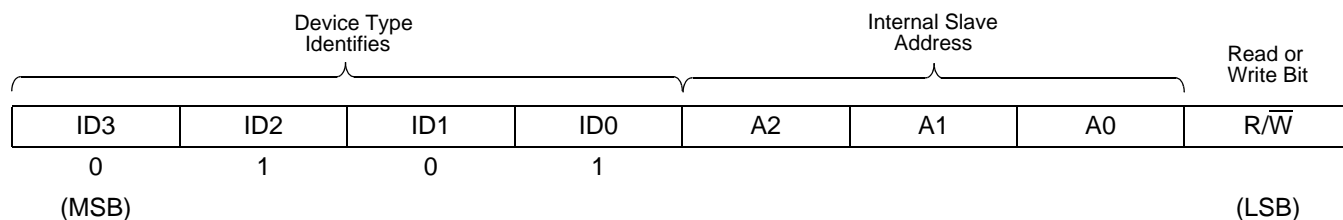
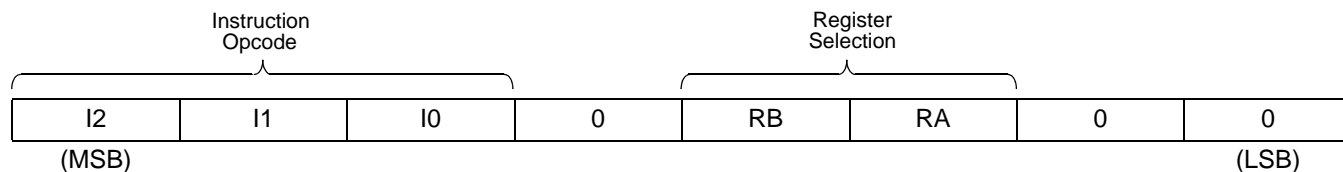


Table 2. Instruction Byte Format



| Register Selected | RB | RA |
|-------------------|----|----|
| DR0 | 0 | 0 |
| DR1 | 0 | 1 |
| DR2 | 1 | 0 |
| DR3 | 1 | 1 |

Table 3. Instruction Set

| Instruction | Instruction Set | | | | | | | | | Operation |
|---|-----------------|----------------|----------------|----------------|---|-----|-----|---|---|---|
| | R/W | I ₂ | I ₁ | I ₀ | 0 | RB | RA | 0 | 0 | |
| Read Wiper Counter Register | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Read the contents of the Wiper Counter Register |
| Write Wiper Counter Register | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Write new value to the Wiper Counter Register |
| Read Data Register | 1 | 1 | 0 | 1 | 0 | 1/0 | 1/0 | 0 | 0 | Read the contents of the Data Register pointed to RB-RA. |
| Write Data Register | 0 | 1 | 1 | 0 | 0 | 1/0 | 1/0 | 0 | 0 | Write new value to the Data Register pointed to RB-RA. |
| XFR Data Register to Wiper Counter Register | 1 | 1 | 1 | 0 | 0 | 1/0 | 1/0 | 0 | 0 | Transfer the contents of the Data Register pointed to by RB-RA.to the Wiper Counter Register |
| XFR Wiper Counter Register to Data Register | 0 | 1 | 1 | 1 | 0 | 1/0 | 1/0 | 0 | 0 | Transfer the contents of the Wiper Counter Register to the Data Register pointed to by RB-RA. |

Note: (1) 1/0 = data is one or zero.

Instruction and Register Description

DEVICE ADDRESSING

WIPER COUNTER REGISTER (WCR)

The X9119 contains a Wiper Counter Registers (see Table 4) for the XDCP potentiometer. The WCR is equivalent to a serial-in, parallel-out register/counter with its outputs decoded to select one of 1024 switches along its resistor array. The contents of the WCR can be altered in one of three ways: (1) it may be written directly by the host via the write wiper counter register instruction (serial load); (2) it may be written indirectly by transferring the contents of one of four associated data registers via the XFR data register; (3) it is loaded with the contents of its data register zero (R0) upon power-up.

The Wiper Counter Register is a volatile register; that is, its contents are lost when the X9119 is powered-down. Although the register is automatically loaded with the value in DR0 upon power-up, this may be different from the value present at power-down. Power-up guidelines are recommended to ensure proper loadings of the DR0 value into the WCR.

DATA REGISTERS (DR0 TO DR3)

The potentiometer has four 10-bit non-volatile Data Registers. These can be read or written directly by the host. Data can also be transferred between any of the four Data Registers and the Wiper Counter Register. All operations changing data in one of the data registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

Bit 9–Bit 0 are used to store one of the 1024 wiper position (0 ~1023).

Table 4. Wiper Control Register, WCR (10-bit), WCR9–WCR0: Used to store the current wiper position (Volatile, V)

| | | | | | | | | | |
|-------|------|------|------|------|------|------|------|------|-------|
| WCR9 | WCR8 | WCR7 | WCR6 | WCR5 | WCR4 | WCR3 | WCR2 | WCR1 | WCR0 |
| V | V | V | V | V | V | V | V | V | V |
| (MSB) | | | | | | | | | (LSB) |

Table 5. Data Register, DR (10-bit), Bit 9–Bit 0: Used to store wiper positions or data (Non-Volatile, NV)

| | | | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| NV | NV | NV | NV | NV | NV | NV | NV | NV | NV |
| MSB | | | | | | | | | LSB |

Four of the six instructions are four bytes in length. These instructions are:

- **Read Wiper Counter Register** – read the current wiper position of the selected potentiometer,
- **Write Wiper Counter Register** – change current wiper position of the selected potentiometer,
- **Read Data Register** – read the contents of the selected Data Register;
- **Write Data Register** – write a new value to the selected Data Register.

The basic sequence of the four byte instructions is illustrated in Figure 3. These four-byte instructions exchange data between the WCR and one of the Data Registers. A transfer from a data register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action will be delayed by $t_{WR,L}$. A transfer from the WCR (current wiper position), to a data register is a write to nonvolatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between one of the four potentiometers and one of its associated registers.

Two instructions (see Figure 4) require a two-byte sequence to complete. These instructions transfer data between the host and the X9119; either between the host and one of the data registers or directly between the host and the Wiper Counter Register. These instructions are:

- **XFR Data Register to Wiper Counter Register** – This transfers the contents of one specified Data Register to the Wiper Counter Register.
- **XFR Wiper Counter Register to Data Register** – This transfers the contents of the Wiper Counter Register to the specified Data Register.

See Instruction format for more details.

POWER UP AND DOWN REQUIREMENTS

There are no restrictions on the power-up condition of V_{CC} and the voltages applied to the potentiometer pins provided that the V_{CC} is always more positive than or equal to the voltages at R_H , R_L , and R_W , i.e. $V_{CC} \geq R_H, R_L, R_W$. There are no restrictions on the power-down condition. However, the datasheet parameters for the DCP do not apply until 1millisecond after V_{CC} reaches its final value.

Figure 3. Two-Byte Instruction Sequence

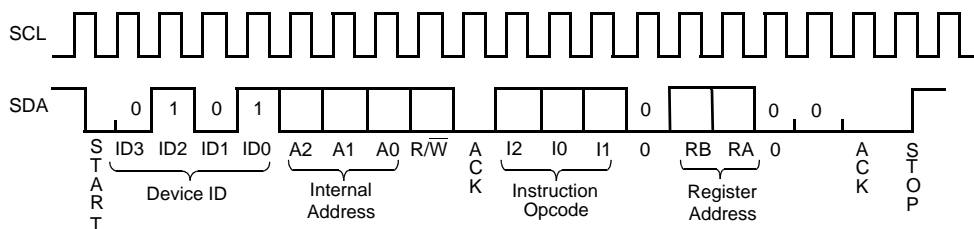
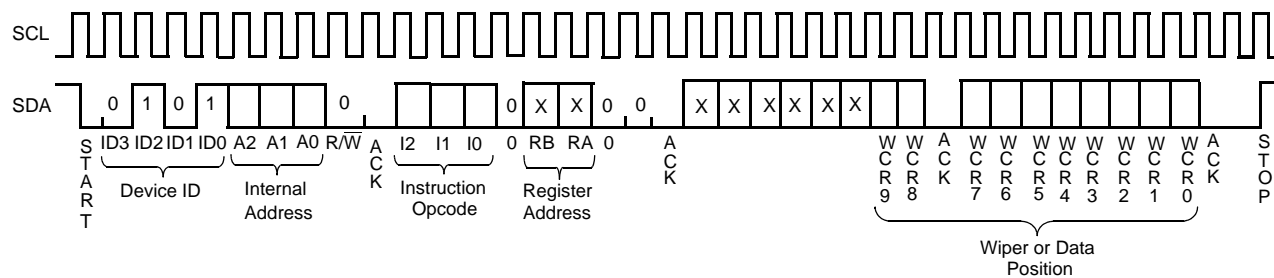


Figure 4. Four-Byte Instruction Sequence (Write or Read for WCR or Data Registers)



INSTRUCTION FORMAT

Read Wiper Counter Register (WCR)

| START | Device Type Identifier | | | | Device Addresses | | | ACK | Instruction Opcode | | | | Register Addresses | | | | ACK | Wiper Position (Sent by Slave on SDA) | | | | | | ACK | Wiper Position (Sent by Slave on SDA) | | | | | | ACK | STOP |
|-------|------------------------|---|---|---|------------------|----|----|---------|--------------------|---|---|---|--------------------|---|---|---|-----|---------------------------------------|---|---|---|---|------|------|---------------------------------------|------|------|------|------|------|------|------|
| | 0 | 1 | 0 | 1 | A2 | A1 | A0 | | R/W = 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | X | X | X | X | X | | X | WCR9 | WCR8 | WCR7 | WCR6 | WCR5 | | |
| | 0 | 1 | 0 | 1 | A2 | A1 | A0 | R/W = 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | X | X | X | WCR9 | WCR8 | WCR7 | WCR6 | WCR5 | WCR4 | WCR3 | WCR2 | WCR1 | WCR0 |

Write Wiper Counter Register (WCR)

| START | Device Type Identifier | | | | Device Addresses | | | ACK | Instruction Opcode | | | | Register Addresses | | | | ACK | Wiper Position (Sent by Master on SDA) | | | | | | ACK | Wiper Position (Sent by Master on SDA) | | | | | | ACK | STOP |
|-------|------------------------|---|---|---|------------------|----|----|---------|--------------------|---|---|---|--------------------|---|---|---|-----|--|---|---|---|---|------|------|--|------|------|------|------|------|------|------|
| | 0 | 1 | 0 | 1 | A2 | A1 | A0 | | R/W = 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | | 0 | X | X | X | X | X | | X | WCR9 | WCR8 | WCR7 | WCR6 | WCR5 | | |
| | 0 | 1 | 0 | 1 | A2 | A1 | A0 | R/W = 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | X | X | X | X | X | X | WCR9 | WCR8 | WCR7 | WCR6 | WCR5 | WCR4 | WCR3 | WCR2 | WCR1 | WCR0 |

Read Data Register (DR)

| START | Device Type Identifier | | | | Device Addresses | | | ACK | Instruction Opcode | | | | Register Addresses | | | | ACK | Wiper Position (Sent by Slave on SDA) | | | | | | ACK | wiper position or data (Sent by Slave on SDA) | | | | | | ACK | STOP |
|-------|------------------------|---|---|---|------------------|----|----|---------|--------------------|---|---|---|--------------------|----|----|---|-----|---------------------------------------|---|---|---|---|------|------|---|------|------|------|------|------|------|------|
| | 0 | 1 | 0 | 1 | A2 | A1 | A0 | | R/W = 1 | 1 | 0 | 1 | 0 | RB | RA | 0 | | 0 | X | X | X | X | X | | X | WCR9 | WCR8 | WCR7 | WCR6 | WCR5 | | |
| | 0 | 1 | 0 | 1 | A2 | A1 | A0 | R/W = 1 | 1 | 0 | 1 | 0 | RB | RA | 0 | 0 | X | X | X | X | X | X | WCR9 | WCR8 | WCR7 | WCR6 | WCR5 | WCR4 | WCR3 | WCR2 | WCR1 | WCR0 |

Write Data Register (DR)

| START | Device Type Identifier | | | | Device Addresses | | | R/W = 0 | SACK | Instruction Opcode | | | | Register Addresses | | | | SACK | Wiper Position or Data (Sent by Master on SDA) | | | | | | SACK | STOP | HIGH-VOLTAGE WRITE CYCLE | | | | | | | | | |
|-------|------------------------|---|---|---|------------------|----|----|---------|------|--------------------|---|---|---|--------------------|----|---|---|------|--|---|---|---|---|------|------|------|--------------------------|------|------|------|------|------|------|------|------|------|
| | 0 | 1 | 0 | 1 | A2 | A1 | A0 | | | 1 | 1 | 0 | 0 | RB | RA | 0 | 0 | | X | X | X | X | X | X | | | | WCR9 | WCR8 | WCR7 | WCR6 | WCR5 | WCR4 | WCR3 | WCR2 | WCR1 |
| | 0 | 1 | 0 | 1 | A2 | A1 | A0 | | | 1 | 1 | 0 | 0 | RB | RA | 0 | 0 | X | X | X | X | X | X | WCR9 | WCR8 | WCR7 | WCR6 | WCR5 | WCR4 | WCR3 | WCR2 | WCR1 | WCR0 | | | |

Transfer Wiper Counter Register (WCR) to Data Register (DR)

| START | Device Type Identifier | | | | Device Addresses | | | R/W = 0 | SACK | Instruction Opcode | | | | Register Addresses | | | | SACK | STOP | HIGH-VOLTAGE WRITE CYCLE |
|-------|------------------------|---|---|---|------------------|----|----|---------|------|--------------------|---|---|---|--------------------|----|---|---|------|------|--------------------------|
| | 0 | 1 | 0 | 1 | A2 | A1 | A0 | | | 1 | 1 | 1 | 0 | RB | RA | 0 | 0 | | | |
| | 0 | 1 | 0 | 1 | A2 | A1 | A0 | | | 1 | 1 | 1 | 0 | RB | RA | 0 | 0 | | | |

Transfer Data Register (DR) to Wiper Counter Register (WCR)

| START | Device Type Identifier | | | | Device Addresses | | | R/W = 1 | SACK | Instruction Opcode | | | | Register Addresses | | | | SACK | STOP |
|-------|------------------------|---|---|---|------------------|----|----|---------|------|--------------------|---|---|---|--------------------|----|---|---|------|------|
| | 0 | 1 | 0 | 1 | A2 | A1 | A0 | | | 1 | 1 | 0 | 0 | RB | RA | 0 | 0 | | |
| | 0 | 1 | 0 | 1 | A2 | A1 | A0 | | | 1 | 1 | 0 | 0 | RB | RA | 0 | 0 | | |

- Notes: (1) "A2 ~ A0": stand for the device addresses sent by the master.
 (2) WCRx refers to wiper position data in the Wiper Counter Register

ABSOLUTE MAXIMUM RATINGS

| | |
|---|-----------------|
| Temperature under bias | -65°C to +135°C |
| Storage temperature | -65°C to +150°C |
| Voltage on SCL, SDA, or any address input with respect to V_{SS} | -1V to +7V |
| $\Delta V = (V_H - V_L) $ | 5V |
| Lead temperature (soldering, 10s) | 300°C |
| I_W (10s) | ±6mA |

RECOMMENDED OPERATING CONDITIONS

| Temp | Min. | Max. |
|------------|-------|-------|
| Commercial | 0°C | +70°C |
| Industrial | -40°C | +85°C |

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Device | Supply Voltage (V_{CC}) Limits ⁽⁴⁾ |
|-----------|---|
| X9118 | 5V ± 10% |
| X9118-2.7 | 2.7V to 5.5V |

ANALOG CHARACTERISTICS (Over recommended industrial (2.7V) operation conditions unless otherwise stated.)

| Symbol | Parameter | Limits | | | | Test Conditions |
|---------------|--|----------|----------|------|-------------------|--|
| | | Min. | Typ. | Max. | Units | |
| R_{TOTAL} | End to End Resistance | | 100 | | k Ω | |
| | End to End Resistance Tolerance | | | ±20 | % | |
| | Power Rating | | | 50 | mW | 25°C, each pot |
| I_W | Wiper Current | | | ±3 | mA | |
| R_W | Wiper Resistance | | 40 | 110 | Ω | Wiper Current = ± 50 μ A, V_{CC} = 5V |
| | | | 150 | 300 | Ω | Wiper Current = ± 50 μ A, V_{CC} = 3V |
| V_{TERM} | Voltage on any R_H or R_L Pin | V_{SS} | | 5 | V | V_{SS} = 0V |
| | Noise | | -120 | | dBV | Ref: 1V |
| | Resolution | | 0.1 | | % | |
| | Absolute Linearity ⁽¹⁾ | | | ±1 | MI ⁽³⁾ | $R_{w(n)(actual)} - R_{w(n)(expected)}$, where n=8 to 1006 |
| | | | ±1.5 | ±2.0 | MI ⁽³⁾ | $R_{w(n)(actual)} - R_{w(n)(expected)}$ ⁽⁵⁾ |
| | Relative Linearity ⁽²⁾ | | | ±0.5 | MI ⁽³⁾ | $R_{w(m+1)} - [R_{w(m)} + MI]$, where m=8 to 1006 |
| | | | ±0.5 | ±1.0 | MI ⁽³⁾ | $R_{w(m+1)} - [R_{w(m)} + MI]$ ⁽⁵⁾ |
| | Temperature Coefficient of R_{TOTAL} | | ±300 | | ppm/°C | |
| | Ratiometric Temp. Coefficient | | | 20 | ppm/°C | |
| $C_H/C_L/C_W$ | Potentiometer Capacitancies | | 10/10/25 | | pF | See Macro model |

- Notes: (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
(2) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
(3) $MI = R_{TOT} / 1023$ or $(R_H - R_L) / 1023$, single pot
(4) n = 0, 1, 2, ..., 1023; m = 0, 1, 2, ..., 1022.
(5) ESD Rating on R_H , R_L , R_W pins is 1.5KV (HBM, 1.0 μ A leakage maximum), ESD rating on all other pins is 2.0kV.

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

| Symbol | Parameter | Limits | | | | Test Conditions |
|------------------|--|-----------------------|------|-----------------------|-------|--|
| | | Min. | Typ. | Max. | Units | |
| I _{CC1} | V _{CC} supply current (active) | | | 3 | mA | f _{SCL} = 400kHz; V _{CC} = +5.5V; SDA = Open; (for 2-wire, Active, Read and Volatile Write States only) |
| I _{CC2} | V _{CC} supply current (nonvolatile write) | | | 5 | mA | f _{SCL} = 400kHz; V _{CC} = +5.5V; SDA = Open; (for 2-wire, Active, Non-volatile Write State only) |
| I _{SB} | V _{CC} current (standby) | | | 3 | μA | V _{CC} = +5.5V; V _{IN} = V _{SS} or V _{CC} ; SDA = V _{CC} ; (for 2-wire, Standby State only) |
| I _{LI} | Input leakage current | | | 10 | μA | V _{IN} = V _{SS} to V _{CC} |
| I _{LO} | Output leakage current | | | 10 | μA | V _{OUT} = V _{SS} to V _{CC} |
| V _{IH} | Input HIGH voltage | V _{CC} x 0.7 | | V _{CC} + 1 | V | |
| V _{IL} | Input LOW voltage | -1 | | V _{CC} x 0.3 | V | |
| V _{OL} | Output LOW voltage | | | 0.4 | V | I _{OL} = 3mA |
| V _{OH} | Output HIGH voltage | | | | | |

ENDURANCE AND DATA RETENTION

| Parameter | Min. | Units |
|-------------------|---------|-----------------------------------|
| Minimum Endurance | 100,000 | Data changes per bit per register |
| Data Retention | 100 | years |

CAPACITANCE

| Symbol | Test | Max. | Units | Test Conditions |
|------------------------------------|--|------|-------|-----------------------|
| C _{IN/OUT} ⁽⁶⁾ | Input/Output capacitance (SI) | 8 | pF | V _{OUT} = 0V |
| C _{IN} ⁽⁶⁾ | Input capacitance (SCL, \overline{WP} , A1 and A0) | 6 | pF | V _{IN} = 0V |

POWER-UP TIMING

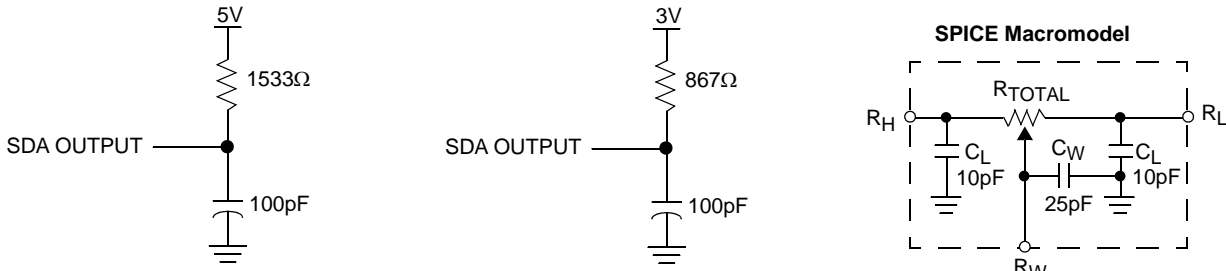
| Symbol | Parameter | Min. | Max. | Units |
|---|---|------|------|-------|
| t _r V _{CC} ⁽⁶⁾ | V _{CC} Power-up Rate | 0.2 | 50 | V/ms |
| t _{PUR} ⁽⁷⁾ | Power-up to Initiation of read operation | | 1 | ms |
| t _{PUW} ⁽⁷⁾ | Power-up to Initiation of write operation | | 50 | ms |

- Notes: (6) This parameter is not 100% tested.
 (7) t_{PUR} and t_{PUW} are the delays required from the time the (last) power supply (V_{CC}) is stable until the specific instruction can be issued. These parameters are not 100% tested.
 (8) This is not a tested or guaranteed parameter and should be used only as a guideline.

A.C. TEST CONDITIONS

| | |
|-------------------------------|--|
| Input pulse levels | $V_{CC} \times 0.1$ to $V_{CC} \times 0.9$ |
| Input rise and fall times | 10ns |
| Input and output timing level | $V_{CC} \times 0.5$ |

EQUIVALENT A.C. LOAD CIRCUIT



AC TIMING HIGH-VOLTAGE WRITE CYCLE TIMING

| Symbol | Parameter | Min. | Max. | Units |
|--------------|---|------|------|-------|
| f_{SCL} | Clock Frequency | | 400 | kHz |
| t_{CYC} | Clock Cycle Time | 2500 | | ns |
| t_{HIGH} | Clock High Time | 600 | | ns |
| t_{LOW} | Clock Low Time | 1300 | | ns |
| $t_{SU:STA}$ | Start Setup Time | 600 | | ns |
| $t_{HD:STA}$ | Start Hold Time | 600 | | ns |
| $t_{SU:STO}$ | Stop Setup Time | 600 | | ns |
| $t_{SU:DAT}$ | SDA Data Input Setup Time | 100 | | ns |
| $t_{HD:DAT}$ | SDA Data Input Hold Time | 0 | | ns |
| t_R | SCL and SDA Rise Time | | 300 | ns |
| t_F | SCL and SDA Fall Time | | 300 | ns |
| t_{AA} | SCL Low to SDA Data Output Valid Time | 250 | | ns |
| t_{DH} | SDA Data Output Hold Time | 0 | | ns |
| T_I | Noise Suppression Time Constant at SCL and SDA inputs | 50 | | ns |
| t_{BUF} | Bus Free Time (Prior to Any Transmission) | 1300 | | ns |
| $t_{SU:WPA}$ | A0, A1, A2 Setup Time | 0 | | ns |
| $t_{HD:WPA}$ | A0, A1, A2 Hold Time | 0 | | ns |

HIGH-VOLTAGE WRITE CYCLE TIMING

| Symbol | Parameter | Typ. | Max. | Units |
|----------|--|------|------|-------|
| t_{WR} | High-voltage write cycle time (store instructions) | 5 | 10 | ms |

XDCP TIMING

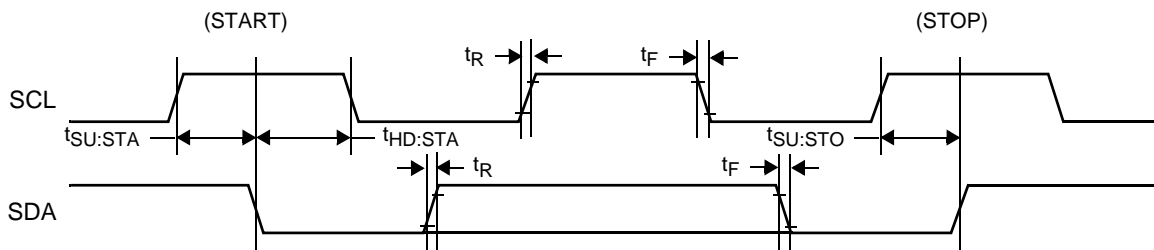
| Symbol | Parameter | Min. | Max. | Units |
|------------|--|------|------|---------|
| t_{WRPO} | Wiper response time after the third (last) power supply is stable | 5 | 10 | μ s |
| t_{WRL} | Wiper response time after instruction issued (all load instructions) | 5 | 10 | μ s |

SYMBOL TABLE

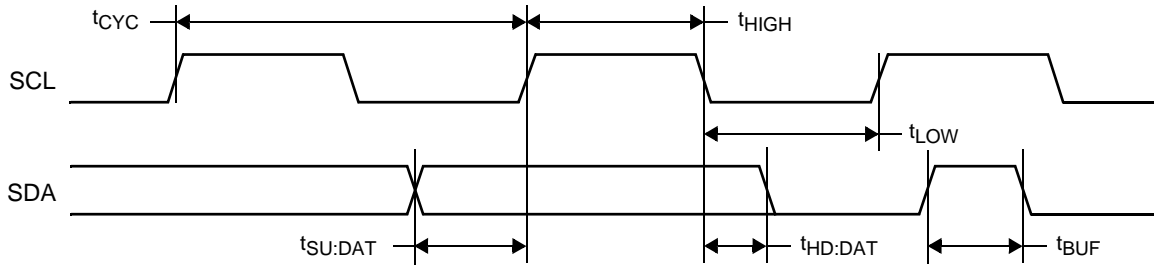
| WAVEFORM | INPUTS | OUTPUTS |
|----------|-----------------------------|-------------------------------|
| | Must be steady | Will be steady |
| | May change from Low to High | Will change from Low to High |
| | May change from High to Low | Will change from High to Low |
| | Don't Care: Changes Allowed | Changing: State Not Known |
| | N/A | Center Line is High Impedance |

TIMING DIAGRAMS

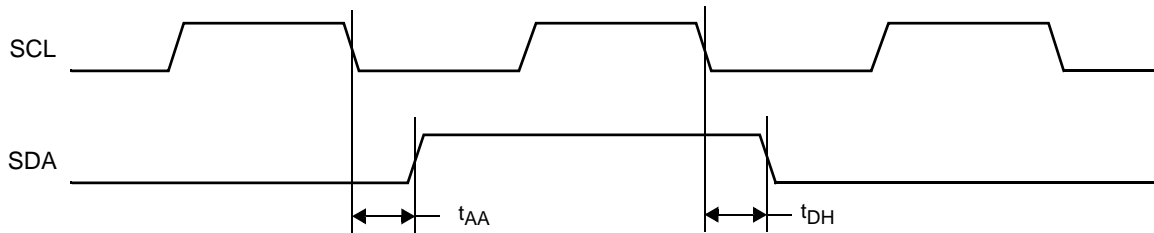
Start and Stop Timing



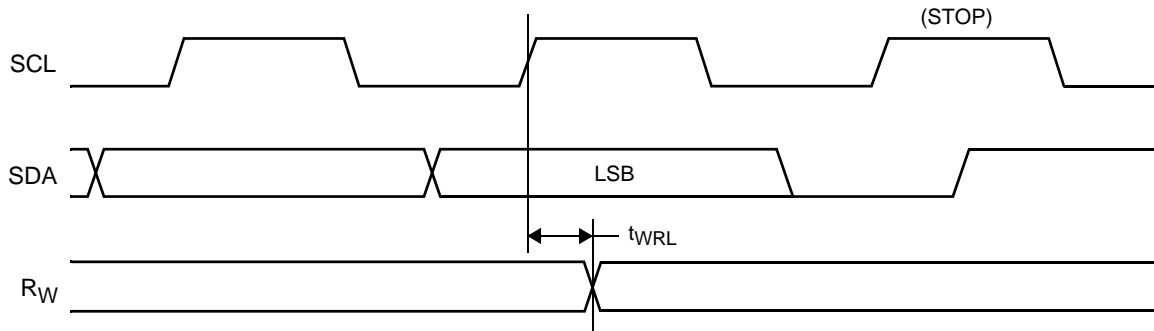
Input Timing



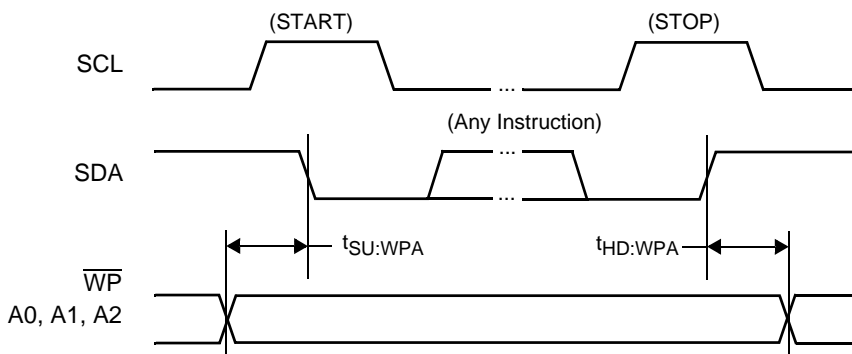
Output Timing



XDCP Timing (for All Load Instructions)

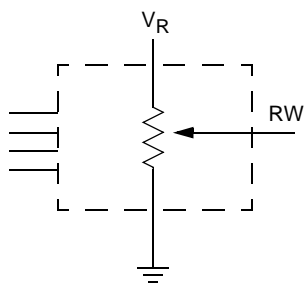


Write Protect and Device Address Pins Timing

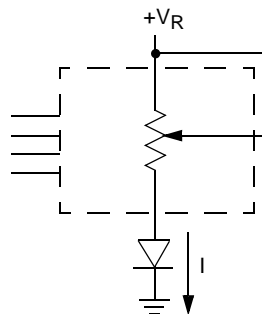


APPLICATIONS INFORMATION

Basic Configurations of Electronic Potentiometers



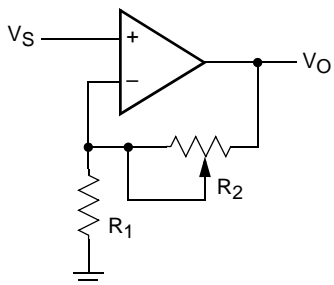
Three terminal Potentiometer;
Variable voltage divider



Two terminal Variable Resistor;
Variable current

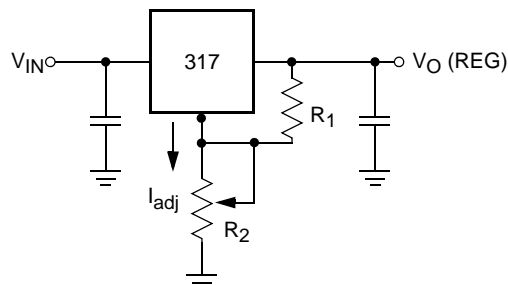
Application Circuits

Noninverting Amplifier



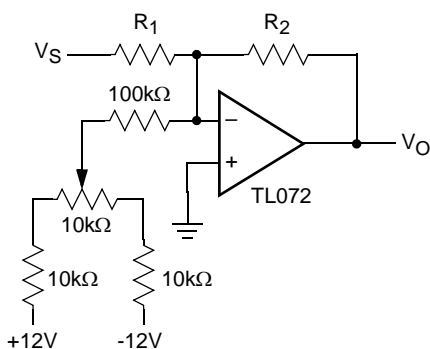
$$V_O = (1 + R_2/R_1)V_S$$

Voltage Regulator

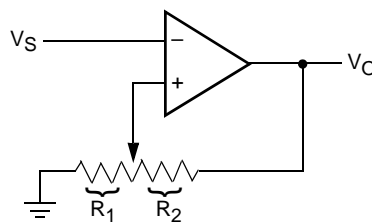


$$V_O (\text{REG}) = 1.25V (1 + R_2/R_1) + I_{\text{adj}} R_2$$

Offset Voltage Adjustment



Comparator with Hysteresis

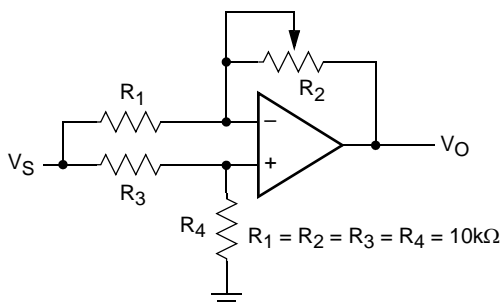


$$V_{UL} = \{R_1/(R_1+R_2)\} V_O(\text{max})$$

$$V_{LL} = \{R_1/(R_1+R_2)\} V_O(\text{min})$$

Application Circuits (Continued)

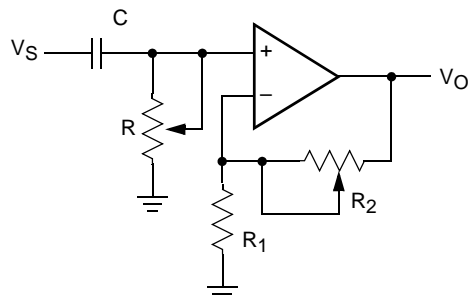
Attenuator



$$V_O = G V_S$$

$$-1/2 \leq G \leq +1/2$$

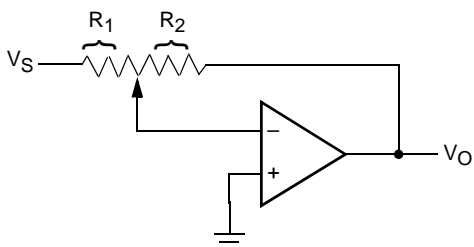
Filter



$$G_O = 1 + R_2/R_1$$

$$f_c = 1/(2\pi RC)$$

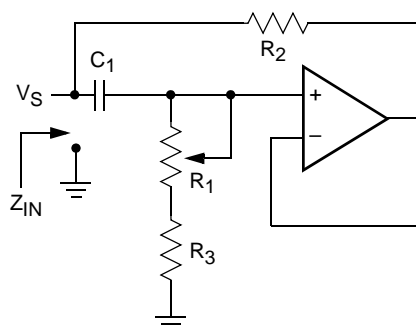
Inverting Amplifier



$$V_O = G V_S$$

$$G = -R_2/R_1$$

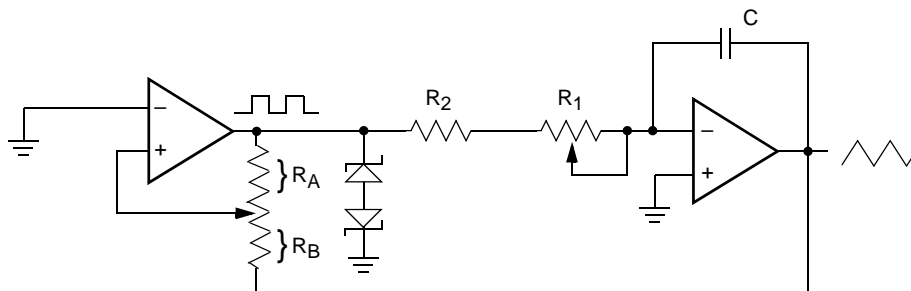
Equivalent L-R Circuit



$$Z_{IN} = R_2 + s R_2 (R_1 + R_3) C_1 = R_2 + s L_{eq}$$

$$(R_1 + R_3) \gg R_2$$

Function Generator

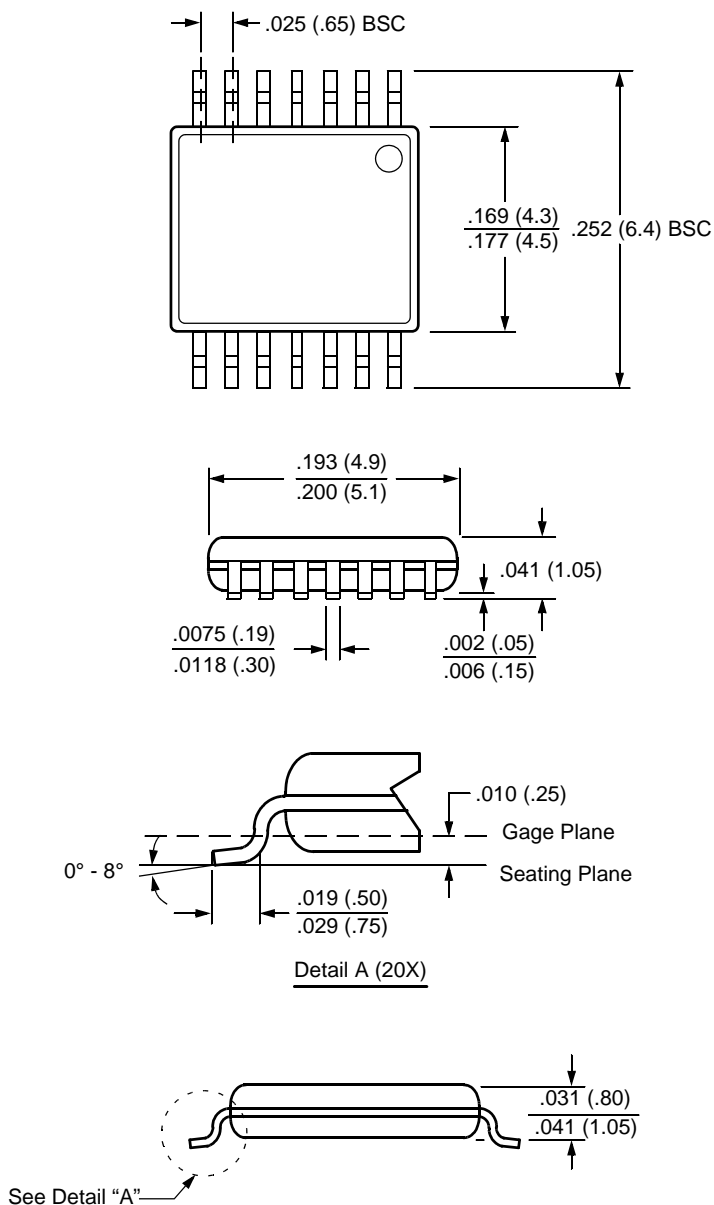


$$\text{frequency} \propto R_1, R_2, C$$

$$\text{amplitude} \propto R_A, R_B$$

PACKAGING INFORMATION

14-Lead Plastic, TSSOP, Package Code V14



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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