Semicustom

CMOS

Standard cell

CS86 Series

■ DESCRIPTION

The CS86 series of 0.18 μ m standard cells is a line of CMOS ASICs based on higher integration implemented by introducing wiring pitch reduction technology and on I/O pad placement technology to the conventional CS81 series.

The CS86 series has three types of cell sets (CS86MN, CS86MZ, and CS86ML), covering a variety of applications, from portable devices requiring low power consumption to image processors requiring large-scale circuitry and high speed. The three types of cell sets can be contained on one chip, allowing those system LSIs to be implemented which require low power consumption as well as high-speed operation for certain types of processing.

■ FEATURES

Technology : 0.18 μm silicon-gate CMOS, 4- to 6-layer wiring

The same chip can therefore incorporate the standard transistor cell and the ultrahigh-

speed or low-leakage process cell together.

• Supply voltage : $+1.8 \text{ V} \pm 0.15 \text{ V}$ (normal) to $+1.1 \text{ V} \pm 0.1 \text{ V}$

• Junction temperature range : -40 °C to +125 °C

Cell set

CS86MN: Offers standard transistor characteristics. Designed as a library for products requiring higher

hroughputs.

CS86MZ: Offers transistor characteristics for ultra high-speed operation. Designed as a library for

products that require higher processing speeds than those provided by CS86MN.

CS86ML: Offers transistor charactersistics with less leak current. Designed as a library for mobile

devices and other products requiring lower power consumption.

• Cell Specifications :

Cell set name	CS86MZ	CS86MN	CS86ML
Delay time*1	70 ps	88 ps	136 ps
Power consumption*2	42.7 nW/MHz	40.1 nW/MHz	38.3 nW/MHz
Leak power*3	3.922 nW	0.023 nW	0.0067 nW

*1 : 2 input NAND cell (low-power type), F/O = 2, normal load, Power supply voltage 1.8 V, Temperature = +25 °C

 *2 : 2 input NAND cell (low-power type) , F/O = 1, 4 Grid, Power supply voltage 1.8 V, Temperature = +25 °C

*3 : 2 input NAND cell (low-power type) , F/O = 0, non load, Power supply voltage 1.8 V, Temperature = +25 °C (Continued)



(Continued)

- Output buffer cells with noise reduction circuits
- Input buffer cells and bidirectional buffer cells with on-chip input pull-up/pull-down resistors
- · Buffer cells for crystal oscillation circuits
- Special interfaces: SSTL2, PCI, P-CML, T-LVTTL, USB 2.0, IEEE1394, and others.
- IP macros : CPU (ARM9, FR-V, and others) , DSP, PCI, IEEE1394, USB 2.0, IrDA, PLL, DAC, ADC, and others.
- Capable of incorporating compiled cells (RAM/ROM/Register file/Delay line)
- · Configurable internal bus circuits
- Advanced hardware/software co-design environment
- Short-term development using Physical Synthesis tool
- Low power consumption using Low Power Synthesis tool
- Short-term development using a timing driven layout tool
- Hierarchical design environment for supporting large-scale circuits
- Support for Signal-Integrity
- Support for Memory (RAM, ROM) SCAN
- Support for Memory (RAM) BIST
- Support for Boundary SCAN
- Support for path delay test
- A variety of package options : QFP, TQFP, LQFP, HQFP, PBGA, FBGA, FLGA, EBGA

■ MACRO LIBRARY (Including macros being prepared)

1. Logic cells

AdderAND-ORAND-OR InverterDecoder

• Clock Buffer • NON-Scan Flip Flop

LatchNANDBuffer

• AND • OR-AND Inverter

• NOR • OR

OR-AND
 Scan Flip Flop
 ENOR
 Delay Buffer
 Selector
 EOR

• Boundary Scan Register • Dummy Clock Buffer

• Bus Driver • Others

2. IP macro

CPU	FR-V, ARM9, and others.
DSP	Communications DSP, DSP for Digital AV, and others.
Peripheral Macro	Interval timer, Interruption controller, DMA controller, RTC, Calender, UART, and others.
Interface macro	PCI, IEEE1394, USB 2.0, IrDA, and others.
Multimedia processing macros	JPEG, MPEG 4.0, and others.
Mixed signal macros	ADC, DAC, OPAMP, and others.
Compiled macros	RAM (1 port, 2 port), ROM, Delay Line, Register file, and others.
PLL	Analog PLL
I/O macro	Compatible with various interface levels between 1.1 V and 5 V; SSTL2, PCI, P-CML, T-LVTTL, USB, IEEE1394, and others.

■ COMPILED CELLS

Compiled cells are macro cells which are automatically generated with the bit/word configuration specified. The CS86 series has the following types of compiled cells. (Note that each macro is different in word/bit range depending on the column type.)

1. Clock synchronous single-port RAM (1 address : 1 RW)

High density type/High density partial write type

Column type	Memory capacity	Word range	Bit range	Unit
4	16 to 72 K	16 to 1 K	1 to 72	bit
16	64 to 72 K	64 to 4 K	1 to 18	bit

• Super high density type/Super high density partial write type

Column type	Memory capacity	Word range	Bit range	Unit
4	64 to 144 K	32 to 2 K	2 to 72	bit

Large scale partial write type

Column type	Memory capacity	Word range	Bit range	Unit
16	24 to 1152 K	4K to 16 K	6 to 72	bit

• Super high density large scale partial write type

Column type	Memory capacity	Word range	Bit range	Unit
16	2 to 1152 K	512 to 16 K	4 to 72	bit

High speed type

Column type	Memory capacity	Word range	Bit range	Unit
8	256 to 144 K	64 to 2 K	4 to 72	bit

2. Clock synchronous dual-port RAM (2 addresses : 1 RW, 1 R)

High density type/Partial write type

Column type	Memory capacity	Word range	Bit range	Unit
4	16 to 72 K	16 to 1 K	1 to 72	bit
16	64 to 72 K	64 to 4 K	1 to 18	bit

3. Clock synchronous register file (3 addresses : 1 W, 2 R)

Column type	Memory capacity	Word range	Bit range	Unit
1	4 to 4608	4 to 64	1 to 72	bit

4. Clock synchronous register file (4 addresses : 2 W, 2 R)

Column type	Memory capacity	Word range	Bit range	Unit
1	4 to 4608	4 to 64	1 to 72	bit

5. Clock synchronous ROM (1 addresses: 1 R)

Column type	Memory capacity	Word range	Bit range	Unit
16	256 to 1024 K	128 to 8 K	2 to 128	bit
64	1 to 1024 K	512 to 32 K	2 to 32	bit

6. Clock synchronous delay line memory (2 addresses : 1 W, 1 R)

Column type	Memory capacity	Word range	Bit range	Unit
8	256 to 32 K	32 to 1 K	8 to 32	bit
16	384 to 32 K	64 to 2 K	6 to 16	bit
32	512 to 32 K	128 to 4 K	4 to 8	bit

■ ABSOLUTE MAXIMUM RATINGS

(Vss = 0 V)

Donomoton	Comple ed	Rat	Rating		
Parameter	Symbol	Min	Max	Unit	
Cupply voltage	V_{DD}	- 0.5	2.5 *1	V	
Supply voltage	טט v	- 0.5	4.0 *2	V	
Input voltage	Vı	- 0.5	$V_{DD}+0.5 \ (\le 2.5 \ V)^{*1}$	V	
Input voltage	VI	- 0.5	$V_{DD}+0.5 (\le 4.0 \text{ V}) *2$	V	
Output voltage	Vo	- 0.5	$V_{DD}+0.5 \ (\le 2.5 \ V)^{*1}$	V	
Output voltage	VO	- 0.5	$V_{DD}+0.5 (\le 4.0 \text{ V}) *2$		
Storage temperature	Tst	- 55	+125	°C	
Junction temperature	Tj	-40	+125	°C	
Output current*3	lo	±10 (3.3 VCMO	S, 2.5 VCMOS)	mA	
Output current s	Ю	± 7.5 (1.8 VCMOS)			
Input signal transmitting rate	Rı	_	Clock input*4 : 200 Normal input : 100	Mbps*5	
Output signal transmitting rate	Ro	_	100	Mbps*5	
Output load capacitance	Со	_	3000/Ro	pF	
Supply pin current	lσ	See "• Supply pin current f	or one VDD/GND pin (mA) "	mA	

^{*1 :} Internal gate part in case of single power supply or dual power supply

• Supply pin current value for one VDD/GND pin (mA)

(a) Maximum current for one I/O*1

 $T_i = +125 \, {}^{\circ}C^{*2}$

Frame	Source type	Maximum current (at standard source) (mA)	Number of layers
	V _{DDE}	68	4
	V _{DDE}	59	5
YH	V _{DDE}	59	6
	V _{DDI} , V _{DD} , V _{SS}	68	4
	V _{DDI} , V _{DD} , V _{SS}	93	5
	V _{DDI} , V _{DD} , V _{SS}	118	6

^{*2 :} I/O part in case 3.3 V I/F or 2.5 V I/F is used by dual power supply.

^{*3 :} DC current which continues more than 10 ms, or average DC current

^{*4 :} in case of I/O cell for clock input

^{*5 :} bps = bit per second

(b) Current value that one I/O can provide to the core

$$T_j = +125^{\circ}C^{*2}$$

Frame	Source type	Maximum current (at standard source) (mA)	Number of layers
	Vddi, Vdd, Vss	34	4
YH	Vddi, Vdd, Vss	34	5
	Vddi, Vdd, Vss	59	6

- *1 : Maximum current for one I/O includes the supply current to the I/O part and the core part.
- *2: The current values change according to the junction temperature. When the junction temperature is not +125°C, multiply the value by the following coefficients.

 $Tj = +111^{\circ}C \text{ to } +125^{\circ}C : 1.0$ $Tj = +91^{\circ}C \text{ to } +110^{\circ}C : 1.4$ $Tj = +90^{\circ}C : 2.8$

Note: How to calculate the number of required supply pins

In case of a frame with 6-layer wiring (2 power supplies)

- Maximum current for one VDD/GND pin
- $V_{DDE} = 59$ mA/pin calucurated using the value in "(a) Maximum supply pin current for one I/O" $V_{DDI} = V_{SS} = 59$ mA/pin calucurated using the value in "(b) Current value that one I/O can provide to the core"
- Needed supply pin count (internal power supply/external power supply/Vss): Ni/Ne/Ns
 DC internal maximum power-supply current: limax, DC external maximum power-supply current: lemax
 Ni = limax/59mA, Ne = lemax/59mA, Ns = limax/59mA + lemax/59mA

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

• Single power supply ($V_{DD} = 1.8 \text{ V} \pm 0.15 \text{ V}$)

(Vss = 0 V)

Parameter	Symbol		- Unit		
Farameter	Symbol	Min	Тур	Max	Onit
Supply voltage	V _{DD}	1.65	1.8	1.95	V
"H" level input voltage	VIH	$V_{DD} \times 0.65$	_	V _{DD} + 0.3	V
"L" level input voltage	Vıl	-0.3	_	$V_{DD} \times 0.35$	V
Junction temperature	Tj	-40		+125	°C

• **Dual power supply** ($V_{DDE} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{DDI} = 1.8 \text{ V} \pm 0.15 \text{ V}/V_{DDI} = 1.5 \text{ V} \pm 0.1 \text{ V}/V_{DDI} = 1.1 \text{ V} \pm 0.1 \text{ V}^*$) ($V_{SS} = 0 \text{ V}$)

Parameter		Symbol			Unit	
Faia	meter	Syllibol	Min	Тур	Max	Onit
		V _{DDE}	3.0	3.3	3.6	
Supply voltage			1.65	1.8	1.95	V
Supply voltage	Supply voltage		1.4	1.5	1.6	
			1.0	1.1	1.2	
"H" level input voltage	1.8 V CMOS	Vih	$V_{DDI} imes 0.65$		V _{DDI} + 0.3	V
n leverinput voltage	3.3 V CMOS	VIH	2.0		VDDE + 0.3	V
"I " lovel input veltage	1.8 V CMOS	VIL	-0.3		$V_{DDI} imes 0.35$	V
"L" level input voltage	3.3 V CMOS	VIL	-0.3	_	0.8	V
Junction temperature		Tj	-40	_	+125	°C

^{* :} $V_{DDI} = 1.1 \text{ V} \pm 0.1 \text{ V}$ is being prepared.

• Dual power supply ($V_{DDE} = 2.5 \text{ V} \pm 0.2 \text{ V}$, $V_{DDI} = 1.8 \text{ V} \pm 0.15 \text{ V/V}$ $V_{DDI} = 1.5 \text{ V} \pm 0.1 \text{ V/V}$ $V_{DDI} = 1.1 \text{ V} \pm 0.1 \text{ V}$ $V_{DDI} = 1.1 \text{ V} \pm 0.1 \text{ V}$ $V_{DDI} = 1.1 \text{ V} \pm 0.1 \text{ V}$

Parameter		Symbol		Unit		
Faiai	netei	Syllibol	Min	Тур	Max	Oille
		V _{DDE}	2.3	2.5	2.7	
Supply voltage			1.65	1.8	1.95	V
Supply voltage		V _{DDI}	1.4	1.5	1.6	·
			1.0	1.1	1.2	
"H" level input voltage	1.8 V CMOS	ViH	$V_{DDI} imes 0.65$		V _{DDI} + 0.3	V
Tr lever input voltage	2.5 V CMOS	VIH	1.7	_	V _{DDE} + 0.3	V
"L" level input voltage	1.8 V CMOS	VIL	-0.3		$V_{DDI} imes 0.35$	V
L level iliput voltage	2.5 V CMOS	VIL	-0.3		0.7	V
Junction temperature		Tj	-40		+125	°C

^{* :} $V_{DDI} = 1.1 \text{ V} \pm 0.1 \text{ V}$ is being prepared.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC characteristics

• Single power supply : V_{DD} = 1.8 V standard

 $(V_{DD} = 1.8 \text{ V} \pm 0.15 \text{ V}, \text{ Vss} = 0 \text{ V}, \text{ T}_{j} = -40 \,^{\circ}\text{C to} + 125 \,^{\circ}\text{C})$

Parameter	Symbol	Conditions		Value		
raiailletei	Symbol	Conditions	Min	Тур	Max	Unit
"H" level output voltage	Vон	Іон = –100 μΑ	V _{DD} -0.2	_	V _{DD}	V
"L" level output voltage	Vol	Ιοι = 100 μΑ	0	_	0.2	V
"H" level output V-I characteristics	_	1.8 V V _{DD} = 1.8 V±0.15 V		*		_
"L" level output V-I characteristics	_	1.8 V V _{DD} = 1.8 V±0.15 V		*		_
Input leakage current	l.	_	_		±5	μΑ
Pull up/Pull down resistance	R₽	Pull up $V_{IL} = 0$, Pull down $V_{IH} = V_{DD}$	8	18	40	kΩ

^{*:} Refer to "(1) 1.8 V" in ■V-I CHARACTERISTICS.

• Dual power supply : $V_{DDE} = 3.3 \text{ V}, V_{DDI} = 1.8 \text{ V}/1.5 \text{ V}/1.1 \text{ V}$ $(V_{DDE} = 3.3 \text{ V} \pm 0.3 \text{ V}/V_{DDI} = 1.8 \text{ V} \pm 0.15 \text{ V}, V_{DDI} = 1.5 \text{ V} \pm 0.1 \text{ V}, V_{DDI} = 1.1 \text{ V} \pm 0.1 \text{ V}, V_{DDI} = 1$

Donomoton	Comple of	Conditions		Value		I Incia
Parameter	Symbol	Conditions	Min	Тур	Max	Unit
"L" lovel output voltage	V _{OH4}	3.3 V Output Io _H = -100 μA	VDDE-0.2		V _{DDE}	V
"H" level output voltage	V _{OH2}	1.8 V Output Ioн = -100 μA	V _{DDI} -0.2	_	V _{DDI}] V
"I " lovel output voltege	V _{OL4}	3.3 V Output IoL = 100 μA	0	_	0.2	V
"L" level output voltage	V _{OL2}	1.8 V Output IoL = 100 μA	0		0.2] V
"H" level output V-I		3.3 V VDDE = 3.3 V±0.3 V		*1		
characteristics	_	1.8 V VDDI = 1.8 V±0.15 V		*2		
"L" level output V-I		3.3 V VDDE = 3.3 V±0.3 V		*1		
characteristics	_	1.8 V VDDI = 1.8 V±0.15 V		*2		
Input leakage current	IL	_	_	_	±5	μΑ
Pull up/Pull down	R₽	3.3 V Pull up V _{IL} = 0, Pull down V _{IH} = V _{DDI}	10	33	80	- kΩ
resistance	KP	1.8 V Pull up V _{IL} = 0, Pull down V _{IH} = V _{DDI}	8	18	40	- K22

^{*1 :} Refer to " (2) 3.3 V" in ■V-I CHARACTERISTICS.

^{*2 :} Refer to " (1) 1.8 V" in ■V-I CHARACTERISTICS.

• Dual power supply : $V_{DDE} = 2.5 \text{ V}, V_{DDI} = 1.8 \text{ V}/1.5 \text{ V}/1.1 \text{ V}$ $(V_{DDE} = 2.5 \text{ V} \pm 0.2 \text{ V}, V_{DDI} = 1.8 \text{ V} \pm 0.15 \text{ V}/V_{DDI} = 1.5 \text{ V} \pm 0.1 \text{ V}/V_{DDI} = 1.1 \text{ V} \pm 0.1 \text{ V}, V_{SS} = 0 \text{ V}, T_j = -40 \text{ °C to } +125 \text{ °C})$

Dorometer	Symbol	Conditions		Value		l lni4
Parameter	Symbol	Conditions	Min	Тур	Max	Unit
"L" lovel output voltage	Vонз	2.5 V Output Ioн = -100 μA	VDDE-0.2		V _{DDE}	V
"H" level output voltage	V _{OH2}	1.8 V Output Ioн = -100 μA	V _{DDI} -0.2		V _{DDI}	- V
"I " lovel output voltoge	V _{OL3}	2.5 V Output IoL = 100 μA	0		0.2	V
"L" level output voltage	V _{OL2}	1.8 V Output IoL = 100 μA	0	_	0.2	_ v
"H" level output V-I		2.5 V VDDE = 2.5 V±0.2 V			•	
characteristics	_	1.8 V VDDI = 1.8 V±0.15 V		*		
"L" level output V-I		2.5 V VDDE = 2.5 V±0.2 V		_		
characteristics	_	1.8 V VDDI = 1.8 V±0.15 V		*		
Input leakage current	lι	_	_		±5	μΑ
Pull up/Pull down	R₽	2.5 V Pull up V _{IL} = 0, Pull down V _{IH} = V _{DDE}	_	25	_	- kΩ
resistance	KP	1.8 V Pull up V _{IL} = 0, Pull down V _{IH} = V _{DDI}	8	18	40	- KS2

^{* :} Refer to " (1) 1.8 V" in ■V-I CHARACTERISTICS.

2. AC CHARACTERISTICS

 $V_{SS} = 0 \text{ V}, T_j = -40 \,^{\circ}\text{C} \text{ to } +125 \,^{\circ}\text{C}.$ (Standard specification)

Parameter	Symbol		Value		Unit
Farameter	er Symbol Min Typ		Max	Offic	
Delay time	t _{pd} *1	typ*2 × tmin*3	typ*2 × ttyp*3	typ*2 × tmax*3	ns

^{*1 :} Delay time = propagation delay time, enable time, disable time.

^{*3:} Measurement conditions

Measurement condition	tmin	ttyp	tmax
$V_{DD} = 1.8 \text{ V} \pm 0.15 \text{ V}, \text{ Vss} = 0 \text{ V}, \text{ T}_{j} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	0.62	1.00	1.88
$V_{DD} = 1.5 \text{ V} \pm 0.10 \text{ V}, \text{ Vss} = 0 \text{ V}, \text{ T}_{j} = -40 ^{\circ}\text{C to } +125 ^{\circ}\text{C}$	0.76	1.25	2.42
$V_{DD} = 1.1~V \pm 0.1~V,~V_{SS} = 0~V,~T_{j} = -40~^{\circ}C~to~+125~^{\circ}C$	1.08	2.14	6.22

Note: AC characteristics are determined based on junction temperature, voltage conditions, and process variation.

^{*2: &}quot;typ" is calculated based on the cell specifications.

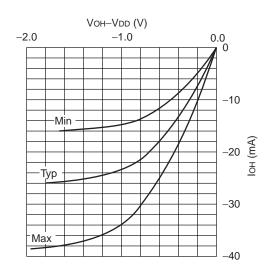
■ V - I CHARACTERISTICS

(1) 1.8 V

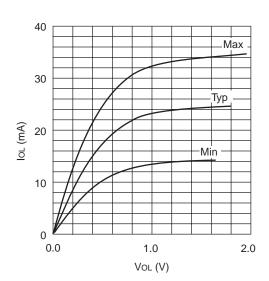
Conditions

Min : Process = Slow, $T_j = +125$ °C, $V_{DD} = 1.65$ V Typ : Process = Typical, $T_j = +25$ °C, $V_{DD} = 1.80$ V

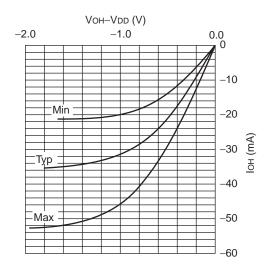
Max : Process = Fast, $T_i = -40$ °C, $V_{DD} = 1.95$ V



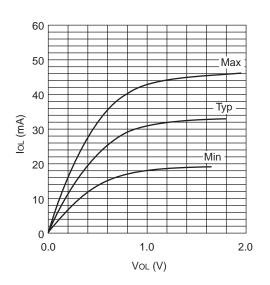
1.8 V CMOS "H" level output (L, M type)



1.8 V CMOS "L" level output (L, M type)



1.8 V CMOS "H" level output (H, V type)

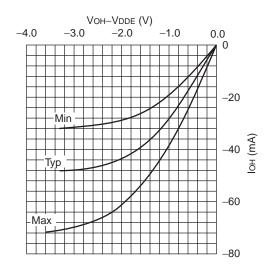


1.8 V CMOS "L" level output (H, V type)

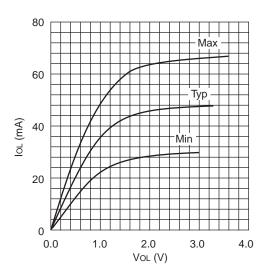
(2) 3.3 V

Conditions

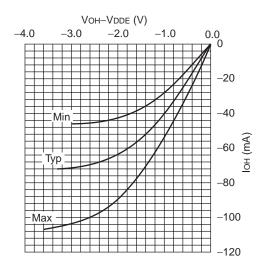
Min : Process = Slow, $T_j = +125$ °C, $V_{DDE} = 3.0$ V Typ : Process = Typical, $T_j = +25$ °C, $V_{DDE} = 3.3$ V Max : Process = Fast, $T_j = -40$ °C, $V_{DDE} = 3.6$ V



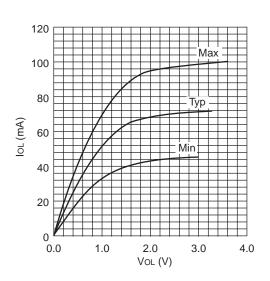
3.3 V CMOS "H" level output (L, M type)



3.3 V CMOS "L" level output (L, M type)



3.3 V CMOS "H" level output (H, V type)



3.3 V CMOS "L" level output (H, V type)

■ INPUT/OUTPUT PIN CAPACITANCE

 $(T_j = +25 \, {}^{\circ}C, \, V_{DD} = VI = 0 \, V, \, f = 1 \, MHz)$

	Parameter Symbol		Requirements	Unit
Input pin	_	CIN	Max 16	pF
Output pin	L, M, H, V type	COUT	Max 16	pF
I/O pin	L, M, H, V type	CI/O	Max 16	pF

Note: Capacitance varies according to the package and the location of the pin.

■ DESIGN METHOD

The integrated standard-cell design environment, SCCAD2, provided for conventional models now supports the CS86 series. This allows you to design ASICs that operate at up to 500 MHz with up to 40 million gates and to halve the layout design period. The Fujitsu's tool GLOSCAD also supports the satandard cell design for CS86 series.

Physical Synthesis

Physical Synthesis tool support is provided on a consulting business basis. A conventional style of ASIC development has a problem that iterations between logic synthesis and layout processing are caused by wiring congestion and the difference between actual and estimated wiring capacities. Supporting logic synthesis based on physical information reduces such iterations and contributes to convergence of ASIC design within the scheduled development period.

Low Power Synthesis

The Low Power Synthesis tool is supported, which enables the use of gated clock buffers of hard macro type incorporating sequential cells, such as latches. The use of gated clock buffers of hard macro type provides low power consumption by the clock line. It also provides reliable operation, reduction in script complexity, and shorter turnaround time (TAT) for processing.

Timing Driven Layout

Performing automatic placement and wiring based on chip-level timing constraints. This prevents post-layout timing problems from developing, which are prominent in particular in the field of deep submicron designs. In addition, all of remaining timing errors are automatically corrected by the Fujitsu's automatic timing correction system. This shortens the development time from the end of creating a net list to the beginning of the prototyping stage.

Hierarchical Design

A top-down hierarchical design approach is taken consistently from logic design to physical design to support larger-scale circuit integration based on deep submicron designing. This enables multiple blocks to be designed logically and physically at the same time and timing convergence to be attained in a short period, providing a design environment capable of easily supporting ultra-large-scale integration of circuits.

Support for Signal Integrity

Automated power wiring enables layout satisfying the design specifications within a short period.

The power width automatic adjustment function designed taking account of internal power consumption and clock frequencies can produce chips satisfying the current density and voltage drop restrictions without human intervention. Also, a verification system is prepared to check the signal noise or delay penalty owing to capacitive coupling between signal conductors and the voltage drop caused by simultaneous local switching.

■ PACKAGES

Package	Pin count	Material
QFP	176, 208, 240	Plastic
TQFP	100, 120	Plastic
LQFP	144, 176, 208, 256	Plastic
HQFP	208, 240, 256, 304	Plastic
PBGA	256, 352, 420	Plastic
FBGA	112, 144, 168, 176, 192, 224, 240, 272, 288, 304, 368	Plastic
FLGA	144, 176, 208, 224, 288	Plastic
EBGA	660	Plastic

Note: Consult Fujitsu for the combination of each package and the time of availability.

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