The RF MOSFET Line

RF Power Field Effect Transistors

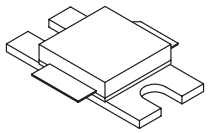
N–Channel Enhancement–Mode Lateral MOSFETs

MRF21030R3
MRF21030SR3

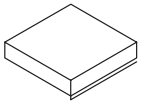
2.2 GHz, 30 W, 28 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for PCN and PCS base station applications with frequencies from 2.0 to 2.2 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN–PCS/cellular radio and WLL applications.

- Wideband CDMA Performance: –45 dB ACPR @ 4.096 MHz, 28 Volts
  Output Power — 3.5 Watts
  Power Gain — 14 dB
  Efficiency — 15%
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2.11 GHz, 30 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.



CASE 465E–03, STYLE 1
NI–400
MRF21030R3



CASE 465F–03, STYLE 1
NI–400S
MRF21030SR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	–0.5, +15	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	83.3 0.48	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

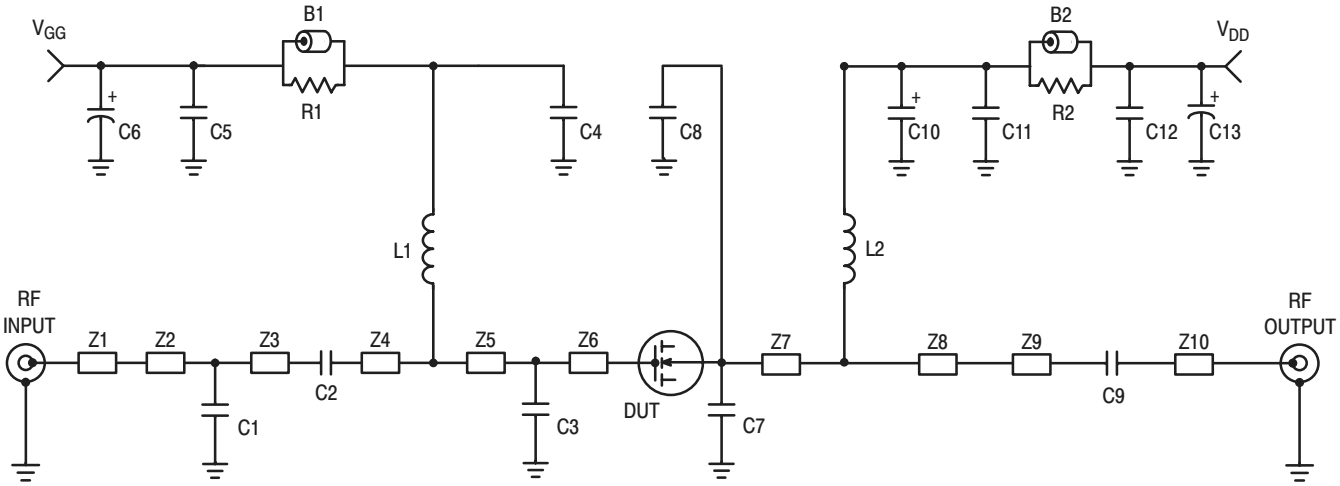
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 20 μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 250 mA)	$V_{GS(Q)}$	2	3.3	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.29	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1 Adc)	g_{fs}	—	2	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (Including Input Matching Capacitor in Package) (1) (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	98.5	—	pF
Output Capacitance (1) (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	37	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	1.3	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 2140.0 MHz, f2 = 2140.1 MHz)	G_{ps}	—	13	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 2140.0 MHz, f2 = 2140.1 MHz)	η	—	33	—	%
3rd Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 2140.0 MHz, f2 = 2140.1 MHz)	IMD	—	–30	—	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 2140.0 MHz, f2 = 2140.1 MHz)	IRL	—	–13	—	dB
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz and f1 = 2170.0 MHz, f2 = 2170.1 MHz)	G_{ps}	12	13	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz and f1 = 2170.0 MHz, f2 = 2170.1 MHz)	η	31	33	—	%
3rd Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz and f1 = 2170.0 MHz, f2 = 2170.1 MHz)	IMD	—	–30	–27.5	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 30 W PEP, I_{DQ} = 250 mA, f1 = 2110.0 MHz, f2 = 2110.1 MHz and f1 = 2170.0 MHz, f2 = 2170.1 MHz)	IRL	—	–13	–9	dB
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 30 W CW, I_{DQ} = 250 mA, f = 2110 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B1, B2	Short Ferrite Beads	Z1	0.153″ x 0.087″ Microstrip
C1	1 pF Chip Capacitor	Z2	0.509″ x 0.156″ Microstrip
C2	4.7 pF Chip Capacitor	Z3	0.572″ x 0.087″ Microstrip
C3	0.5 pF Chip Capacitor	Z4	0.509″ x 0.232″ Microstrip
C4	3.9 pF Chip Capacitor	Z5	0.277″ x 0.143″ Microstrip
C5, C12	0.1 μF Chip Capacitors	Z6	0.200″ x 0.305″ Microstrip
C6, C13	470 μF, 63 V Electrolytic Chip Capacitors	Z7	0.200″ x 0.511″ Microstrip
C7, C8	0.3 pF Chip Capacitors	Z8	0.510″ x 0.328″ Microstrip
C9	3.6 pF Chip Capacitor	Z9	0.608″ x 0.081″ Microstrip
C10	22 μF Tantalum Chip Capacitor	Board	0.030″ Glass Teflon®, TLX8-0300
C11	5.1 pF Chip Capacitor		Taconix (ε_r = 2.55)
L1, L2	12.5 nH Inductors		
R1, R2	12 Ω Chip Resistors (1206)		

Figure 1. MRF21030 Test Circuit Schematic

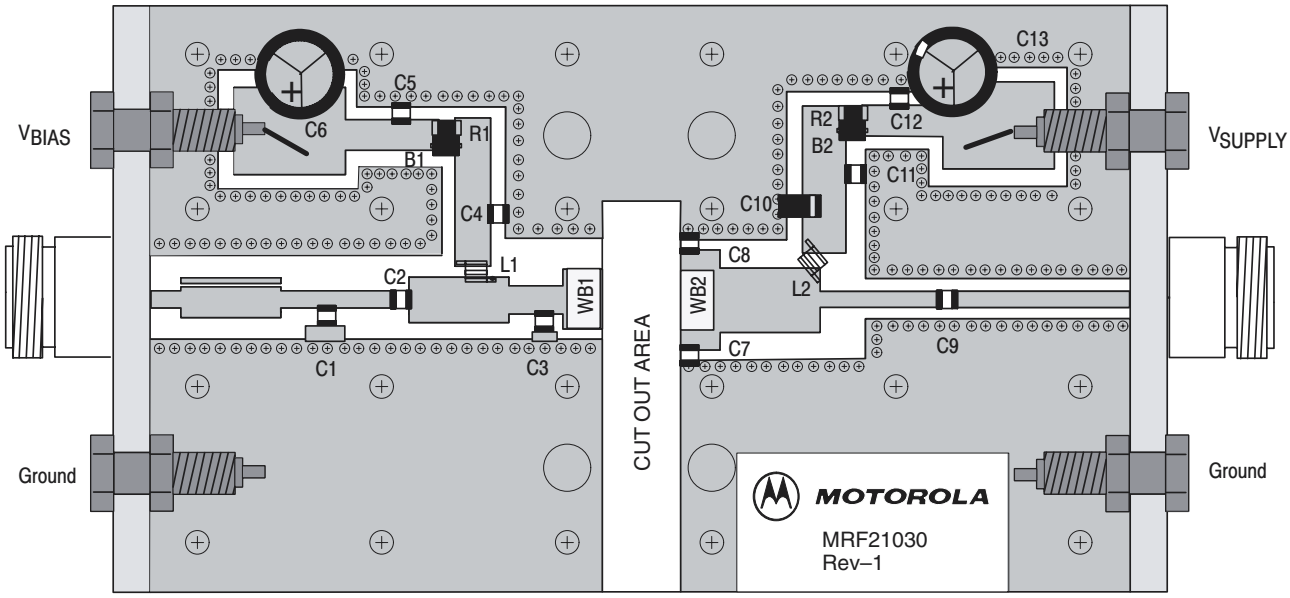


Figure 2. MRF21030 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

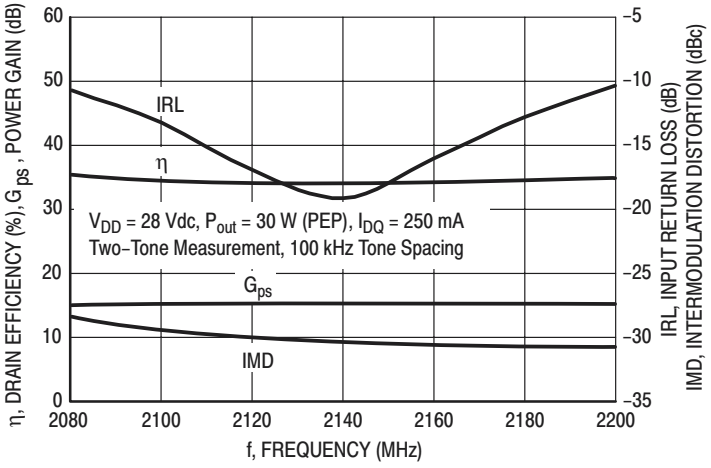


Figure 3. Class AB Broadband Circuit Performance

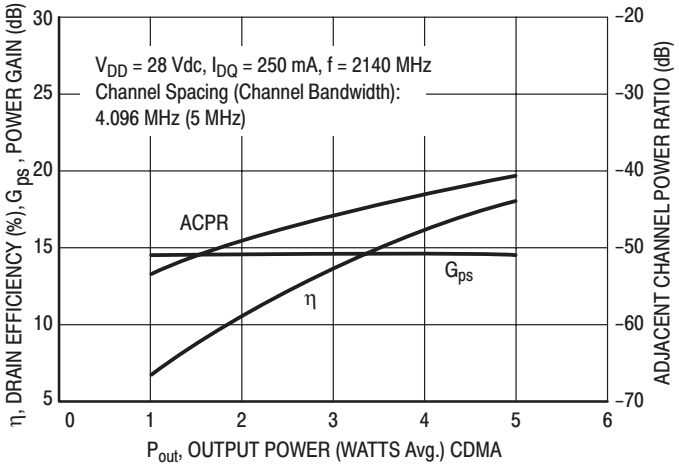


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

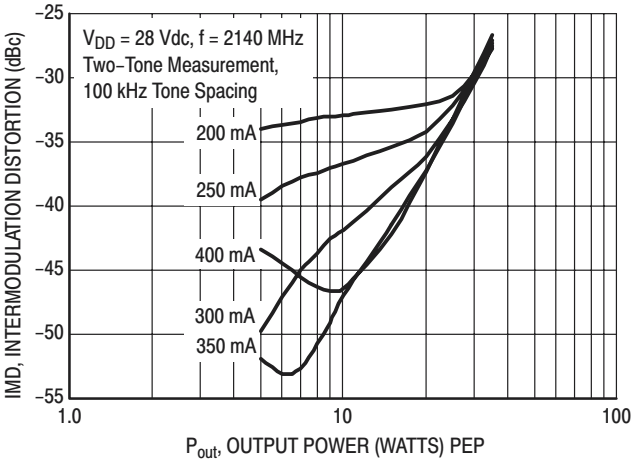


Figure 5. Intermodulation Distortion versus Output Power

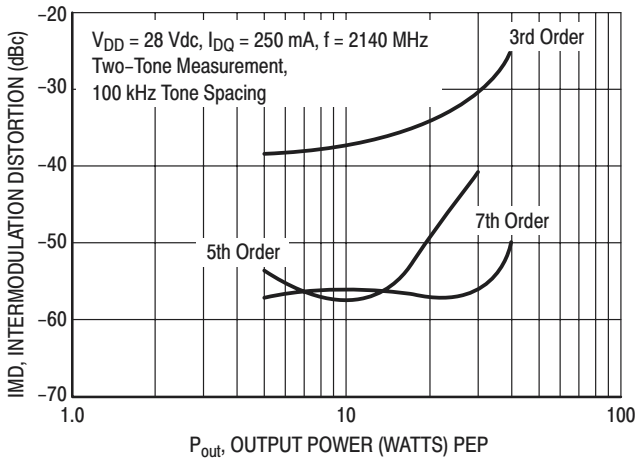


Figure 6. Intermodulation Distortion Products versus Output Power

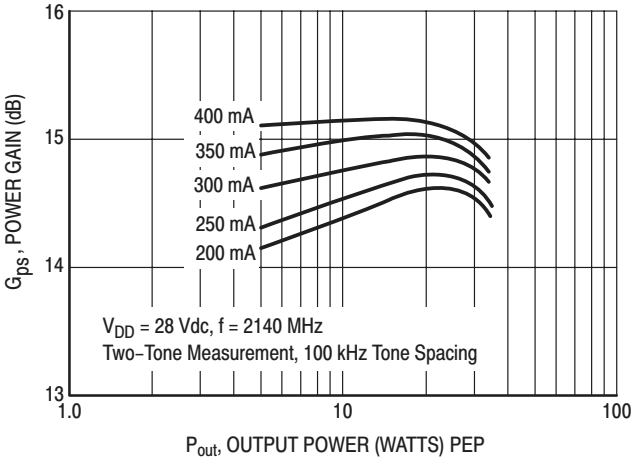


Figure 7. Power Gain versus Output Power

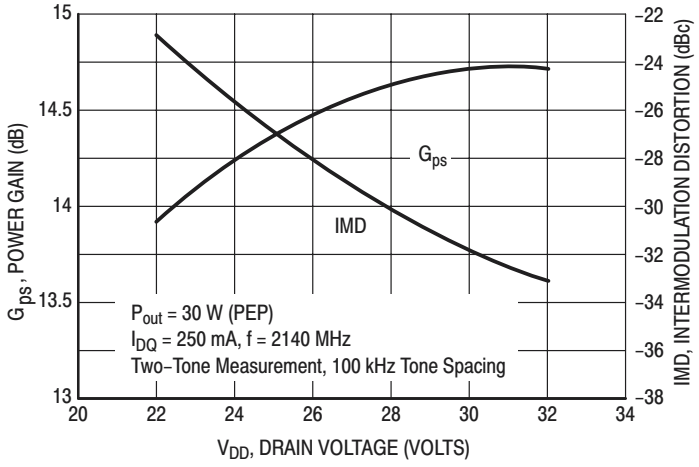
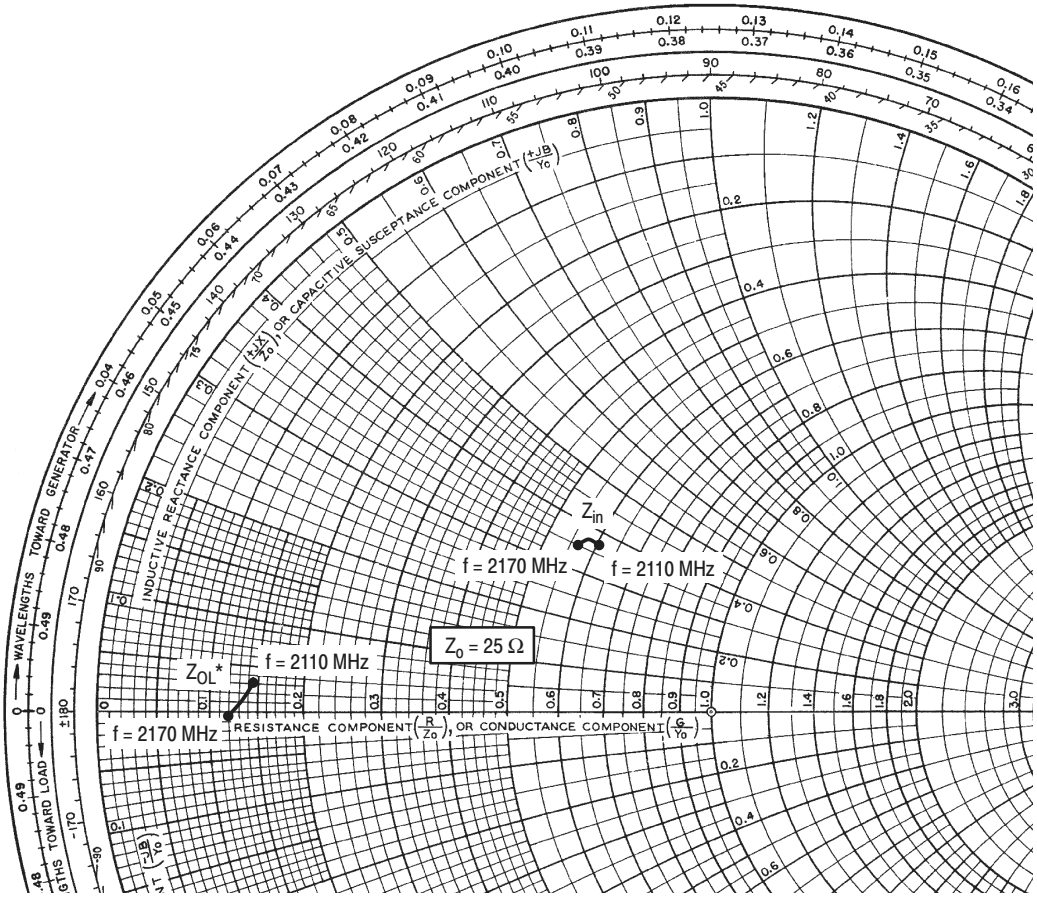


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



V_{DD} = 28 V, I_{DQ} = 250 mA, P_{out} = 30 W PEP

f MHz	Z_{in} Ω	Z_{OL}* Ω
2110	15.3 + j9.4	3.7 + j0.78
2140	14.6 + j9.4	3.4 + j0.37
2170	14.3 + j8.8	3.0 – j0.13

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

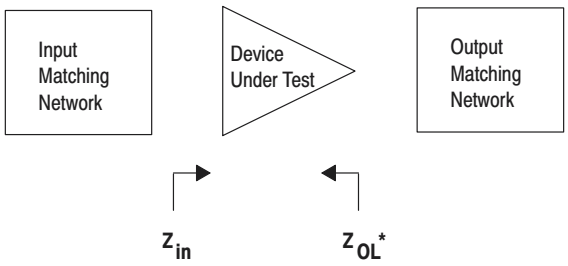
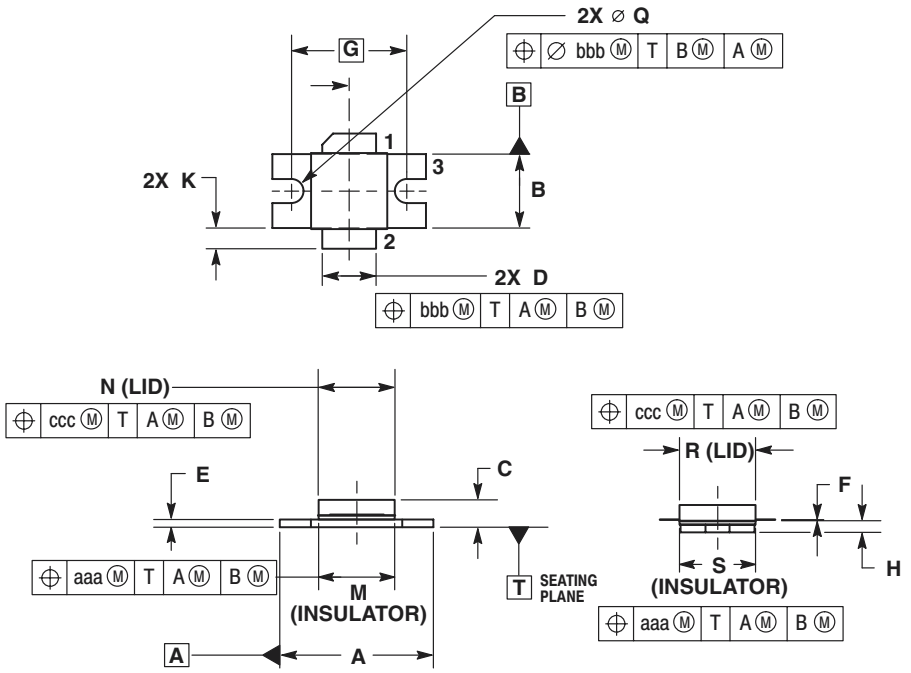


Figure 9. Series Equivalent Input and Output Impedance

NOTES

PACKAGE DIMENSIONS

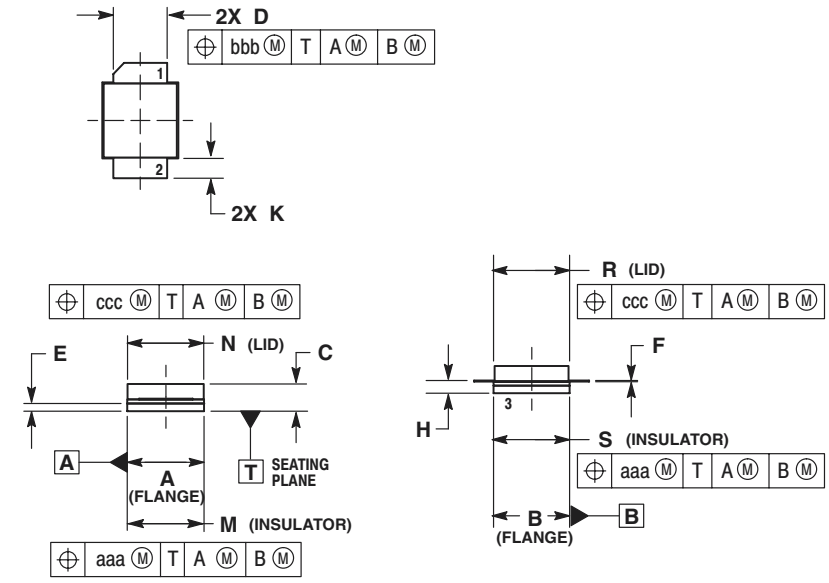


NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.795	.805	20.19	20.44
B	.380	.390	9.65	9.9
C	.125	.163	3.17	4.14
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.003	.006	0.07	0.15
G	.600 BSC		15.24 BSC	
H	.057	.067	1.45	1.7
K	.092	.122	2.33	3.1
M	.395	.405	10	10.3
N	.395	.405	10	10.3
Q	∅ .110	∅ .130	∅ 2.79	∅ 3.3
R	.395	.405	10	10.3
S	.395	.405	10	10.3
aaa	.005 BSC		0.127 BSC	
bbb	.010 BSC		0.254 BSC	
ccc	.015 BSC		0.381 BSC	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465E–03
ISSUE D
NI–400
MRF21030R3



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	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.395	.405	10.03	10.29
B	.395	.405	10.03	10.29
C	.125	.163	3.18	4.14
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.003	.006	0.08	0.15
H	.057	.067	1.45	1.70
K	.092	.122	2.34	3.10
M	.395	.405	10.03	10.29
N	.395	.405	10.03	10.29
R	.395	.405	10.03	10.29
S	.395	.405	10.03	10.29
aaa	.005 REF		0.127 REF	
bbb	.010 REF		0.254 REF	
ccc	.015 REF		0.38 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465F–03
ISSUE B
NI–400S
MRF21030SR3

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