PEDL66579-03

OKI Semiconductor

This version: Nov. 1999

MSM66579 Family

Preliminary

16-Bit Microcontroller

GENERAL DESCRIPTION

The MSM66579 family of highly functional CMOS 16-bit single chip microcontrollers utilizes the nX-8/500S, Oki's proprietary CPU core.

Four channels of serial ports, consisting of two channels of synchronous serial ports with 32-byte FIFO registers and two channels of UART/synchronous serial ports, enable easy interfacing with external peripheral LSI devices such as an encoder/decoder or servocontroller.

A switching function permits selection of separate address and data lines or multiplexed lines for the bus interface to correspond to various peripheral LSI devices.

With features such as a clock gear function, dual clock function, programmable pull-up ports in which individual bits can be programmed, and a small, thin package, the MSM66579 family of microprocessors is optimally suited for the system control of small-sized low power devices.

The flash ROM versions (MSM66Q577L and MSM66Q579L) programmable with a single 2.7V (minimum) power supply and flash ROM version (MSM66Q577) programmable with a single 5V power supply are also included in the family. These versions are easily adaptable to quick specification changes and to new product revisions.

APPLICATIONS

Digital Audio Control Systems
PC peripheral Control Systems
Office Electronics Control Systems

ORDERING INFORMATION

Order Code or Product Name	Package	Remark
MSM66577L-TB	100-pin plastic TQFP (TQFP 100-P-1414-0.50-K)	Low voltage mask ROM version (2.4 to 3.6 V)
MSM66577-TB		5 V mask ROM version
MSM66Q577L-TB		MSM66577L flash ROM version
MSM66Q577-TB		MSM66577 flash ROM version
MSM66579L-TB		Low voltage mask ROM version (2.4 to 3.6 V)
MSM66Q579L-TB		MSM66579L flash ROM version

FEATURES

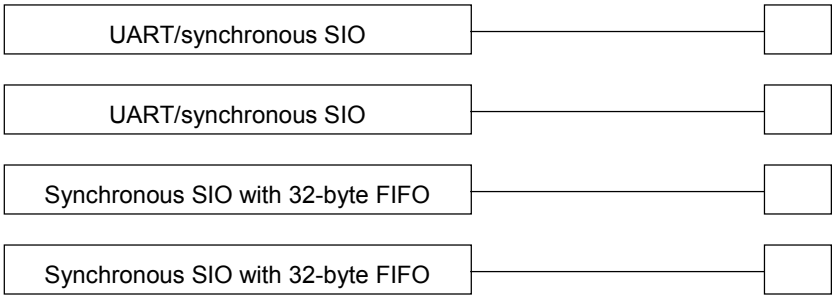
Name	MSM66577L	MSM66577	MSM66579L
Operating temperature	–30°C to +70°C		
Power supply voltage/ maximum frequency	V_{DD} = 2.4 to 3.6 V/f = 14 MHz	V_{DD} = 4.5 to 5.5 V/f = 30 MHz	V_{DD} = 2.4 to 3.6 V/f = 28 MHz
Minimum instruction execution time	143 ns at 14 MHz 61 µs at 32.768 kHz	67 ns at 30 MHz 61 µs at 32.768 kHz	71 ns at 28 MHz 61 µs at 32.768 kHz
Internal ROM size (max. external)	128 KB (1 MB)		
Internal RAM size (max. external)	4 KB (1 MB)		12 KB (1 MB)
I/O ports	74 I/O pins (with programmable pull-up resistors) 8 input-only pins		
Timers	16-bit free running timer × 1ch		
	Compare out/capture input × 2ch		
	16-bit timer (auto reload/timer out) × 1ch		
	8-bit auto reload timer × 2ch (can also be used as 16-bit timer × 1ch)		
	8-bit auto reload timer × 1ch		
	8-bit auto reload timer × 3ch (also functions as serial communication baud rate generator)		
	8-bit auto reload timer × 1ch (also functions as watchdog timer)		
	Watch timer (Real-timer counter) × 1ch		
	8-bit PWM × 4ch (can also be used as 16-bit PWM × 2ch)		
Serial port	Synchronous, with 32-byte FIFO × 2ch		
	UART/Synchronous × 2ch		
A/D converter	10-bit A/D converter × 8ch		
D/A converter	8-bit D/A converter × 2ch		
External interrupt	Non-maskable × 1ch Maskable × 8ch		
Interrupt priority	3 levels		
Others	Separate address and data busses/multiplexed address and data busses		
	Bus release function		
	Dual clocks		
Flash ROM version	MSM66Q577L	MSM66Q577	MSM66Q579L

SPECIAL FEATURES

1. High-performance CPU
The family includes the high-performance CPU, powerful bit manipulation instruction set, full symmetrical addressing mode, and ROM WINDOW function, and also provides the best optimized C compiler support.

2. A variety of power saving modes
Attaching a 32.768-kHz crystal produces a real-time clock signal from the internal clock timer. Use of a single clock in place of dual clocks is possible. Switching the CPU clock to this clock signal, 1/2 × main clock, or 1/4 × main clock, then produces operation in a low power consumption mode. The clock gear function allows a 1/2 × or 1/4 × main clock to be selected for the CPU operating clock.
The family provides a wide range of standby control functions. In addition to the usual STOP mode that stops the oscillator, there are the quick restart STOP mode that shuts down the CPU and peripherals but leaves the oscillator running, and the HALT mode that shuts down the CPU but leaves the peripherals running.

3. Variety of multifunctional serial ports
The family includes two channels of built-in synchronous serial ports with 32-byte FIFO implementing an auto transfer function. The family allows multi-byte 1-frame information which consists of address, command, and data to be easily and efficiently transmitted to or received from a serial interface type peripheral LSI device. The family also allows multi-byte character information to be easily and efficiently transmitted to or received from an LCD module. In addition, the family has two channels of combined UART/synchronous serial ports, and provides four channels of serial interfaces.



4. MSM66Q577L, MSM66Q577 and MSM66Q579L with flash memory programmable with single power supply
In addition to the regular mask ROM version, the family includes these versions with 128KB of flash memory that can be programmed using a single power supply. For the MSM66Q577L and MSM66Q579L, an internal booster circuit derives the necessary program voltage from the device's low (2.7 V min) power supply, and the program voltage for the MSM66Q577 is provided with a single 5 V power supply.

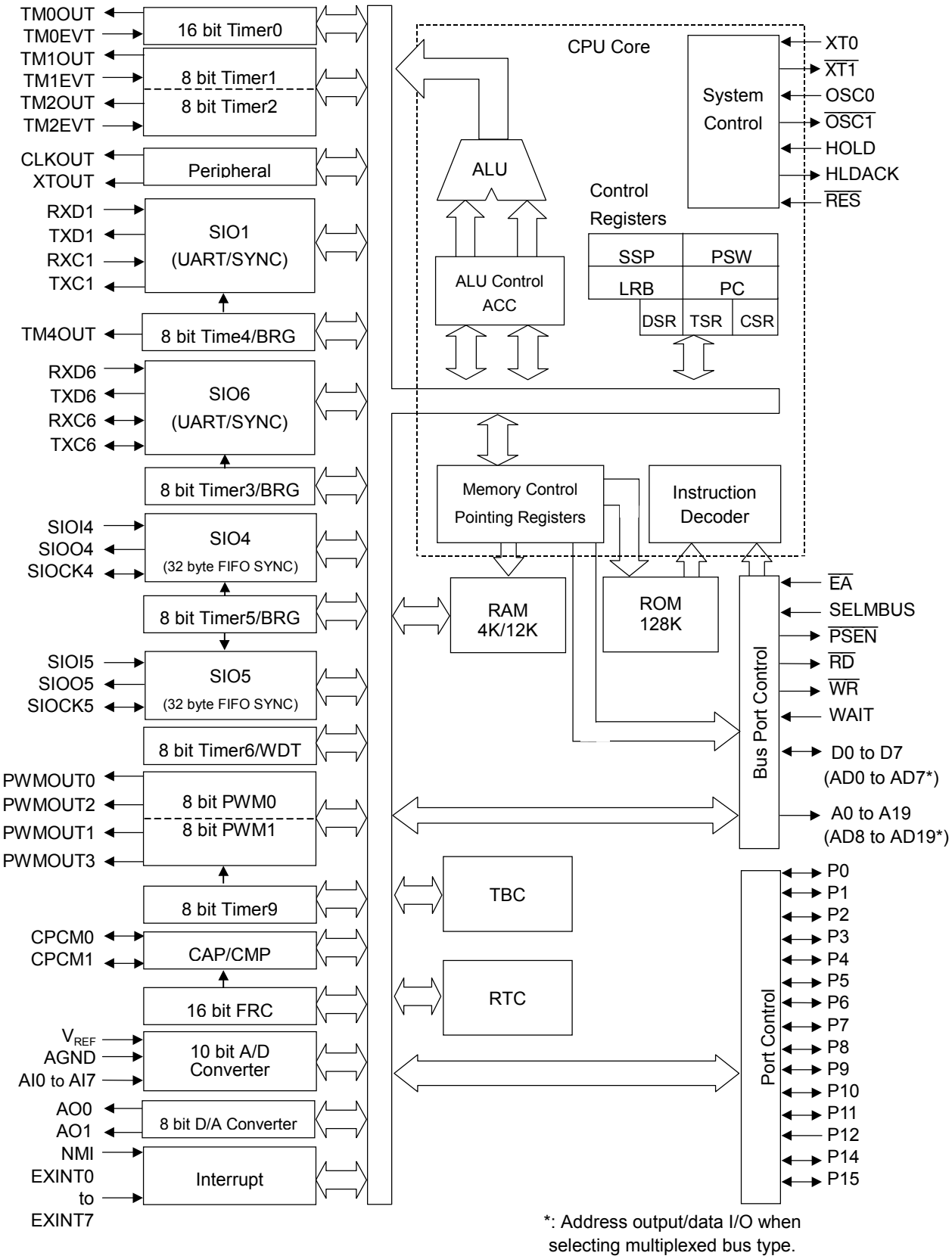
5. High-precision A/D and D/A converters
The family includes a high-precision 10-bit analog-to-digital converter with eight channels and 8-bit digital-to-analog converter with two channels.

6. Multifunction PWM
The family supports both 8- and 16-bit PWM operation. Choosing between the time-base counter output or overflow from an 8-bit auto-reload timer as the PWM counter clock source provides a wide number of possibilities over a broad frequency range. The 16-bit PWM configuration supports a high-speed synchronization mode that generates a high-precision output signal with less ripple suitable for digital-to-analog control applications.

7. Programmable pull-up resistors
Building the pull-up resistors into the chip contributes to overall design compactness. Making them programmable on a per-bit basis allows complete flexibility in circuit board layout and system design. These programmable pull-up resistors are available for all I/O pins not already assigned specific functions (such as the oscillator connection pins).

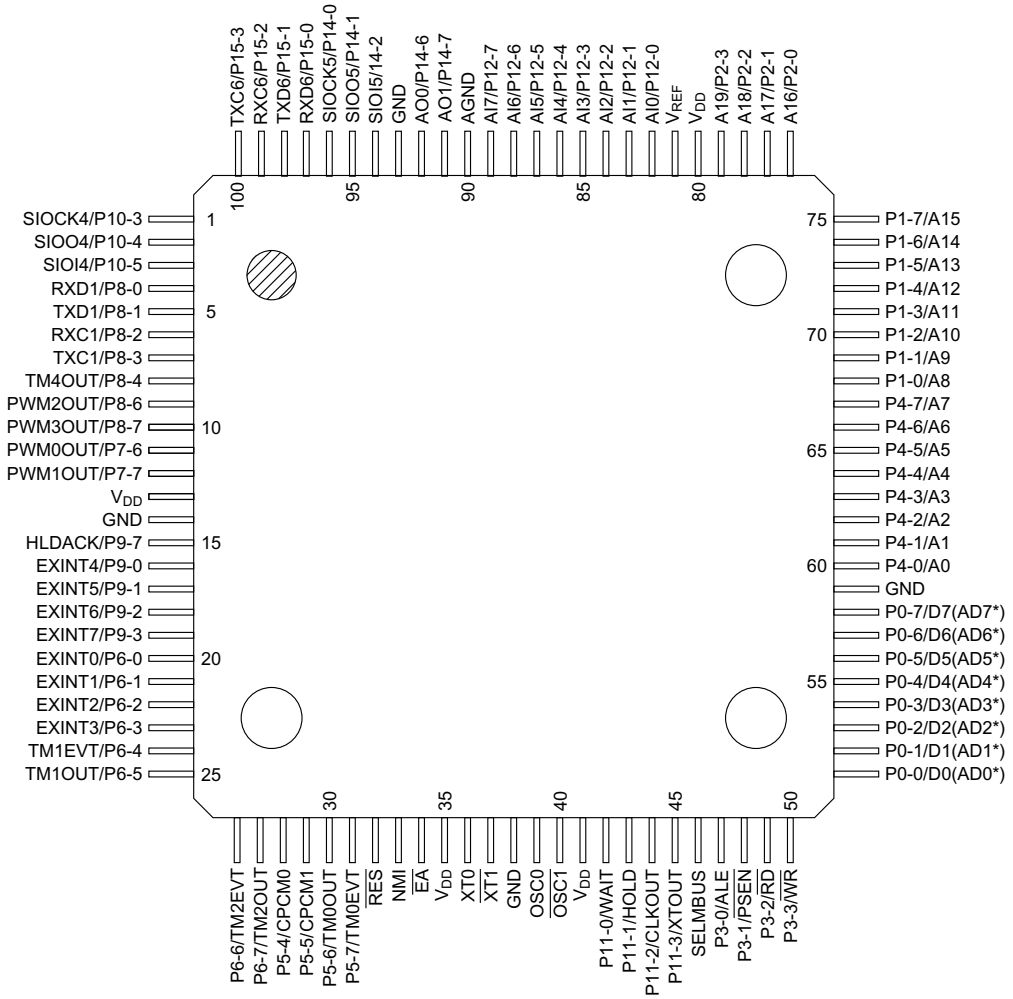
8. Wide support for external interrupts
There are a total of nine interrupt channels for use in communicating with external devices: eight for maskable interrupts and one for non-maskable interrupts.

BLOCK DIAGRAM



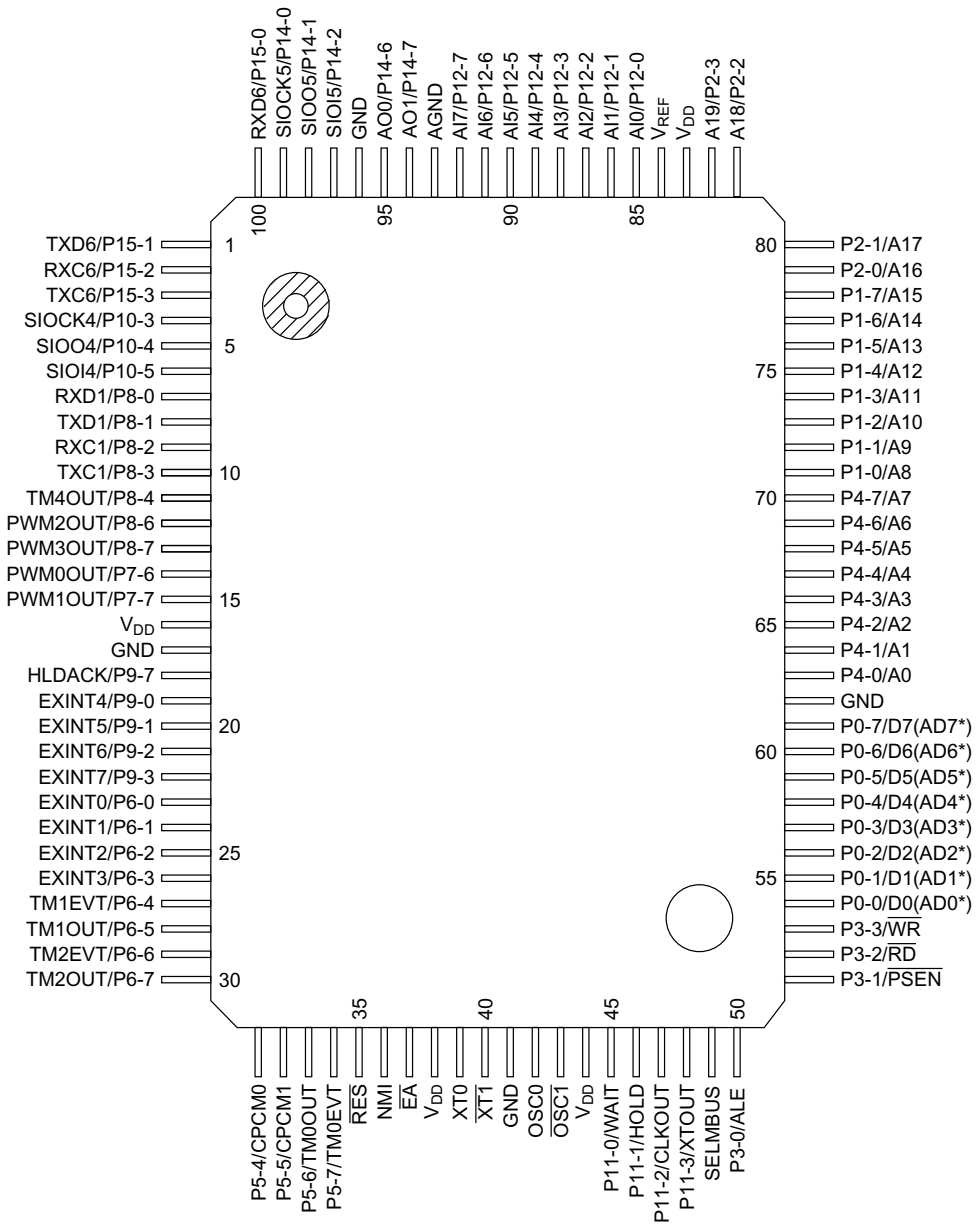
*: Address output/data I/O when selecting multiplexed bus type.

PIN CONFIGURATION (TOP VIEW)



100-pin Plastic TQFP

*: Address output/data I/O when selecting multiplexed bus type.



100-pin Plastic QFP

*: Address output/data I/O when selecting multiplexed bus type.

PIN DESCRIPTIONS

In the Type column, "I" indicates an input pin, "O" indicates an output pin, and "I/O" indicates an I/O pin.

Function	Symbol	Description			
		Primary function		Secondary function	
		Type		Type	
Port	P0_0/D0 (AD0) to P0_7/D7 (AD7)	I/O	8-bit I/O port 10 mA sink capability Pull-up resistors can be specified for each individual bit	I/O	External memory access Data I/O port (Address output/data I/O port when selecting a multiplexed bus)
	P1_0/A8 to P1_7/A15	I/O	8-bit I/O port Pull-up resistors can be specified for each individual bit	O	External memory access Address output port
	P2_0/A16 to P2_3/A19	I/O	4-bit I/O port Pull-up resistors can be specified for each individual bit	O	External memory access Address output port
	P3_0/ALE	I/O	4-bit I/O port 10 mA sink capability Pull-up resistors can be specified for each individual bit	O	External memory access Address latch enable signal output pin
	P3_1/$\overline{\text{PSEN}}$			O	External program memory access Read strobe output pin
	P3_2/$\overline{\text{RD}}$			O	External memory access Read strobe output pin
	P3_3/$\overline{\text{WR}}$			O	External memory access Write strobe output pin
	P4_0/A0 to P4_7/A7	I/O	8-bit I/O port Pull-up resistors can be specified for each individual bit	O	External memory access Address output port (When selecting a separate bus type)
	P5_4/CPCM0	I/O	4-bit I/O port Pull-up resistors can be specified for each individual bit	I/O	Capture 0 input / Compare 0 output pin
	P5_5/CPCM1			I/O	Capture 1 input / Compare 1 output pin
	P5_6/TM0OUT			O	Timer 0 timer output pin
	P5_7/TM0EVT			I	Timer 0 external event input pin
	P6_0/EXINT0	I/O	8-bit I/O port Pull-up resistors can be specified for each individual bit	I	External interrupt 0 input pin
	P6_1/EXINT1			I	External interrupt 1 input pin
	P6_2/EXINT2			I	External interrupt 2 input pin
	P6_3/EXINT3			I	External interrupt 3 input pin
	P6_4/TM1EVT			I	Timer1 external event input pin
	P6_5/TM1OUT			O	Timer 1 timer output pin
	P6_6/TM2EVT			I	Timer 2 external event pin
	P6_7/TM2OUT			O	Timer 2 timer output pin

Function	Symbol	Description			
		Primary function		Secondary function	
		Type		Type	
Port	P7_6/PWM0OUT	I/O	2-bit I/O port Pull-up resistors can be specified for each individual bit	O	PWM0 output pin
	P7_7/PWM1OUT			O	PWM1 output pin
	P8_0/RXD1	I/O	7-bit I/O port Pull-up resistors can be specified for each individual bit	I	SIO1 receive data input pin
	P8_1/TXD1			O	SIO1 transmit data output pin
	P8_2/RXC1			I/O	SIO1 receive clock I/O pin
	P8_3/TXC1			I/O	SIO1 transmit clock I/O pin
	P8_4/TM4OUT			O	Timer 4 timer output pin
	P8_6/PWM2OUT			O	PWM2 output pin
	P8_7/PWM3OUT			O	PWM3 output pin
	P9_0/EXINT4	I/O	5-bit I/O port Pull-up resistors can be specified for each individual bit	I	External Interrupt 4 input pin
	P9_1/EXINT5			I	External Interrupt 5 input pin
	P9_2/EXINT6			I	External Interrupt 6 input pin
	P9_3/EXINT7			I	External Interrupt 7 input pin
	P9_7/HLDACK			O	HOLD mode output pin
	P10_3/SIOCK4	I/O	3-bit I/O port Pull-up resistors can be specified for each individual bit	I/O	SIO4 transmit-receive clock I/O pin
	P10_4/SIOO4			I	SIO4 receive data input pin
	P10_5/SIOI4			O	SIO4 transmit data output pin
	P11_0/WAIT	I/O	4-bit I/O port 10 mA sink capability Pull-up resistors can be specified for each individual bit	I	External data memory access wait input pin
	P11_1/HOLD			I	HOLD mode request input pin
	P11_2/CLKOUT			O	Main clock pulse output pin
	P11_3/XTOUT			O	Sub clock pulse output pin
	P12_0/AI0 to P12_7/AI7	I	8-bit input port	I	A/D converter analog input port
	P14_0/SIOCK5	I/O	5-bit I/O port Pull-up resistors can be specified for each individual bit	I/O	SIO5 transmit-receive clock I/O pin
	P14_1/SIOO5			O	SIO5 transmit data output pin
	P14_2/SIOI5			I	SIO5 receive data input pin
	P14_6/AO0			O	D/A converter analog output port
	P14_7/AO1			O	D/A converter analog output port
	P15_0/RXD6	I/O	4-bit I/O port Pull-up resistors can be specified for each individual bit	I	SIO6 receive data input pin
	P15_1/TXD6			O	SIO6 transmit data output pin
	P15_2/RXC6			I/O	SIO6 receive clock I/O pin
	P15_3/TXC6			I/O	SIO6 transmit clock I/O pin

Function	Symbol	Type	Description
Power supply	V_{DD}	I	Power supply pin Connect all V_{DD} pins to the power supply.*
	GND	I	GND pin Connect all GND pins to GND.*
	V_{REF}	I	Analog reference voltage pin
	AGND	I	Analog GND pin
Oscillation	XT0	I	Sub clock oscillation input pin Connect to a crystal oscillator of f = 32.768 kHz.
	$\overline{XT1}$	O	Sub clock oscillation output pin Connect to a crystal oscillator of f = 32.768 kHz. The clock output is opposite in phase to XT0.
	OSC0	I	Main clock oscillation input pin Connect to a crystal or ceramic oscillator. Or, input an external clock.
	$\overline{OSC1}$	O	Main clock oscillation output pin Connect to a crystal or ceramic oscillator. The clock output is opposite in phase to OSC0. Leave this pin unconnected when an external clock is used.
Reset	$\overline{RES}$	I	Reset input pin
Other	NMI	I	Non-maskable interrupt input pin
	$\overline{EA}$	I	External program memory access input pin If the $\overline{EA}$ pin is enabled (low level), the internal program memory is masked and the CPU executes the program code in external program memory through all address space.
	SELMBUS	I	SELMBUS = H: Address/data separate bus type SELMBUS = L: Multiplexed bus type

* Each of the family devices has unique pattern routes for the internal power and ground. Connect the power supply voltage to all V_{DD} pins and the ground potential to all GND pins. If a device may have one or more V_{DD} or GND pins to which the power supply voltage or the ground potential is not connected, it can not be guaranteed for normal operation.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition		Rating	Unit
Digital power supply voltage	V_{DD}	GND = AGND = 0 V Ta = 25°C		–0.3 to +7.0	V
Input voltage	V_I			–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog reference voltage	V_{REF}			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AI}			–0.3 to V_{REF}	V
Power dissipation	P_D	Ta = 70°C per package	100-pin TQFP	650	mW
			100-pin QFP	750	mW
Storage Temperature	T_{STG}	—		–50 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition		Range	Unit
Digital power supply voltage	V_{DD}	MSM66577	$f_{OSC} \leq 30$ MHz	4.5 to 5.5	V
		MSM66577L	$f_{OSC} \leq 14$ MHz	2.4 to 3.6	
		MSM66579L	$f_{OSC} \leq 28$ MHz	2.4 to 3.6	
		MSM66Q577	$f_{OSC} \leq 30$ MHz	4.5 to 5.5	
		MSM66Q577L	$f_{OSC} \leq 14$ MHz	2.7 to 3.3	
		MSM66Q579L	$f_{OSC} \leq 28$ MHz	2.7 to 3.3	
Analog reference voltage	V_{REF}	—		V_{DD} –0.3 to V_{DD}	V
Analog input voltage	V_{AI}	—		AGND to V_{REF}	V
Memory hold voltage	V_{DDH}	f_{OSC} = 0 Hz		2.0 to 5.5	V
Operating frequency	f_{OSC}	MSM66577	V_{DD} = 4.5 to 5.5 V	2 to 30	MHz
		MSM66577L	V_{DD} = 2.4 to 3.6 V	2 to 14	
		MSM66579L	V_{DD} = 2.4 to 3.6 V	2 to 28	
		MSM66Q577	V_{DD} = 4.5 to 5.5 V	2 to 30	
		MSM66Q577L	V_{DD} = 2.7 to 3.3 V	2 to 14	
		MSM66Q579L	V_{DD} = 2.7 to 3.3 V	2 to 28	
	f_{XT}	—		32.768	kHz
Ambient temperature	Ta	—		–30 to +70	°C
Fan out	N	MOS load		20	—
		TTL load	P0, P3, P11	6	—
			P1, P2, P4, P5, P6, P7, P8, P9, P10, P14, P15	1	—

ALLOWABLE OUTPUT CURRENT VALUES

MSM66577L/577/579L (V_{DD} = 2.4 to 3.6 V/4.5 to 5.5 V, Ta = –30 to +70°C)
MSM66Q577L/Q577/Q579L (V_{DD} = 2.7 to 3.3 V/4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Pin	Symbol	Min.	Typ.	Max.	Unit
"H" output pin (1 pin)	All output pins	I_{OH}	—	—	–2	mA
"H" output pins (sum total)	Sum total of all output pins	ΣI_{OH}	—	—	–40	
"L" output pin (1 pin)	P0, P3, P11	I_{OL}	—	—	10	
	Other ports				5	
"L" output pins (sum total)	Sum total of P0, P3, P11	ΣI_{OL}	—	—	80	
	Sum total of P1, P2, P4				50	
	Sum total of P5, P6, P9					
	Sum total of P7, P8, P10, P14, P15					
	Sum total of all output pins				140	

[Note]
Each of the family devices has unique pattern routes for the internal power and ground. Connect the power supply voltage to all V_{DD} pins and the ground potential to all GND pins. If a device may have one or more V_{DD} or GND pins to which the power supply voltage or the ground potential is not connected, it can not be guaranteed for normal operation.

ELELCTRICAL CHARACTERISTICS

DC Characteristics 1 (V_{DD} = 4.5 to 5.5 V)

(V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage *1	V_{IH}	—	0.44V_{DD}	—	V_{DD}+0.3	V
"H" input voltage *2,*3,*4,*5,*6,*7			0.80V_{DD}	—	V_{DD}+0.3	
"L" input voltage *1	V_{IL}	—	–0.3	—	0.16V_{DD}	
"L" input voltage *2,*3,*4,*5,*6,*7			–0.3	—	0.2V_{DD}	
"H" output voltage *1, *4	V_{OH}	I_O = –400 µA	V_{DD}–0.4	—	—	
		I_O = –2.0 mA	V_{DD}–0.6	—	—	
"H" output voltage *2		I_O = –200 µA	V_{DD}–0.4	—	—	
		I_O = –2.0 mA	V_{DD}–0.6	—	—	
"L" output voltage *1, *4	V_{OL}	I_O = 3.2 mA	—	—	0.4	
		I_O = 10.0 mA	—	—	0.8	
"L" output voltage *2		I_O = 1.6 mA	—	—	0.4	
		I_O = 5.0 mA	—	—	0.8	
Input leakage current *3, *6	I_{IH}/I_{IL}	V_I = V_{DD}/0 V	—	—	1/–1	µA
Input current *5			—	—	1/–250	
Input current *7			—	—	15/–15	
Output leakage current *1, *2, *4	I_{LO}	V_O = V_{DD}/0 V	—	—	±10	µA
Pull-up resistance	R_{pull}	V_I = 0 V	25	50	100	kΩ
Input capacitance	C_I	f = 1 MHz, Ta = 25°C	—	5	—	pF
Output capacitance	C_O		—	7	—	
Analog reference supply current	I_{REF}	During A/D operation	—	—	4	mA
		When A/D is stopped	—	—	10	µA
Supply current (STOP mode)	I_{DDS}	OSC is stopped, XT is not used. V_{DD} = 2 V, Ta = 25°C *8	—	0.2	10	µA
		OSC is stopped, XT is not used. *8	—	1	100	
Supply current (HALT mode)	I_{DDH}	f = 30 MHz, No Load	—	40	60	mA
		f = 30 MHz, No Load	—	60	90	mA
Supply current	I_{DD}	f = 32.768 kHz, No Load	—	70	120	µA

*1: Applicable to P0
*2: Applicable to P1, P2, P4, P5, P6, P7, P8, P9, P10, P14, P15
*3: Applicable to P12
*4: Applicable to P3, p11
*5: Applicable to $\overline{RES}$
*6: Applicable to SELMBUS, $\overline{EA}$, NMI
*7: Applicable to OSC0
*8: Ports used as inputs are at V_{DD} or 0 V. Other ports are unloaded.

DC Characteristics 2 (V_{DD} = 2.4 to 3.6 V)

MSM66577L/579L (V_{DD} = 2.4 to 3.6 V, Ta = –30 to +70°C)
MSM66Q577L/Q579L (V_{DD} = 2.7 to 3.3 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage *1	V_{IH}	—	0.44V_{DD}	—	V_{DD}+0.3	V
"H" input voltage *2,*3,*4,*5,*6,*7			0.80V_{DD}	—	V_{DD}+0.3	
"L" input voltage *1	V_{IL}	—	–0.3	—	0.16V_{DD}	
"L" input voltage *2,*3,*4,*5,*6,*7			–0.3	—	0.2V_{DD}	
"H" output voltage *1, *4	V_{OH}	I_O = –400 µA	V_{DD}–0.4	—	—	
		I_O = –2.0 mA	V_{DD}–0.8	—	—	
"H" output voltage *2		I_O = –200 µA	V_{DD}–0.4	—	—	
		I_O = –1.0 mA	V_{DD}–0.8	—	—	
"L" output voltage *1, *4	V_{OL}	I_O = 3.2 mA	—	—	0.5	
		I_O = 5.0 mA	—	—	0.9	
"L" output voltage *2		I_O = 1.6 mA	—	—	0.5	
		I_O = 2.5 mA	—	—	0.9	
Input leakage current *3, *6	I_{IH}/I_{IL}	V_I = V_{DD}/0 V	—	—	1/–1	µA
Input current *5			—	—	1/–250	
Input current *7			—	—	15/–15	
Output leakage current *1, *2, *4	I_{LO}	V_O = V_{DD}/0 V	—	—	±10	µA
Pull-up resistance	R_{pull}	V_I = 0 V	40	100	200	kΩ
Input capacitance	C_I	f = 1 MHz, Ta = 25°C	—	5	—	pF
Output capacitance	C_O		—	7	—	
Analog reference supply current	I_{REF}	During A/D operation	—	—	2	mA
		When A/D is stopped	—	—	5	µA
Supply current (STOP mode)	I_{DDS}	OSC is stopped, XT is not used. V_{DD} = 2 V, Ta = 25°C *8	—	0.2	10	µA
		OSC is stopped, XT is not used. *8	—	1	100	
Supply current (HALT mode)	I_{DDH}	f = 14 MHz, No Load	—	—	TBD	mA
		f = 14 MHz, No Load	—	—	TBD	mA
Supply current	I_{DD}	f = 32.768 kHz, No Load	—	—	TBD	µA

*1: Applicable to P0
*2: Applicable to P1, P2, P4, P5, P6, P7, P8, P9, P10, P14, P15
*3: Applicable to P12
*4: Applicable to P3, p11
*5: Applicable to $\overline{RES}$
*6: Applicable to SELMBUS, $\overline{EA}$, NMI
*7: Applicable to OSC0
*8: Ports used as inputs are at V_{DD} or 0 V. Other ports are unloaded.

AC Characteristics 1 (V_{DD} = 4.5 to 5.5 V)

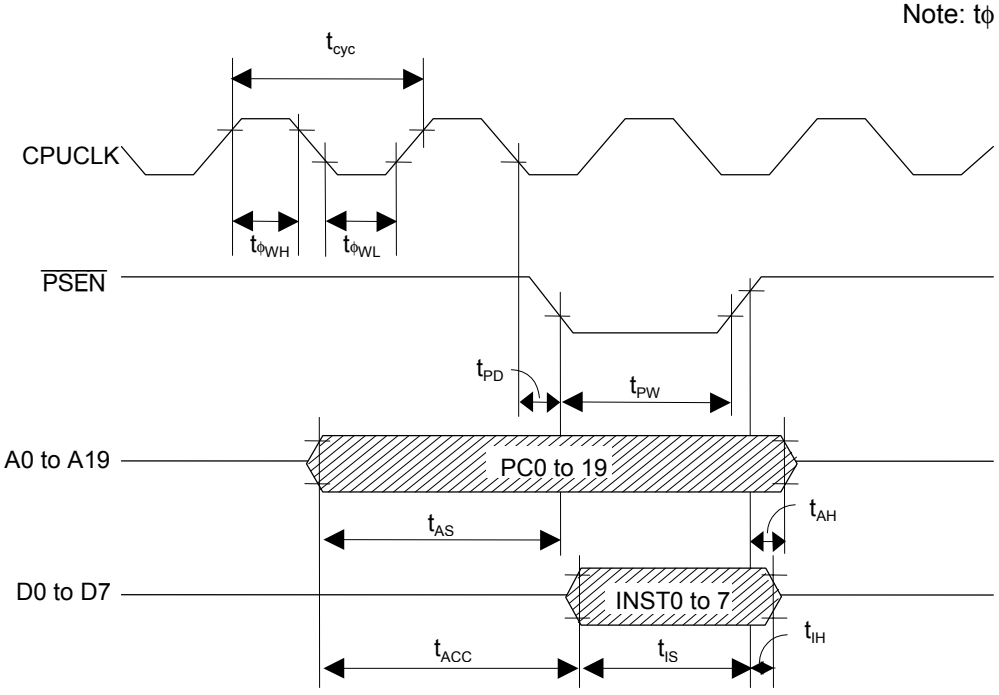
(1) Separate Bus Type

External program memory control

(V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 30 MHz	33.3	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	13	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		13	—	
$\overline{PSEN}$ pulse width	t_{PW}		2 tϕ – 15	—	
$\overline{PSEN}$ pulse delay time	t_{PD}		—	45	
Address setup time	t_{AS}		tϕ – 25	—	
Address hold time	t_{AH}		0	9	
Instruction setup time	t_{IS}		30	—	
Instruction hold time	t_{IH}		0	—	
Read data access time	t_{ACC}		—	3 tϕ – 70	

Note: $t\phi = t_{cyc}/2$



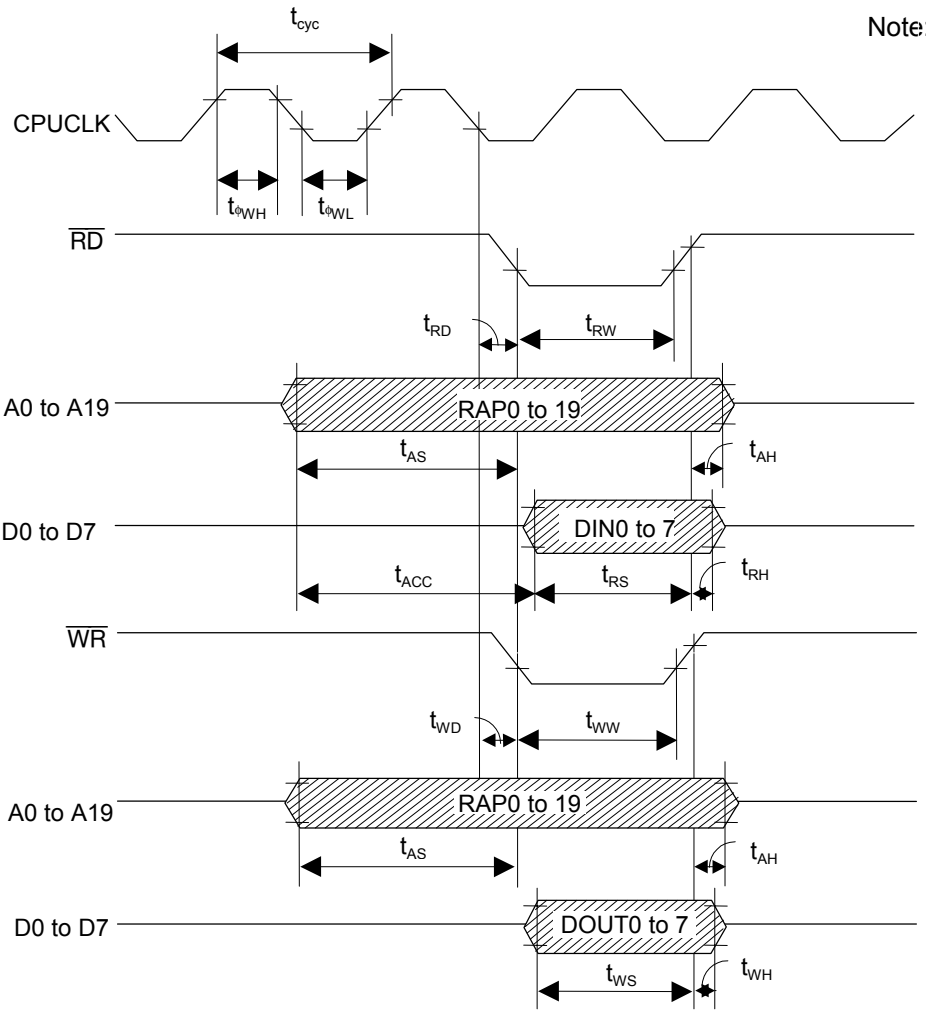
Bus timing during no wait cycle time

External data memory control

(V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 30 MHz	33.3	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	13	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		13	—	
$\overline{RD}$ pulse width	t_{RW}		2 tϕ – 15	—	
$\overline{WR}$ pulse width	t_{WW}		2 tϕ – 15	—	
$\overline{RD}$ pulse delay time	t_{RD}		—	45	
$\overline{WR}$ pulse delay time	t_{WD}		—	45	
Address setup time	t_{AS}		tϕ – 25	—	
Address hold time	t_{AH}		tϕ – 3	tϕ +3	
Read data setup time	t_{RS}		30	—	
Read data hold time	t_{RH}		0	—	
Read data access time	t_{ACC}		—	3tϕ –70	
Write data setup time	t_{WS}		2tϕ – 30	—	
Write data hold time	t_{WH}		tϕ – 3	tϕ + 3	

Note: $t\phi = t_{cyc}/2$



Bus timing during no wait cycle time

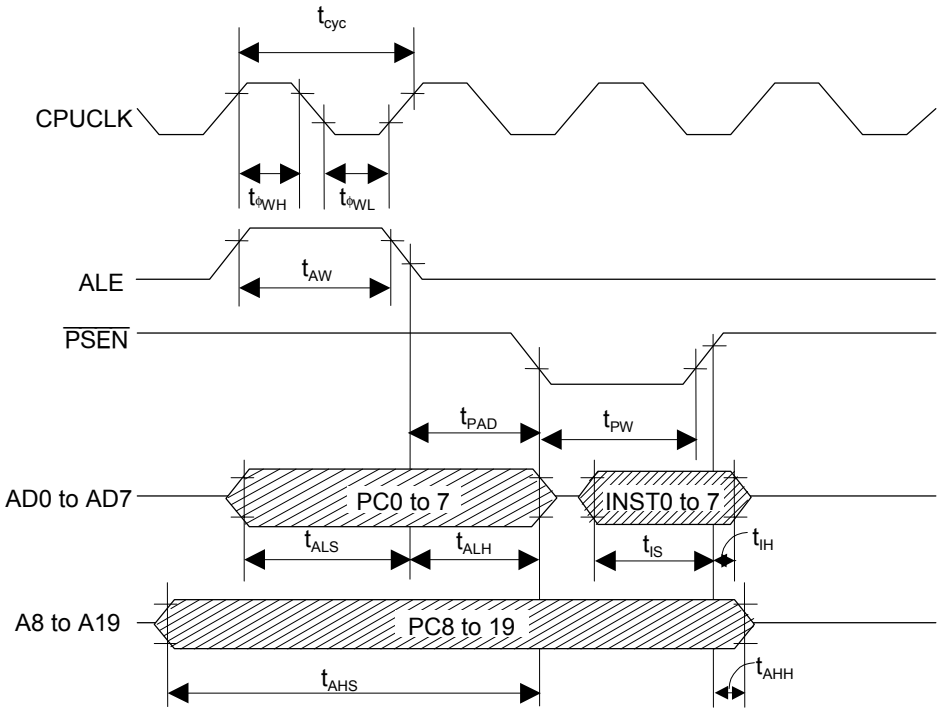
(2) Multiplexed bus type

External program memory control

(V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 30 MHz	33.3	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	13	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		13	—	
ALE pulse width	T_{AW}		2 tϕ – 10	—	
$\overline{PSEN}$ pulse width	t_{PW}		2 tϕ – 14	—	
$\overline{PSEN}$ pulse delay time	t_{PAD}		tϕ – 10	tϕ + 10	
Low address setup time	t_{ALS}		2tϕ – 20	2tϕ + 3	
Low address hold time	t_{ALH}		tϕ – 10	tϕ + 10	
High address setup time	t_{AHS}		3tϕ – 30	4tϕ + 3	
High address hold time	t_{AHH}		0	tϕ + 10	
Instruction setup time	t_{IS}		24	—	
Instruction hold time	t_{IH}		0	tϕ – 3	

Note: $t\phi = t_{cyc}/2$



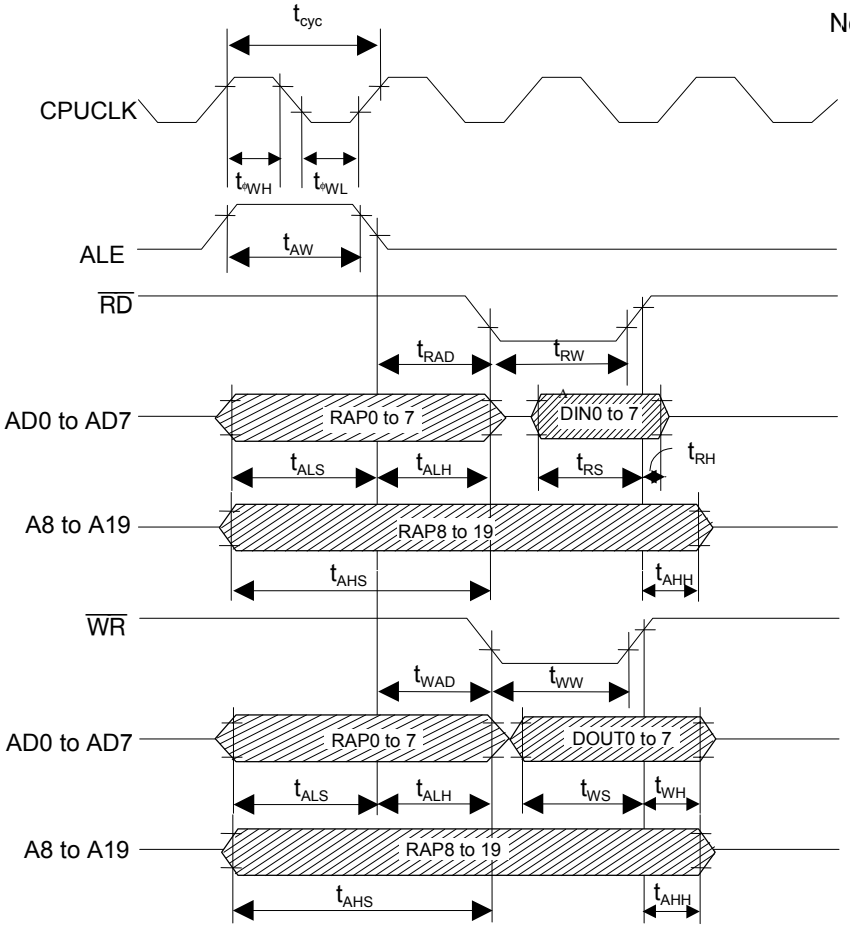
Bus timing during no wait cycle time

External data memory control

(V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 30 MHz	33.3	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	13	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		13	—	
ALE pulse width	t_{AW}		2 tϕ – 10	—	
$\overline{RD}$ pulse width	t_{RW}		2 tϕ – 14	—	
$\overline{WR}$ pulse width	t_{WW}		2 tϕ – 14	—	
$\overline{RD}$ pulse delay time	t_{RAD}		tϕ – 10	tϕ +10	
$\overline{WR}$ pulse delay time	t_{WAD}		tϕ – 10	tϕ +10	
Low address setup time	t_{ALS}		2 tϕ – 20	2 tϕ +3	
Low address hold time	t_{ALH}		tϕ – 10	tϕ +10	
High address setup time	t_{AHS}		3 tϕ – 30	3 tϕ +3	
High address hold time	t_{AHH}		tϕ – 10	tϕ +10	
Read data setup time	t_{RS}		24	—	
Read data hold time	t_{RH}		0	tϕ – 3	
Write data setup time	t_{WS}		2tϕ – 12	—	
Write data hold time	t_{WH}		tϕ – 3	tϕ + 3	

Note: $t\phi = t_{cyc}/2$



Bus timing during no wait cycle time

(3) Serial port control

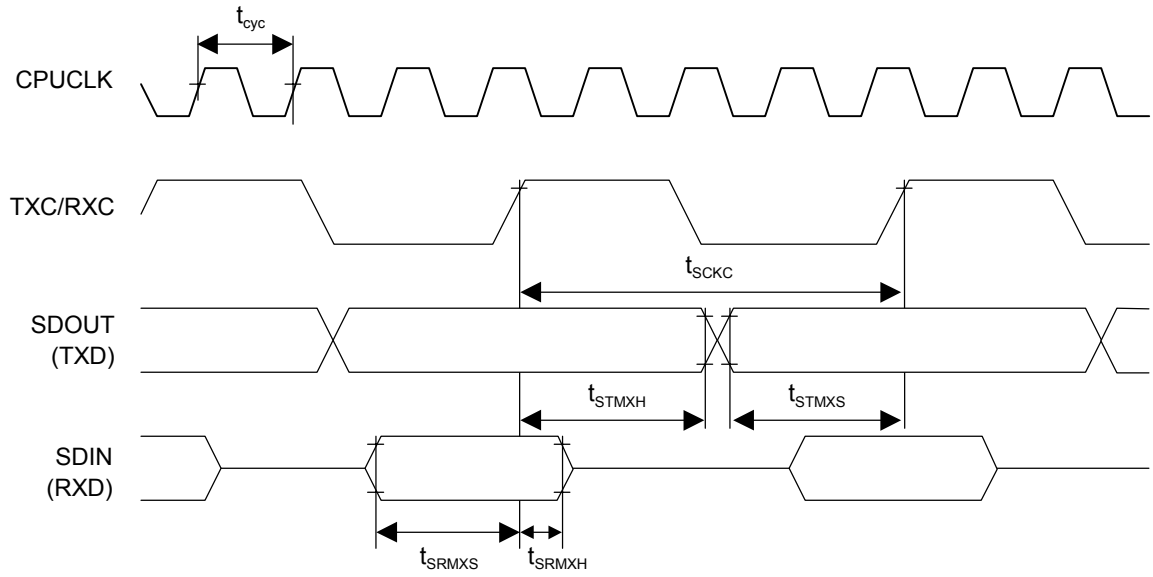
Serial ports 1 and 6 (SIO1 and 6)

Master mode (Clock synchronous serial port)

(V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 30 MHz	33.3	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	4 t_{cyc}	—	
Output data setup time	t_{STMXS}		2 tϕ – 5	—	
Output data hold time	t_{STMXH}		5 tϕ – 10	—	
Input data setup time	t_{SRMXS}		13	—	
Input data hold time	t_{SRMXH}		0	—	

Note: tϕ = t_{cyc}/2

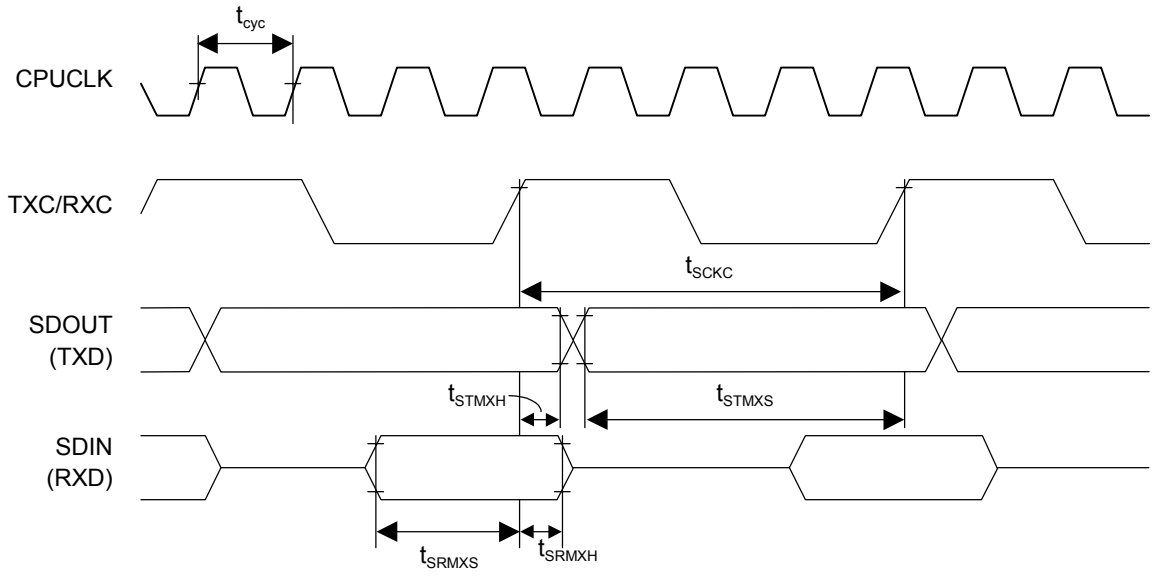


Slave mode (Clock synchronous serial port)

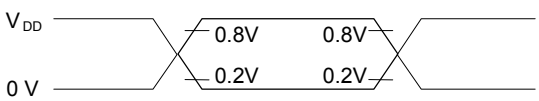
(V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 30 MHz	33.3	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	4 t_{cyc}	—	
Output data setup time	t_{STMXS}		2 tϕ – 15	—	
Output data hold time	t_{STMXH}		4 tϕ – 10	—	
Input data setup time	t_{SRMXS}		13	—	
Input data hold time	t_{SRMXH}		3	—	

Note: tϕ = t_{cyc}/2



Measurement points for AC timing



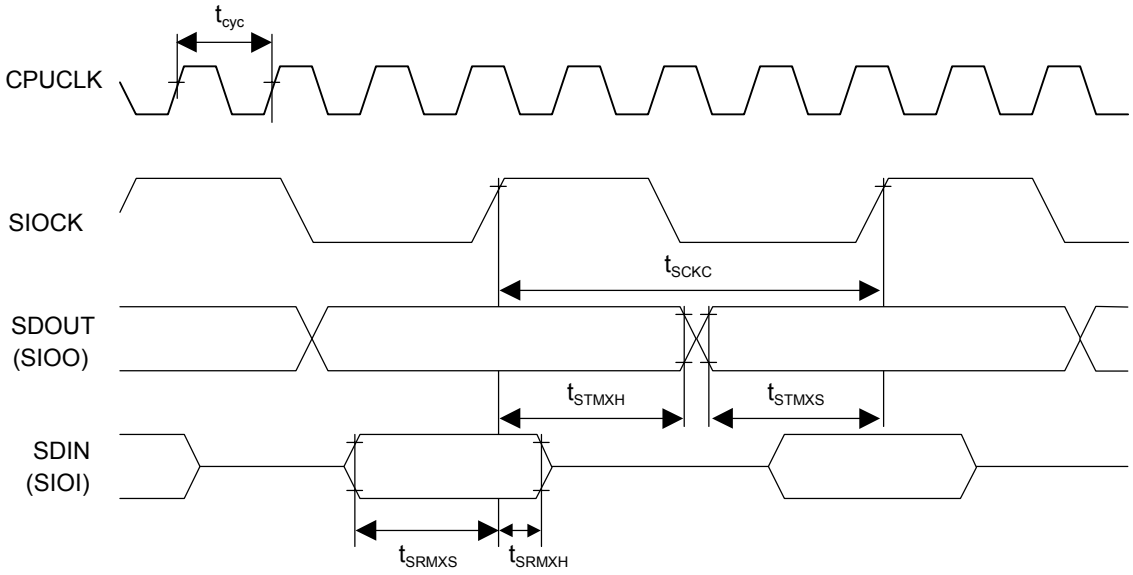
Serial ports 4 and 5 (SIO4 and 5)

Master mode (Clock synchronous serial port)

(V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 30 MHz	33.3	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	6 t_{cyc}	—	
Output data setup time	t_{STMXS}		6 tϕ – 5	—	
Output data hold time	t_{STMXH}		4.5 tϕ – 10	—	
Input data setup time	t_{SRMXS}		13	—	
Input data hold time	t_{SRMXH}		0	—	

Note: tϕ = t_{cyc}/2

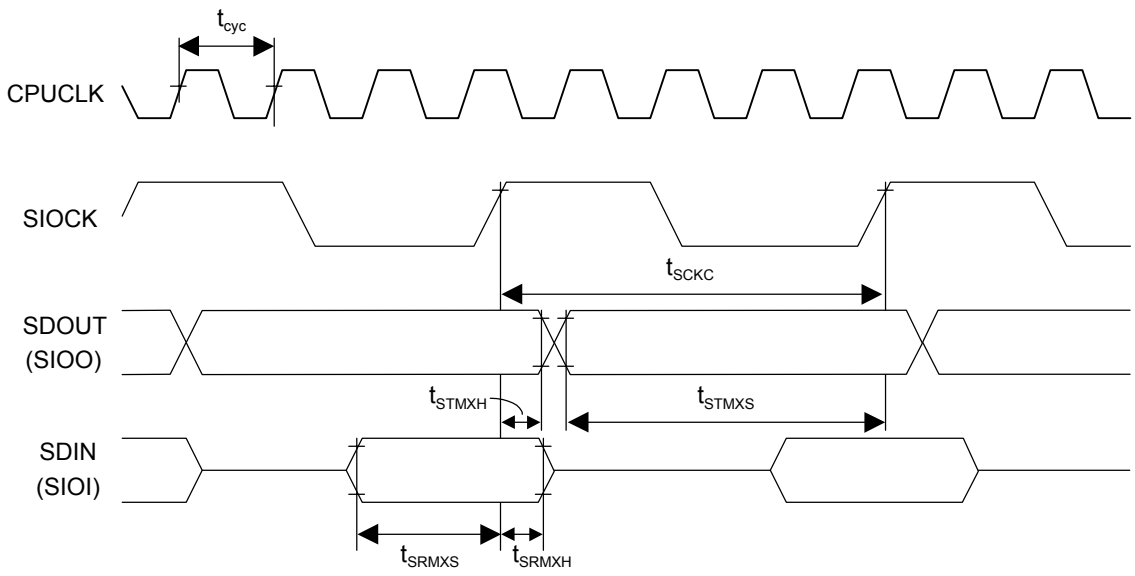


Slave mode (Clock synchronous serial port)

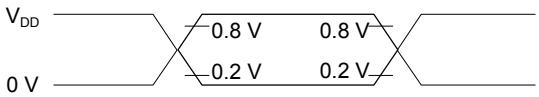
(V_{DD} = 4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 30 MHz	33.3	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	6 t_{cyc}	—	
Output data setup time	t_{STMXS}		3 tϕ – 15	—	
Output data hold time	t_{STMXH}		6 tϕ – 10	—	
Input data setup time	t_{SRMXS}		13	—	
Input data hold time	t_{SRMXH}		3	—	

Note: $t\phi = t_{cyc}/2$



Measurement points for AC timing



AC Characteristics 2 (V_{DD} = 2.4 to 3.6 V)

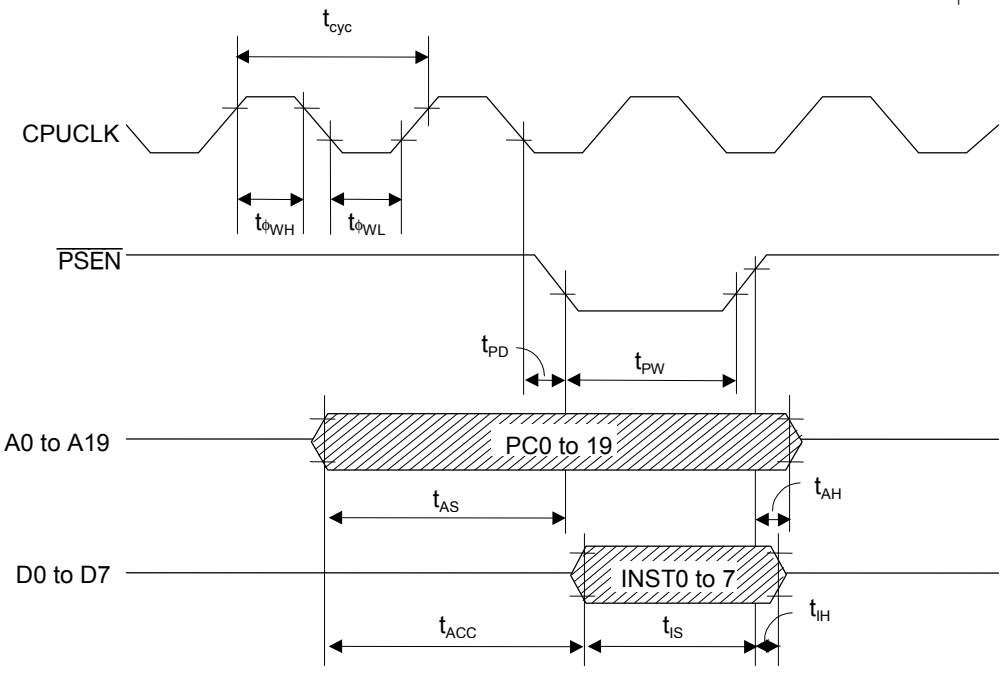
(1) Separate Bus Type

External program memory control

MSM66577L/579L (V_{DD} = 2.4 to 3.6 V, Ta = –30 to +70°C)
MSM66Q577L/Q579L (V_{DD} = 2.7 to 3.3 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 14 MHz	71.4	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	28	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		28	—	
$\overline{PSEN}$ pulse width	t_{PW}		2 tϕ – 20	—	
$\overline{PSEN}$ pulse delay time	t_{PD}		—	75	
Address setup time	t_{AS}		tϕ – 40	—	
Address hold time	t_{AH}		0	18	
Instruction setup time	t_{IS}		60	—	
Instruction hold time	t_{IH}		0	—	
Read data access time	t_{ACC}		—	3 tϕ – 120	

Note: tϕ = t_{cyc}/2



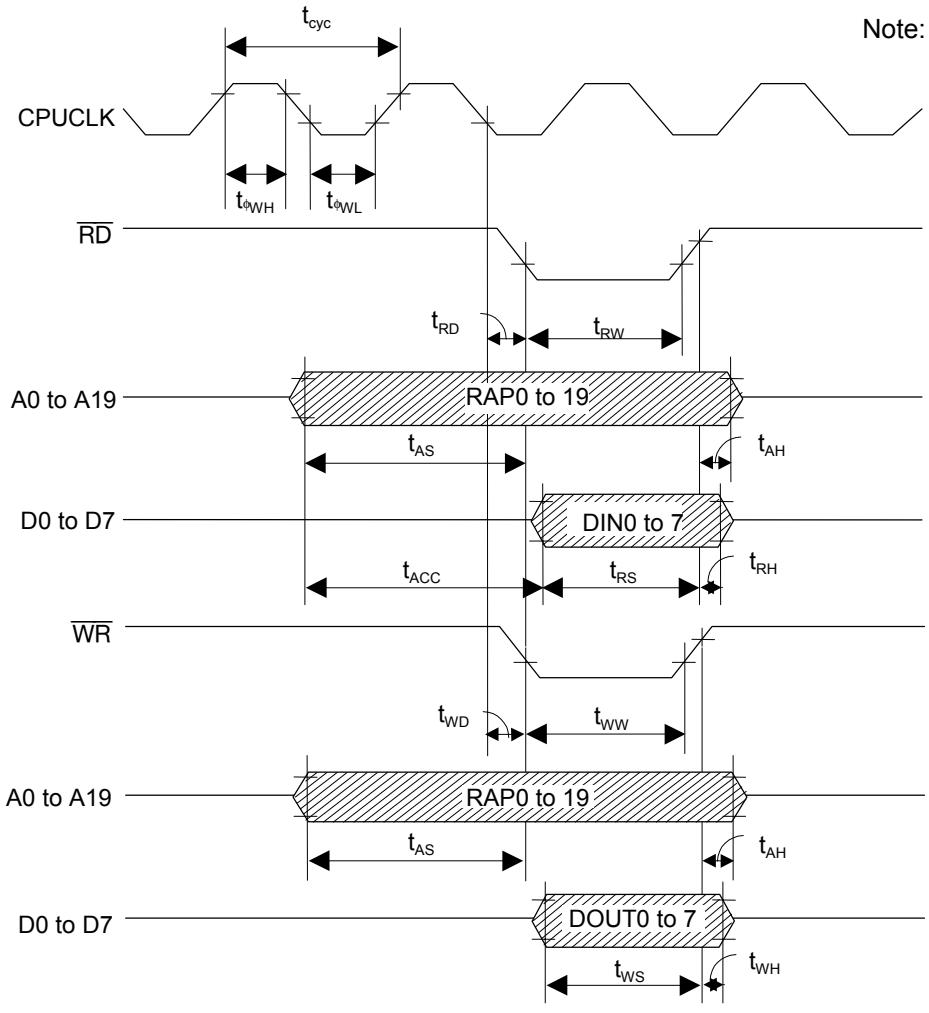
Bus timing during no wait cycle time

External data memory control

MSM66577L/579L (V_{DD} = 2.4 to 3.6 V, Ta = –30 to +70°C)
MSM66Q577L/Q579L (V_{DD} = 2.7 to 3.3 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 14 MHz	71.4	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	28	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		28	—	
$\overline{RD}$ pulse width	t_{RW}		2 tϕ – 20	—	
$\overline{WR}$ pulse width	t_{WW}		2 tϕ – 20	—	
$\overline{RD}$ pulse delay time	t_{RD}		—	75	
$\overline{WR}$ pulse delay time	t_{WD}		—	75	
Address setup time	t_{AS}		tϕ – 40	—	
Address hold time	t_{AH}		tϕ – 6	tϕ +6	
Read data setup time	t_{RS}		60	—	
Read data hold time	t_{RH}		0	—	
Read data access time	t_{ACC}		—	3tϕ –120	
Write data setup time	t_{WS}		2tϕ – 40	—	
Write data hold time	t_{WH}		tϕ – 6	tϕ + 6	

Note: $t\phi = t_{cyc}/2$



Bus timing during no wait cycle time

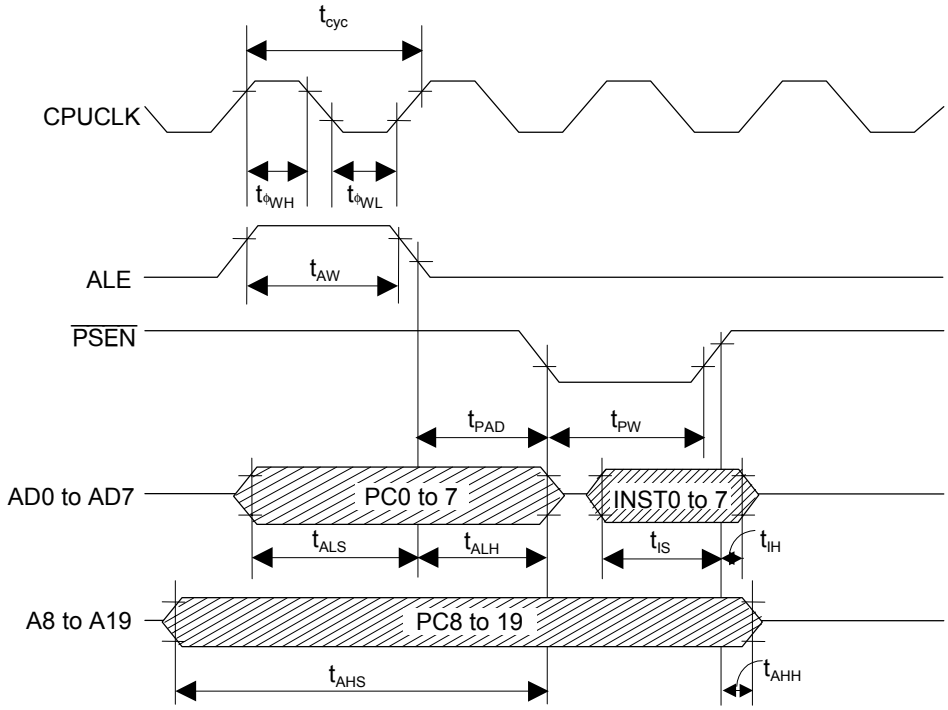
(2) Multiplexed bus type

External program memory control

MSM66577L/579L (V_{DD} = 2.4 to 3.6 V, Ta = –30 to +70°C)
MSM66Q577L/Q579L (V_{DD} = 2.7 to 3.3 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 14 MHz	71.4	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	28	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		28	—	
ALE pulse width	t_{AW}		2 tϕ – 15	—	
$\overline{PSEN}$ pulse width	t_{PW}		2 tϕ – 18	—	
$\overline{PSEN}$ pulse delay time	t_{PAD}		tϕ – 6	tϕ + 6	
Low address setup time	t_{ALS}		2tϕ – 40	2tϕ + 6	
Low address hold time	t_{ALH}		tϕ – 15	tϕ + 15	
High address setup time	t_{AHS}		3tϕ – 50	4tϕ + 6	
High address hold time	t_{AHH}		0	tϕ + 15	
Instruction setup time	t_{IS}		58	—	
Instruction hold time	t_{IH}		0	tϕ – 6	

Note: $t\phi = t_{cyc}/2$



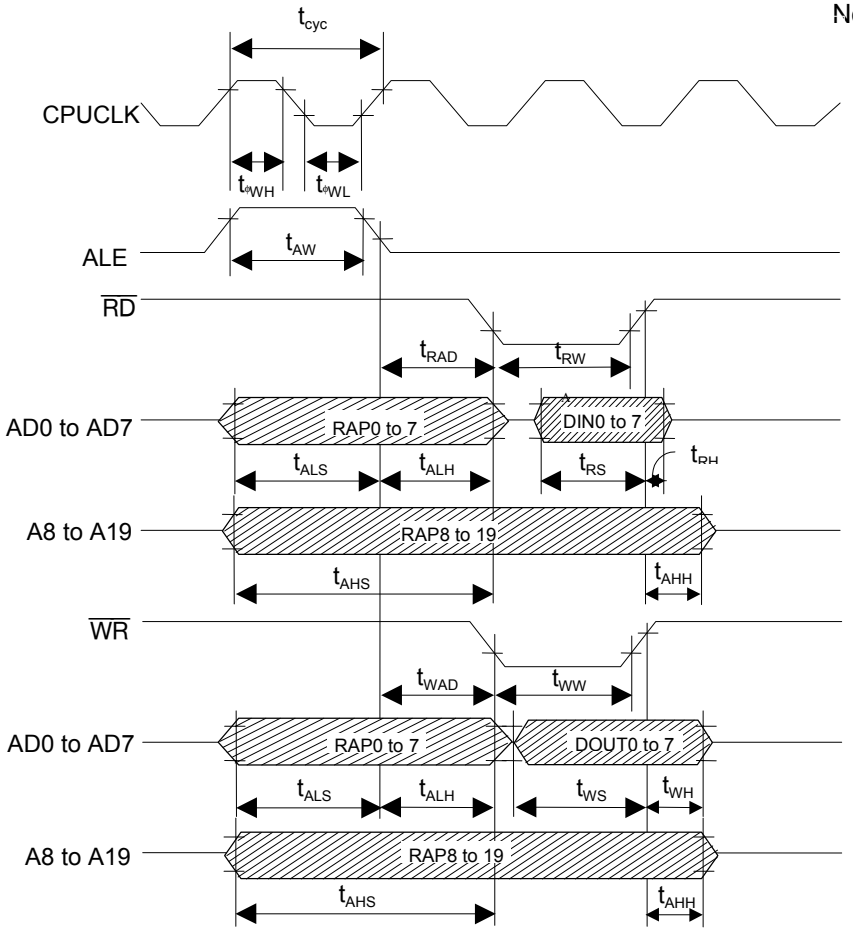
Bus timing during no wait cycle time

External data memory control

MSM66577L/579L (V_{DD} = 2.4 to 3.6 V, Ta = –30 to +70°C)
MSM66Q577L/Q579L (V_{DD} = 2.7 to 3.3 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 30 MHz	71.4	—	ns
Clock pulse width (HIGH level)	$t_{\phi WH}$	C_L = 50 pF	28	—	
Clock pulse width (LOW level)	$t_{\phi WL}$		28	—	
ALE pulse width	t_{AW}		2 tϕ – 18	—	
$\overline{RD}$ pulse width	t_{RW}		2 tϕ – 18	—	
$\overline{WR}$ pulse width	t_{WW}		2 tϕ – 18	—	
$\overline{RD}$ pulse delay time	t_{RAD}		tϕ – 6	tϕ +6	
$\overline{WR}$ pulse delay time	t_{WAD}		tϕ – 6	tϕ +6	
Low address setup time	t_{ALS}		2 tϕ – 12	2 tϕ	
Low address hold time	t_{ALH}		tϕ – 6	tϕ +6	
High address setup time	t_{AHS}		3 tϕ – 12	3 tϕ +12	
High address hold time	t_{AHH}		tϕ – 6	tϕ +6	
Read data setup time	t_{RS}		48	—	
Read data hold time	t_{RH}		0	tϕ – 6	
Write data setup time	t_{WS}		2tϕ – 24	—	
Write data hold time	t_{WH}		tϕ – 6	tϕ + 6	

Note: $t\phi = t_{cyc}/2$



Bus timing during no wait cycle time

(3) Serial port control

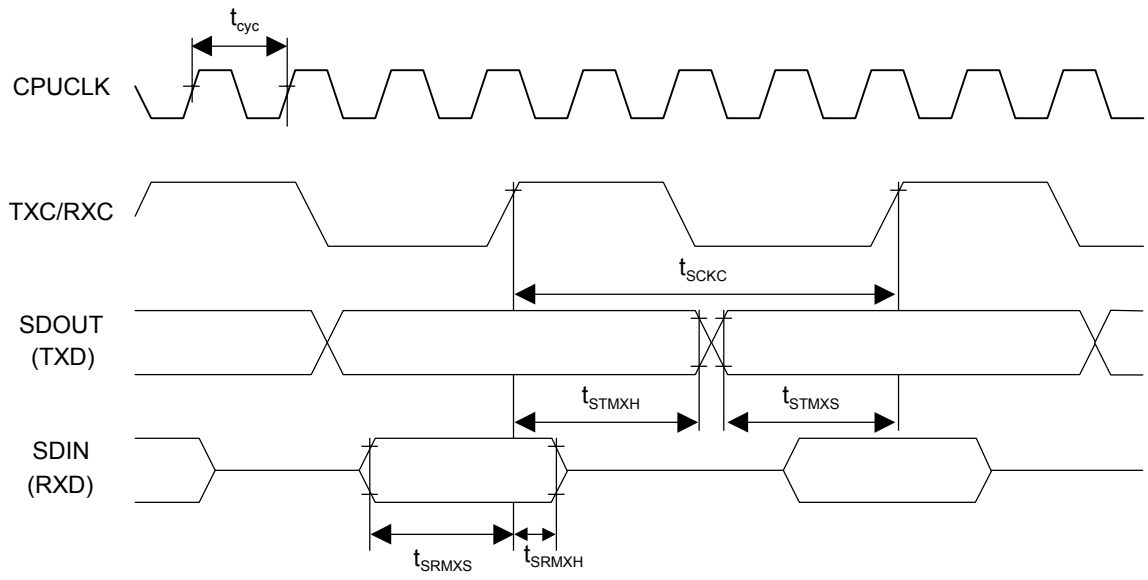
Serial ports 1 and 6 (SIO1 and 6)

Master mode (Clock synchronous serial port)

MSM66577L/579L (V_{DD} = 2.4 to 3.6 V, Ta = –30 to +70°C)
MSM66Q577L/Q579L (V_{DD} = 2.7 to 3.3 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 14 MHz	71.4	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	4 t_{cyc}	—	
Output data setup time	t_{STMXS}		2 tϕ – 10	—	
Output data hold time	t_{STMXH}		5 tϕ – 20	—	
Input data setup time	t_{SRMXS}		21	—	
Input data hold time	t_{SRMXH}		0	—	

Note: $t\phi = t_{cyc}/2$

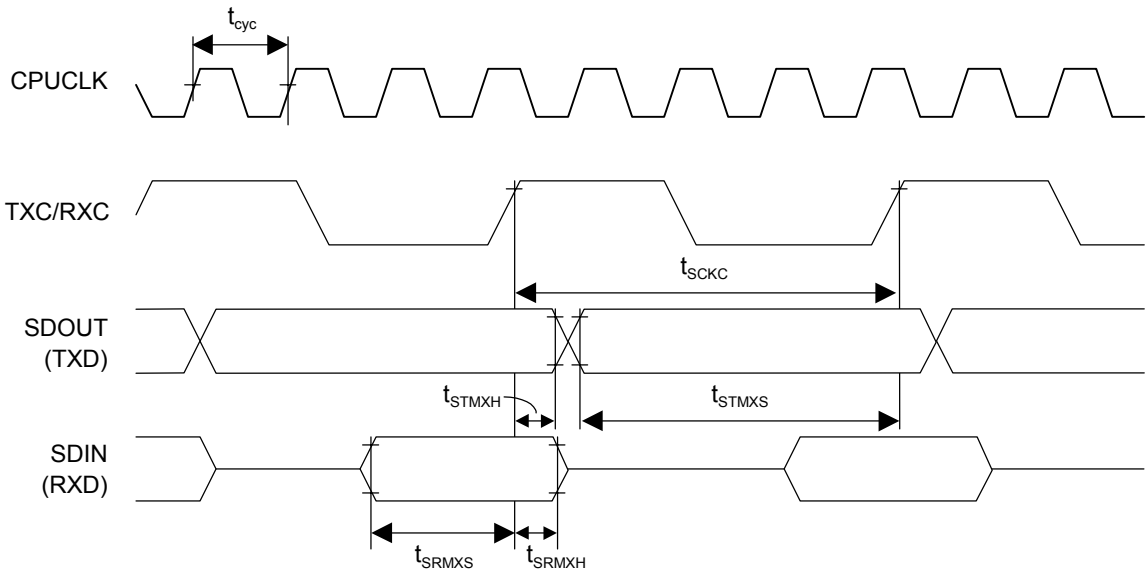


Slave mode (Clock synchronous serial port)

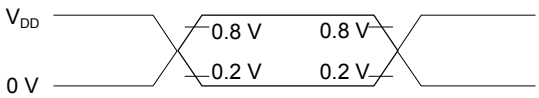
MSM66577L/579L (V_{DD} = 2.4 to 3.6 V, Ta = –30 to +70°C)
MSM66Q577L/Q579L (V_{DD} = 2.7 to 3.3 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 14 MHz	71.4	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	4 t_{cyc}	—	
Output data setup time	t_{STMXS}		2 tϕ – 30	—	
Output data hold time	t_{STMXH}		4 tϕ – 20	—	
Input data setup time	t_{SRMXS}		21	—	
Input data hold time	t_{SRMXH}		7	—	

Note: tϕ = t_{cyc}/2



Measurement points for AC timing



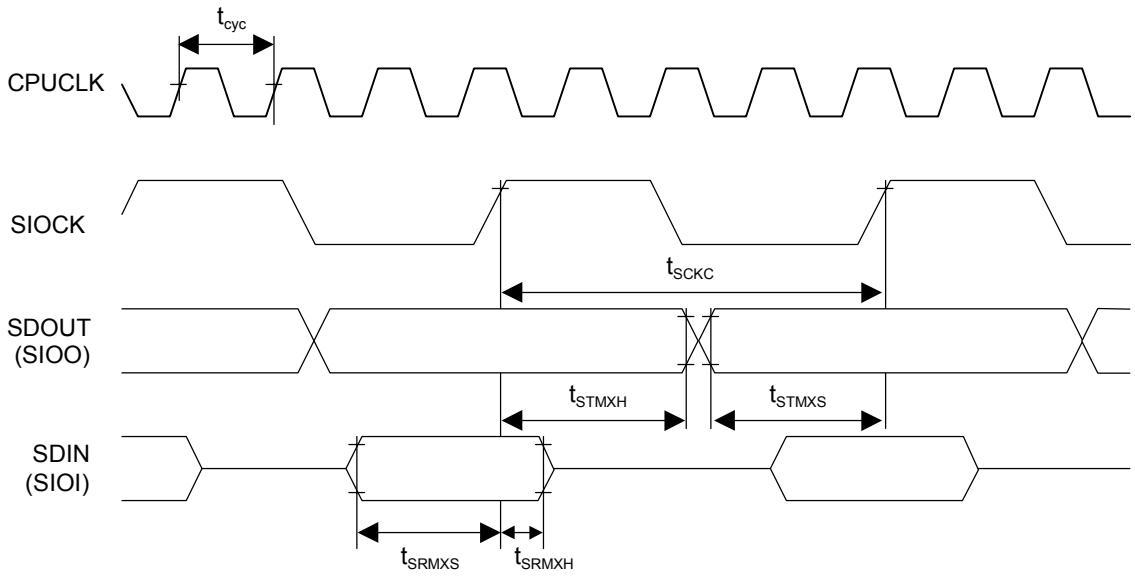
Serial ports 4 and 5 (SIO4 and 5)

Master mode (Clock synchronous serial port)

MSM66577L/ 579L (V_{DD} = 2.4 to 3.6 V, Ta = –30 to +70°C)
MSM66Q577L/Q579L (V_{DD} = 2.7 to 3.3 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 14 MHz	71.4	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	5.6 t_{cyc}	—	
Output data setup time	t_{STMXS}		5.6 tϕ – 10	—	
Output data hold time	t_{STMXH}		4.2 tϕ – 20	—	
Input data setup time	t_{SRMXS}		21	—	
Input data hold time	t_{SRMXH}		0	—	

Note: tϕ = t_{cyc}/2

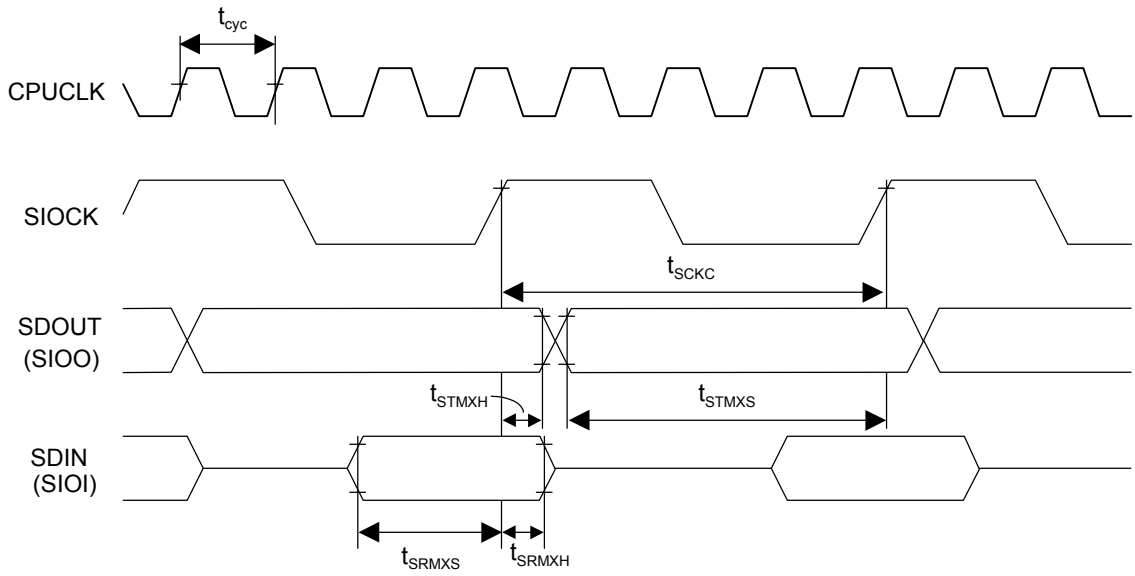


Slave mode (Clock synchronous serial port)

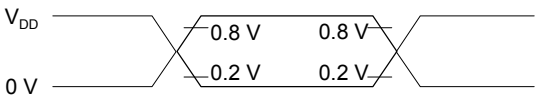
MSM66577L/579L (V_{DD} = 2.4 to 3.6 V, Ta = –30 to +70°C)
MSM66Q577L/Q579L (V_{DD} = 2.7 to 3.3 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Cycle time	t_{cyc}	f_{OSC} = 14 MHz	71.4	—	ns
Serial clock cycle time	t_{SCKC}	C_L = 50 pF	5.6 t_{cyc}	—	
Output data setup time	t_{STMXS}		2.8 $t\phi$ – 30	—	
Output data hold time	t_{STMXH}		5.6 $t\phi$ – 20	—	
Input data setup time	t_{SRMXS}		21	—	
Input data hold time	t_{SRMXH}		7	—	

Note: $t\phi = t_{cyc}/2$



Measurement points for AC timing



A/D Converter Characteristics 1 (V_{DD} = 4.5 to 5.5 V)

(Ta = –30 to 70°C, V_{DD} = V_{REF} = 4.5 to 5.5 V, AGND = GND = 0 V)

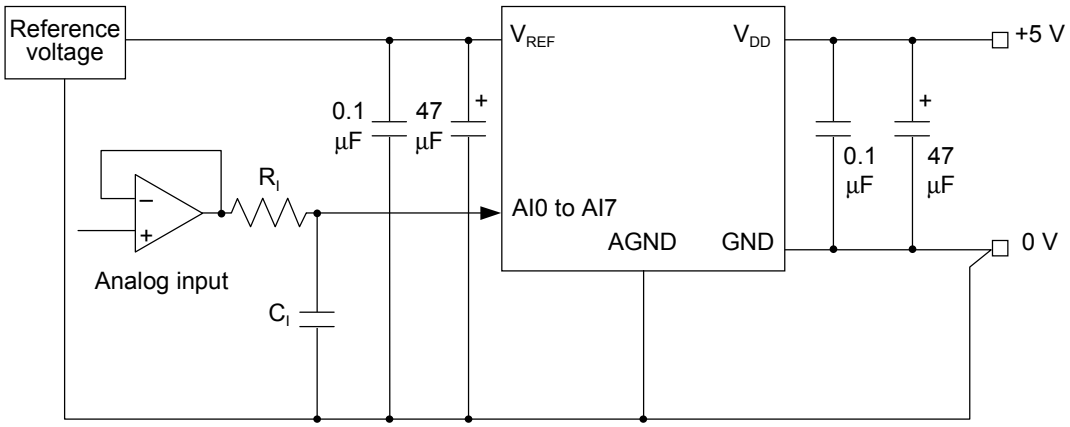
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to measurement circuit 1 Analog input source impedance $R_I \leq 5$ kΩ t_{conv} = 10.7 µs	—	10	—	Bit
Linearity error	E_L		—	—	±3	LSB
Differential linearity error	E_D		—	—	±2	
Zero scale error	E_{ZS}		—	—	+3	
Full-scale error	E_{FS}		—	—	–3	
Cross talk	E_{CT}	Refer to measurement circuit 2	—	—	±1	
Conversion time	t_{CONV}	Set according to ADTM set data	10.7	—	—	µs/ch

A/D Converter Characteristics 2 (V_{DD} = 2.4 to 3.6 V)

(Ta = –30 to 70°C, V_{DD} = V_{REF} = 2.7 to 3.6 V, AGND = GND = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to measurement circuit 1 Analog input source impedance $R_I \leq 5$ kΩ t_{conv} = 10.7 µs	—	10	—	Bit
Linearity error	E_L		—	—	±3	LSB
Differential linearity error	E_D		—	—	±2	
Zero scale error	E_{ZS}		—	—	+3	
Full-scale error	E_{FS}		—	—	–3	
Cross talk	E_{CT}	Refer to measurement circuit 2	—	—	±1	
Conversion time	t_{CONV}	Set according to ADTM set data	27.4	—	—	µs/ch

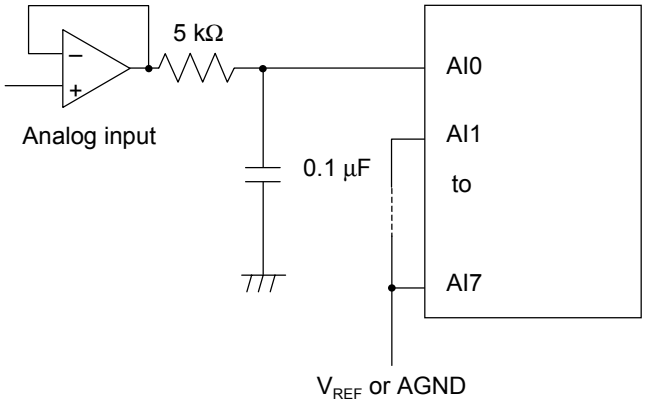
[Note] The A/D conversion time should be set according to ADTV set data. Set the number of conversion clock cycles according to frequencies of operation so that the A/D conversion time is 32 µs or more.



R_I (impedance of analog input source) ≤5 kΩ

$C_I \cong 0.1$ µF

Measurement Circuit 1



Cross talk is the difference between the A/D conversion results when the same analog input is applied to AI0 through AI7 and the A/D conversion results of the circuit to the left.

Measurement Circuit 2

Definition of Terminology

1. Resolution
   Resolution is the value of minimum discernible analog input.
   With 10 bits, since $2^{10} = 1024$, resolution of $(V_{REF} - AGND) \div 1024$ is possible.

2. Linearity error
   Linearity error is the difference between ideal conversion characteristics and actual conversion characteristics of a 10-bit A/D converter (not including quantization error).
   Ideal conversion characteristics can be obtained by dividing the voltage between V_{REF} and AGND into 1024 equal steps.

3. Differential linearity error
   Differential linearity error indicates the smoothness of conversion characteristics. Ideally, the range of analog input voltage that corresponds to 1 converted bit of digital output is $1LSB = (V_{REF} - AGND) \div 1024$. Differential error is the difference between this ideal bit size and bit size of an arbitrary point in the conversion range.

4. Zero scale error
   Zero scale error is the difference between ideal conversion characteristics and actual conversion characteristics at the point where the digital output changes from 000H to 001H.

5. Full-scale error
   Full-scale error is the difference between ideal conversion characteristics and actual conversion characteristics at the point where the digital output changes from 3FEH to 3FFH.

D/A Converter Characteristics

(V_{DD} = 2.4 to 3.6 V/4.5 to 5.5 V, Ta = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	—	—	—	8	Bit
Linearity error	E_L		—	—	1	LSB
Absolute precision	—		—	—	2	
Conversion time	t_{CONV}	C_L = 50 pF	—	20	50	µs
Analog output impedance	—	—	—	20	—	kΩ

Definition of Terminology

1. Resolution
Resolution is the value of minimum discernible analog output.
With 8 bits, since $2^8 = 256$, resolution of $(V_{DD} – GND) \div 256$ is possible.

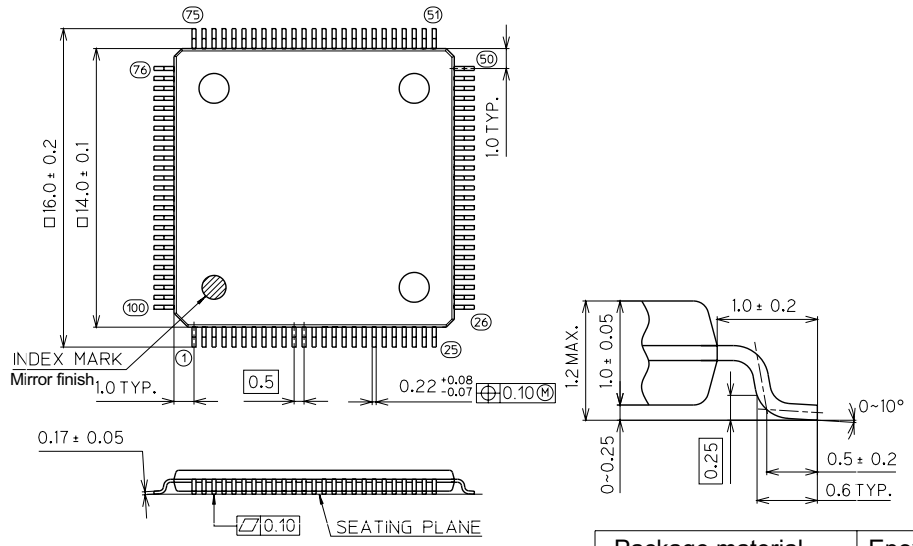
2. Linearity error
Linearity error is the difference between ideal conversion characteristics and actual conversion characteristics of an 8-bit D/A converter.
Ideal conversion characteristics can be obtained by dividing the voltage between V_{DD} and GND into 256 equal steps.

3. Differential linearity error
Differential linearity error indicates the smoothness of conversion characteristics. Ideally, the range of analog input voltage that corresponds to 1 converted bit of digital input is $1LSB = (V_{DD} – GND) \div 256$. Differential error is the difference between this ideal bit size and bit size of an arbitrary point in the conversion range.

4. Absolute precision
Absolute precision is a gross error including a linearity error and the effect of noise.

PACKAGE DIMENSIONS

TQFP100-P-1414-0.50-K



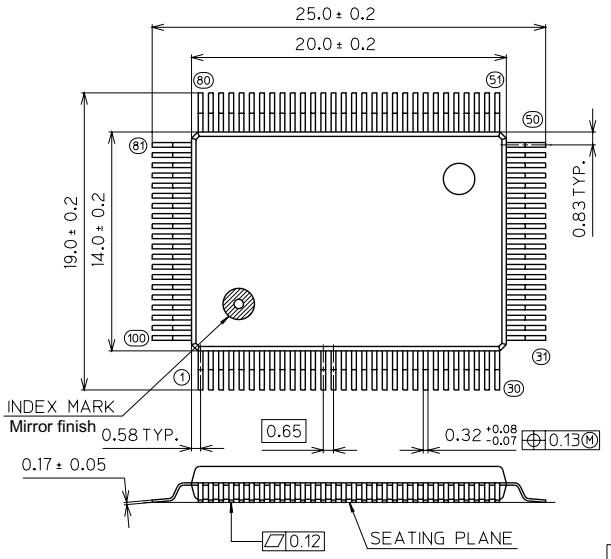
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.55 TYP.

Notes for Mounting the Surface Mount Type Packages

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit:mm)

QFP100-P-1420-0.65-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.29 TYP.

Notes for Mounting the Surface Mount Type Packages

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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