



## SPICE Device Model NTHD5905T1

Dual P-Channel 1.8 V (G-S) MOSFET

### APPLICATION NOTE

#### CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro-Model (Sub-circuit)
- Level 3 MOS
- Applicable for both Linear and Switch Mode
- Applicable over a -55 to 125°C Temperature Range
- Models Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### DESCRIPTION

The attached SPICE Model describes typical electrical characteristics of the p-channel vertical DMOS. The sub-circuit model was extracted and optimized over a 25°C to 125°C temperature range under pulse conditions for 0 to -5 volts gate drives. Saturated output impedance model accuracy has been maximized for gate biases near threshold. A novel gate-to-drain feedback capacitor network is used to model gate charge characteristics while avoiding convergence problems of switched  $C_{gd}$  model. Model parameter values are optimized to provide a best fit to measure electrical data and are not intended as an exact physical description of a device.

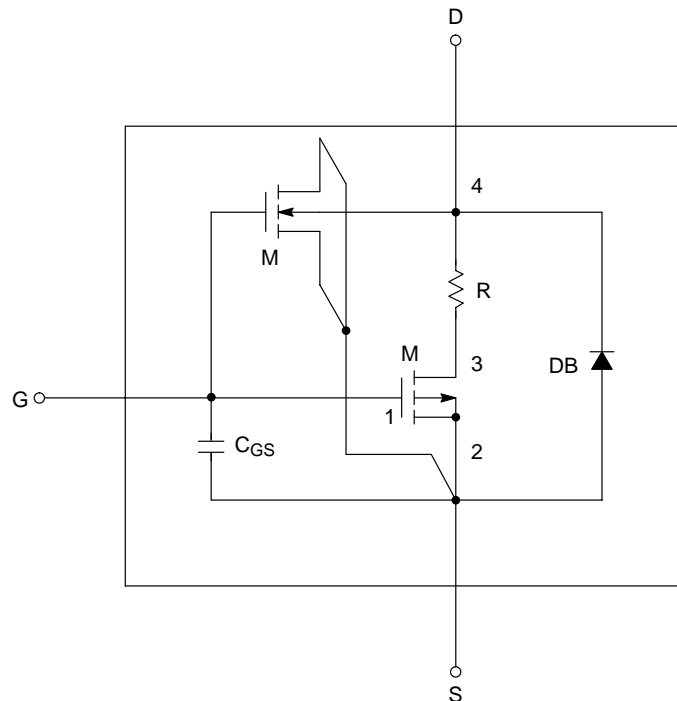


Figure 1. Model Sub-circuit

This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

# AND8048/D

## MODEL EVALUATION

**P-CHANNEL DEVICE** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Test Conditions	Typical	Unit
<b>Static</b>				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	0.83	V
On-State Drain Current (Note 1.)	$I_{D(on)}$	$V_{DS} \leq -5.0 \text{ V}, V_{GS} = 4.5 \text{ V}$	36	A
Drain-Source On-State Resistance (Note 1.)	$r_{DS(on)}$	$V_{GS} = -4.5 \text{ V}, I_D = -3.0 \text{ A}$ $V_{GS} = -2.5 \text{ V}, I_D = -2.5 \text{ A}$ $V_{GS} = -1.8 \text{ V}, I_D = -1.0 \text{ A}$	0.080 0.110 0.142	$\Omega$
Forward Transconductance (Note 1.)	$g_{fs}$	$V_{DS} = 5.0 \text{ V}, I_D = 3.0 \text{ A}$	7.6	S
Diode Forward Voltage (Note 1.)	$V_{SD}$	$I_S = -0.9 \text{ A}, V_{GS} = 0.0 \text{ V}$	-0.80	V
<b>Dynamic (Note 2.)</b>				
Total Gate Charge	$Q_g$	$V_{DS} = -4.0 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -3.0 \text{ A}$	35	nC
Gate-Source Charge	$Q_{gs}$		0.5	
Gate-Drain Charge	$Q_{gd}$		1.5	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -4.0 \text{ V}, R_L = 4.0 \Omega, I_D \cong -1.0 \text{ A},$ $V_{GEN} = -4.5 \text{ V}, R_G = 6.0 \Omega$	13	ns
Rise Time	$t_r$		19	
Turn-Off Delay Time	$t_{d(off)}$		24	
Fall Time	$t_f$		12	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = -0.9 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	28	

1. Pulse test: pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .
2. Guaranteed by design, not subject to production testing.

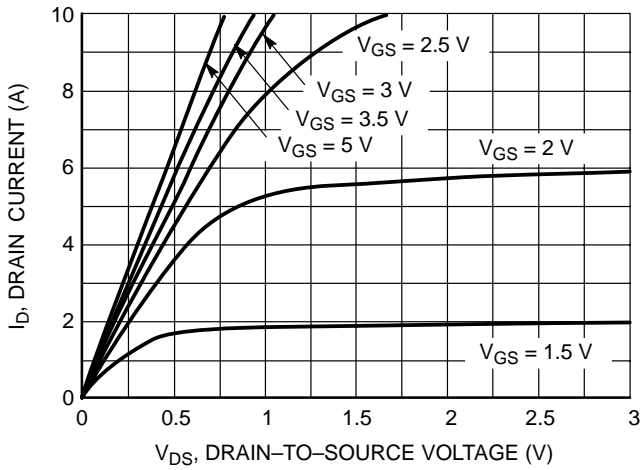


Figure 2. Drain Current vs. Drain-to-Source Voltage

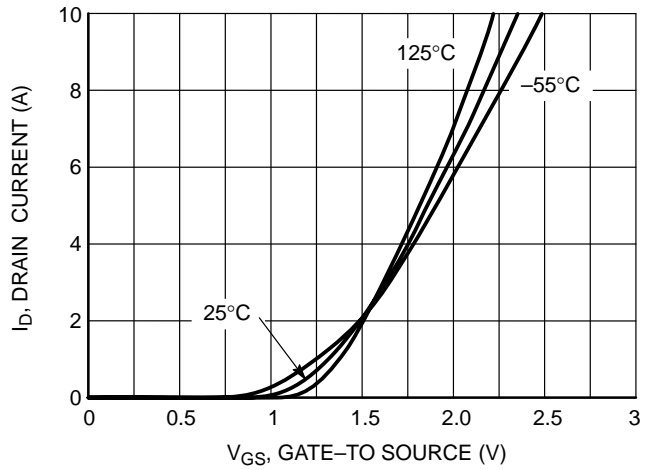


Figure 3. Drain Current vs. Gate-to-Source Voltage

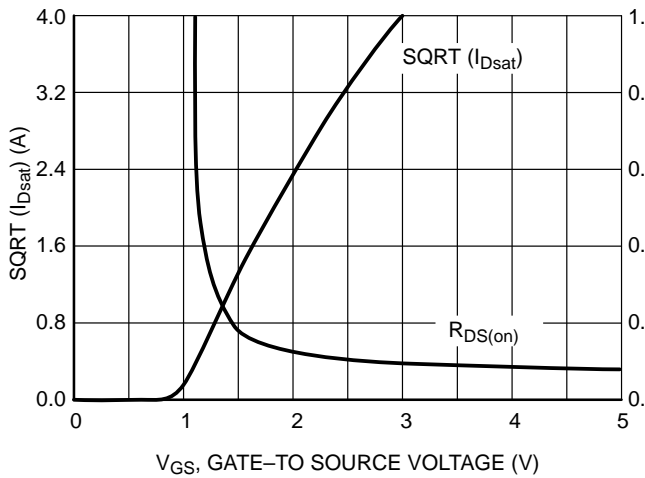


Figure 4. Sqrt vs. Gate-to-Source Voltage

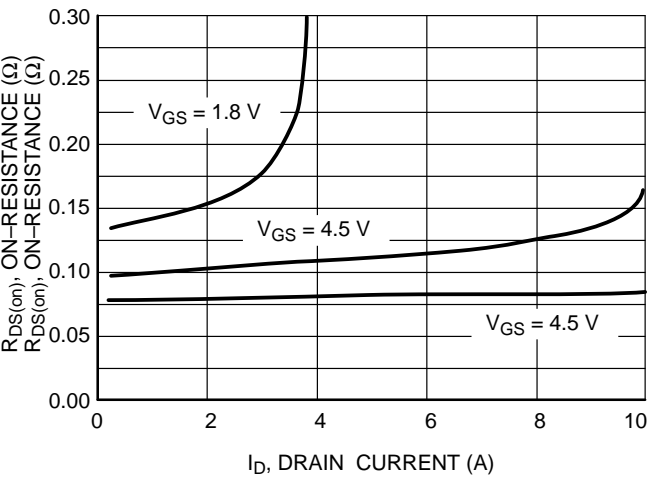


Figure 5. On-Resistance vs. Drain Current

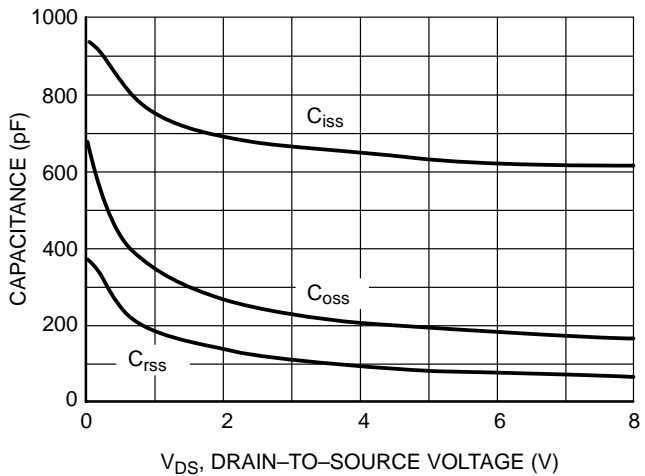


Figure 6. Capacitance vs. Drain-to-Source Voltage

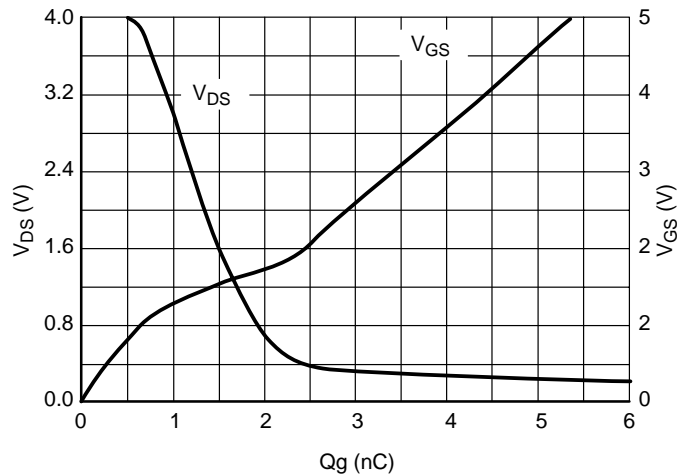


Figure 7.  $V_{DS}$  vs.  $Q_g$

# AND8048/D

## H-SPICE

```
.SUBCKT Si5905DC 4 1 2
M1 3 1 2 2 PMOS W = 183649u L = 0.50u
M1 2 1 2 4 NMOS W = 183649u L = 1.05u
R1 4 3 RTEMP 18E-3
CGS 1 2 540E-12
DBD 2 4 DBD
*****
.MODEL PMOS PMOS (LEVEL = 3 TOX = 1.7E-8
+RS = 45E-3 RD = 0 NSUB = 0.67E16
+KP = 4.7E-5 UO = 400
+VMAX = 0 XJ = 5E-7 KAPPA = 20E-3
+ETA = 1E-4 TPG = -1
+IS = 0 LD = 0 CAPOP = 5
+CGSO = 0 CGDO = 0 CGBO = 0
+TLEV = 1 BEX = -1.5 TCV = 1.5E-3
+NFS = 0.8E12 DELTA = 0.1)
*****
.MODEL NMOS NMOS (LEVEL = 3 TOX = 1.7E-8
+NSUB = 16E16 NSF = 10E11 TPG = -1)
*****
.MODEL DBD D (CJO = 200E-12 VJ = 0.38 M = 0.31
+RS = 0.6 FC = 0.5 IS = 1E-8 TT = 9E-8 N = 1 BV = 8.5)
*****
.MODEL RTEMP R (TC1 = 7.5E-3 TC2 = 5.5E-6)
*****
.ENDS
```

# AND8048/D

## P-SPICE

```
.SUBCKT Si5905DC 4 1 2
M1 3 1 2 2 PMOS W = 183649u L = 0.50u
M1 2 1 2 4 NMOS W = 183649u L = 1.05u
R1 4 3 RTEMP 18E-3
CGS 1 2 540E-12
DBD 2 4 DBD
*****
.MODEL PMOS PMOS (LEVEL = 3 TOX = 1.7E-8
+RS = 45E-3 RD = 0 NSUB = 0.67E16
+KP = 4.7E-5 UO = 400
+VMAX = 0 XJ = 5E-7 KAPPA = 20E-3
+ETA = 1E-4 TPG = -1
+IS = 0 LD = 0 CAPOP = 5
+CGSO = 0 CGDO = 0 CGBO = 0
+NFS = 0.8E12 DELTA = 0.1)
*****
.MODEL NMOS NMOS (LEVEL = 3 TOX = 1.7E-8
+NSUB = 16E16 NSF = 10E11 TPG = -1)
*****
.MODEL DBD D (CJO = 200E-12 VJ = 0.38 M = 0.31
+RS = 0.6 FC = 0.5 IS = 1E-8 TT = 9E-8 N = 1 BV = 8.5)
*****
.MODEL RTEMP R (TC1 = 7.5E-3 TC2 = 5.5E-6)
*****
.ENDS
```

# AND8048/D

## I<sub>S</sub>-SPICE

```
.SUBCKT Si5905DC 4 1 2
M1 3 1 2 2 PMOS W = 183649u L = 0.50u
M1 2 1 2 4 NMOS W = 183649u L = 1.05u
R1 4 3 18E-3 RTEMP
CGS 1 2 540E-12
DBD 2 4 DBD
*****
.MODEL PMOS PMOS (LEVEL = 3 TOX = 1.7E-8
+RS = 45E-3 RD = 0 NSUB = 0.67E16
+KP = 4.7E-5 UO = 400
+VMAX = 0 XJ = 5E-7 KAPPA = 20E-3
+ETA = 1E-4 TPG = -1
+IS = 0 LD = 0 CAPOP = 5
+CGSO = 0 CGDO = 0 CGBO = 0
+NFS = 0.8E12 DELTA = 0.1)
*****
.MODEL NMOS NMOS (LEVEL = 3 TOX = 1.7E-8
+NSUB = 16E16 NSF = 10E11 TPG = -1)
*****
.MODEL DBD D (CJO = 200E-12 VJ = 0.38 M = 0.31
+RS = 0.6 FC = 0.5 IS = 1E-8 TT = 9E-8 N = 1 BV = 8.5)
*****
.MODEL RTEMP R (TC1 = 7.5E-3 TC2 = 5.5E-6)
*****
.ENDS
```

## Notes

**ON Semiconductor** and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com  
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**EUROPE:** LDC for ON Semiconductor – European Support

**German Phone:** (+1) 303-308-7140 (Mon-Fri 2:30pm to 7:00pm CET)  
**Email:** ONlit-german@hibbertco.com  
**French Phone:** (+1) 303-308-7141 (Mon-Fri 2:00pm to 7:00pm CET)  
**Email:** ONlit-french@hibbertco.com  
**English Phone:** (+1) 303-308-7142 (Mon-Fri 12:00pm to 5:00pm GMT)  
**Email:** ONlit@hibbertco.com

**EUROPEAN TOLL-FREE ACCESS\*: 00-800-4422-3781**

\*Available from Germany, France, Italy, UK, Ireland

### CENTRAL/SOUTH AMERICA:

**Spanish Phone:** 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)  
**Email:** ONlit-spanish@hibbertco.com  
**Toll-Free from Mexico:** Dial 01-800-288-2872 for Access –  
then Dial 866-297-9322

**ASIA/PACIFIC:** LDC for ON Semiconductor – Asia Support

**Phone:** 1-303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)  
**Toll Free from Hong Kong & Singapore:**  
**001-800-4422-3781**  
**Email:** ONlit-asia@hibbertco.com

**JAPAN:** ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031  
**Phone:** 81-3-5740-2700  
**Email:** r14525@onsemi.com

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local Sales Representative.