

4MB SYNCHRONOUS CARD EDGE DIMM

FEATURES

- 4x128Kx64 Synchronous
- Access Speed(s): $T_{KHQV} = 9.5, 10, 11, 12, 15ns$
- Flow-Through Architecture
- Clock Controlled Registered Bank Enables (E1#, E2#, E3#, E4#)
- Clock Controlled Registered Address
- Clock Controlled Registered Global Write (GW#)
- Aynchronous Output Enable (G#)
- Internally self-timed Write
- Gold Lead Finish
- 3.3V $\pm 10\%$, -5% Operation
- Access Speed(s): $t_{KHQV} = 9.5, 10, 11, 12, 15ns$
- Common Data I/O
- High Capacitance (30pf) drive, at rated Access Speed
- Single total array Clock
- Multiple Vcc and GND

DESCRIPTION

The EDI2KG64128VxxD is a Synchronous SRAM, 60 position Card Edge DIMM (120 contacts) Module, organized as 4x128Kx64. The Module contains eight (8) Synchronous Burst Ram Devices, packaged in the industry standard JEDEC 14mmx20mm TQFP placed on a Multilayer FR4 Substrate. The module architecture is defined as a Synchronous Only, Flow-Through, Early Write Device. This module provides High Performance, Ultra Fast access times at a cost per bit benefit over BiCMOS Asynchronous SRAM based devices. As well as improved cost per bit, the use of Synchronous or Synchronous Burst devices or modules can ease the memory subsystem design by reducing or easing the memory controller requirement.

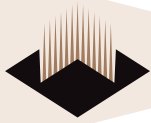
Synchronous operations are in relation to an externally supplied clock, Registered Address, Registered Global Write, Registered Enables as well as an Asynchronous Output enable. All read and write operations to this module are performed on Quad Words (64 bit operations).

Write cycles are internally self timed and are initiated by a rising clock edge. This feature relieves the designer the task of developing external write pulse width circuitry.

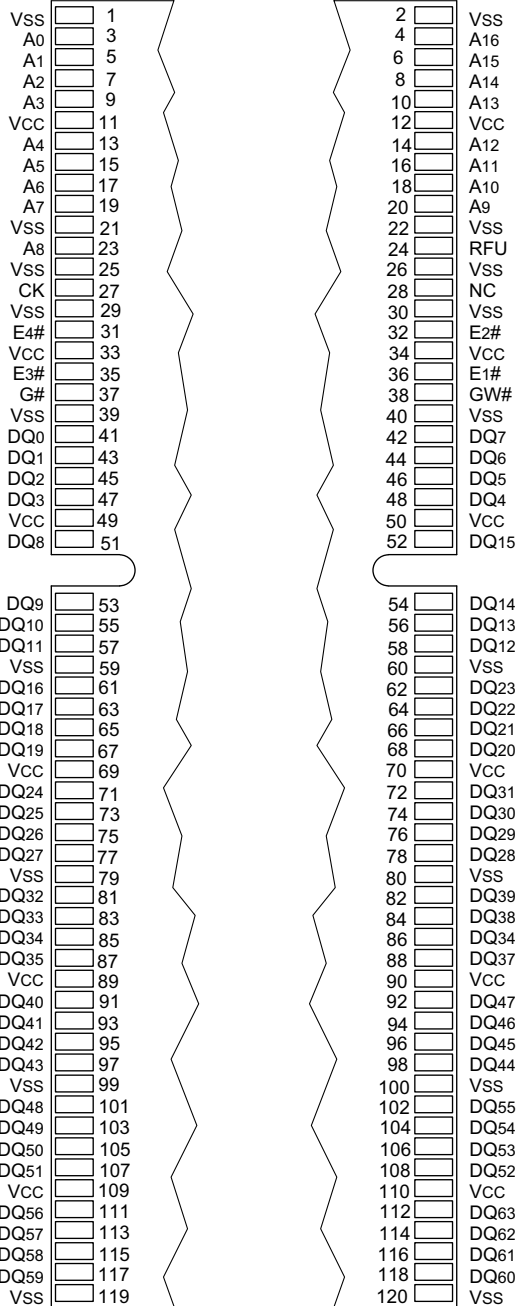
PIN NAMES

DQ0-DQ63	Input/Output Bus
A015	Address Bus
E1#, E2#, E3#, E4#	Synchronous Bank Enables
CK	Array Clock
GW#	Synchronous Global Write Enable
G#	Asynchronous Output Enable
Vcc	3.3V Power Supply
Vss	Ground
NC	No Connect

*This product is subject to change without notice.

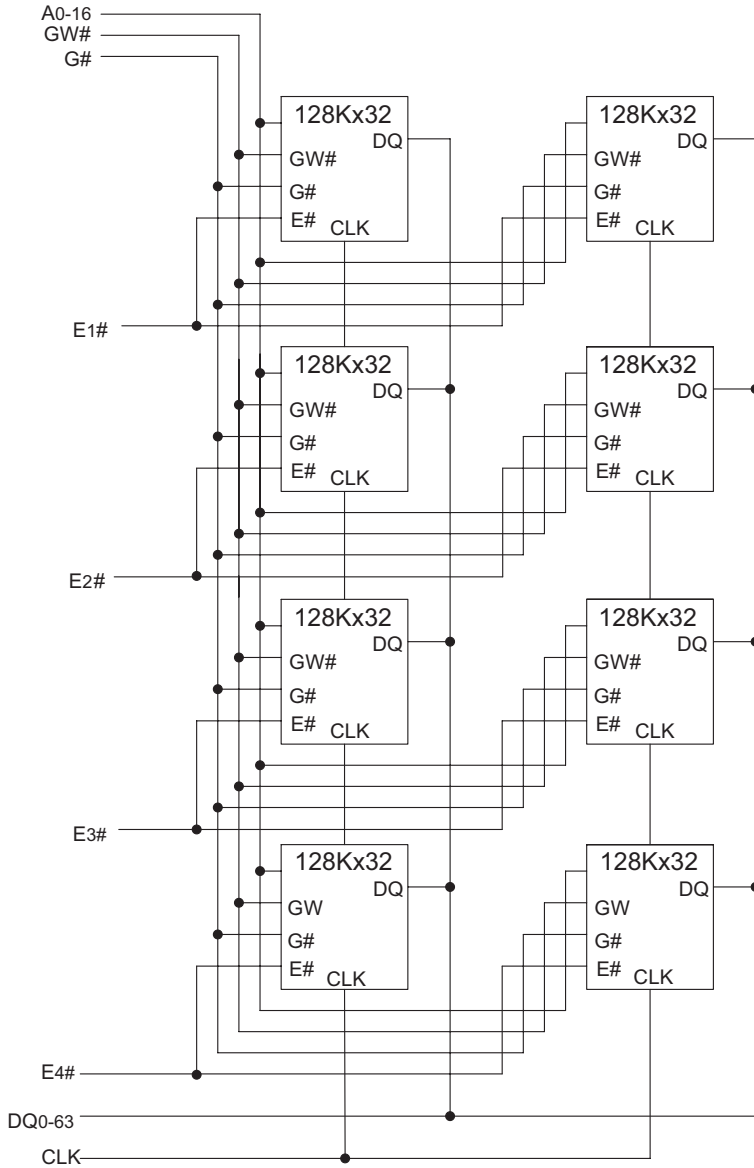


PIN CONFIGURATION





FUNCTIONAL BLOCK DIAGRAM



**PIN DESCRIPTIONS**

DIMM Pins	Symbol	Type	Description
3, 5, 7, 9, 13, 15, 17, 19, 20, 23, 18, 16, 14, 10, 8, 6	A0-A15	Input Synchronous	Addresses: These inputs are registered and must meet the setup and hold times around the rising edge of CK. The burst counter generates internal addresses associated with A ₀ and A ₁ , during burst and wait cycle.
38	GW#	Input Synchronous	Global Write: This active LOW input allows a full 72-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CK.
27	CK	Input Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
36, 32, 35, 31	E1#, E2# E3#, E4#	Input Synchronous	Bank Enables: These active LOW inputs are used to enable each individual Synchronous bank and to gate ADSP#.
37	G#	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
Various	DQ0-63	Input/Output	Data Inputs/Outputs: First byte is DQ ₀₋₇ , second byte is DQ ₈₋₁₅ , third byte is DQ ₁₆₋₂₃ , fourth byte is DQ ₂₄₋₃₁ , fifth byte is DQ ₃₂₋₃₉ , sixth byte is DQ ₄₀₋₄₇ , seventh byte is DQ ₄₈₋₅₅ and the eight byte is DQ ₅₆₋₆₄ .
Various	Vcc	Supply	Core power supply: +3.3V -5%/+10%
Various	Vss	Ground	Ground



SYNCHRONOUS ONLY – TRUTH TABLE

Operation	E1#	E2#	E3#	E4#	GW#	G#	CK	DQ
Synchronous Write-Bank 1	L	H	H	H	L	H	↑	High-Z
Synchronous Read-Bank 1	L	H	H	H	H	L	↑	
Synchronous Write-Bank 2	H	L	H	H	L	H	↑	High-Z
Synchronous Read-Bank 2	H	L	H	H	H	L	↑	
Synchronous Write-Bank 3	H	H	L	H	L	H	↑	High-Z
Synchronous Read-Bank 3	H	H	L	H	H	L	↑	
Synchronous Write-Bank 4	H	H	H	L	L	H	↑	High-Z
Synchronous Read-Bank 4	H	H	H	L	H	L	↑	
Snooze Mode	X	X	X	X	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Relative to Vss	-0.5V to +4.6V
V _{IN}	-0.5V to Vcc +0.5V
Storage Temperature	-55°C to +125°C
Operating Temperature (Commercial)	0°C to +70°C
Operating Temperature (Industrial)	-40°C to +85°C
Short Circuit Output Current	20 mA

* Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

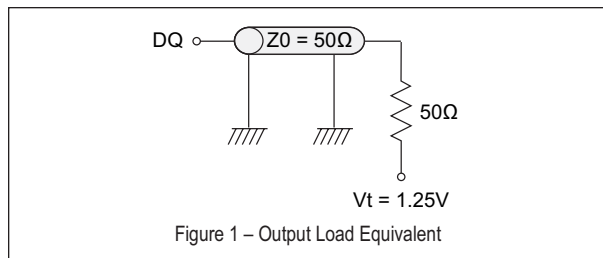
Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V _{CC}	3.14	3.3	3.6	V
Supply Voltage	V _{SS}	0.0	0.0	0.0	V
Input High	V _{IH}	2.2	3.0	V _{CC} + 0.3	V
Input Low	V _{IL}	-0.3	0.0	0.8	V
Input Leakage	I _{LI}	-2	1	2	μA
Output Leakage	I _{LO}	-2	1	2	μA
Output High I _{OH} = -4ma	V _{OH}	2.4	-	-	V
Output Low I _{OL} = 8ma	V _{OL}	-	-	0.4	V

DC ELECTRICAL CHARACTERISTICS – READ CYCLE

Description	Symbol	Typ	Max					Units
			9.5	10	11	12	15	
Power Supply Current	I _{CC1}	1.55	2.8	2.2	2.2	2.7	2.0	A
Power Supply Current Device Selected, No Operation	I _{CC}	.75	1.8	1.5	1.3	1.3	1.0	A
Snooze Mode	I _{CCZZ}	200	300	300	300	300	300	mA
CMOS Standby	I _{CC3}	400	500	500	500	500	500	mA
Clock Running-Deselect	I _{CCK}	600	900	900	900	900	900	mA

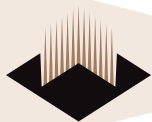
*TBD

AC TEST LOAD



AC TEST CONDITIONS

Parameter	I/O	Unit
Input Pulse Levels	V _{SS} to 3.0V	V
Input and Output Timing Ref.	1.25	V
Output Test Equivalencies	See figure at left	V



READ CYCLE TIMING PARAMETERS

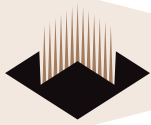
Description	Sym	9.5ns		10ns		11ns		12ns		15ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Cycle Time	t _{KHKH}	*	*	12		12		15		20		ns
Clock High Time	t _{KHKL}	*	*	5		5		5		6		ns
Clock Low Time	t _{KLKH}	*	*	5		5		5		6		ns
Clock to Output Valid	t _{KHQV}	*	*		10		11		12		15	ns
Clock to Output Invalid	t _{KHQX1}	*	*	3		3		3		3		ns
Clock to Output Low-Z	t _{KHQX}	*	*	2		2		2		2		ns
Output Enable to Output Valid	t _{GLQV}	*	*		4		5		5		6	ns
Output Enable to Output Low-Z	t _{GLQX}	*	*	0		0		0		0		ns
Output Enable to Output High-Z	t _{GHQZ}	*	*		4		5		5		5	ns
Address Setup	t _{AVKH}	*	*	2.5		2.5		2.5		2.5		ns
Bank Enable Setup	t _{EVKH}	*	*	2.5		2.5		2.5		2.5		ns
Address Hold	t _{KHAX}	*	*	1.0		1.0		1.0		1.0		ns
Bank Enable Hold	t _{KHEX}	*	*	1.0		1.0		1.0		1.0		ns

*TBD

WRITE CYCLE TIMING PARAMETERS

Description	Sym	9.5ns		10ns		11ns		12ns		15ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Cycle Time	t _{KHKH}	*	*	12		12		15		20		ns
Clock High Time	t _{KHKL}	*	*	5		5		5		6		ns
Clock Low Time	t _{KLKH}	*	*	5		5		5		6		ns
Address Setup	t _{AVKH}	*	*	2.5		2.5		2.5		2.5		ns
Address Hold	t _{KHAX}	*	*	1.0		1.0		1.0		1.0		ns
Bank Enable Setup	t _{EVKH}	*	*	2.5		2.5		2.5		2.5		ns
Bank Enable Hold	t _{KHEX}	*	*	1.0		1.0		1.0		1.0		ns
Global Write Enable Setup	t _{WVKH}	*	*	2.5		2.5		2.5		2.5		ns
Global Write Enable Hold	t _{KHWX}	*	*	1.0		1.0		1.0		1.0		ns
Data Setup	t _{DVKH}	*	*	2.5		2.5		2.5		2.5		ns
Data Hold	t _{KHDX}	*	*	1.0		1.0		1.0		1.0		ns

*TBD

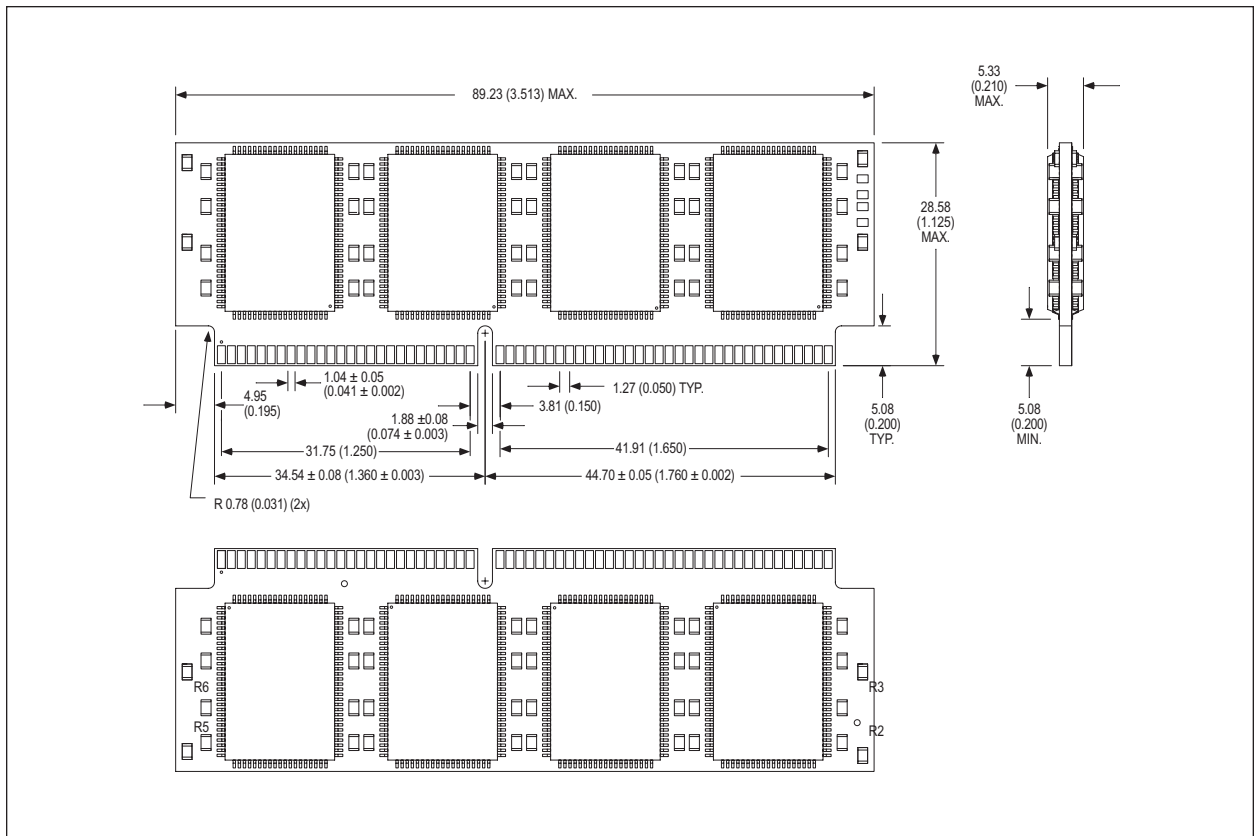


ORDERING INFORMATION

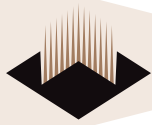
Part Number	Organization	Voltage	Speed (ns)	Package	Height*
EDI2GG464128V95D*	4x128Kx64	3.3	9.5	120 Card Edge DIMM	28.58 (1.125")
EDI2GG464128V10D*	4x128Kx64	3.3	10	120 Card Edge DIMM	28.58 (1.125")
EDI2GG464128V11D	4x128Kx64	3.3	11	120 Card Edge DIMM	28.58 (1.125")
EDI2GG464128V12D	4x128Kx64	3.3	12	120 Card Edge DIMM	28.58 (1.125")
EDI2GG464128V15D*	4x128Kx64	3.3	15	120 Card Edge DIMM	28.58 (1.125")

*Consult Factory for Availability

PACKAGE DESCRIPTION: 120 LEAD CARD EDGE DIMM



ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES).



Document Title

4MB SYNCHRONOUS CARD EDGE DIMM

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	July 1999	
Rev 1	Corrected block diagram specs	10-25-04	