Ordering number : ENA0910

SANYO Semiconductors
DATA SHEET

LA73074CL — Monolithic Linear IC
Video Driver for DSC/Cell Phone

Overview

The LA73074CL is a low voltage drive (2.7V to 3.6V) video driver developed for portable appliances including digital still cameras and cell phones. It incorporates a minus-voltage generator that allows the LA73074CL to generate its output with the pedestal voltage set to 0V, so that no output coupling capacitor is required. This enables substantial reduction in mounting space without concerned about V-sag.

Features

- Output coupling capacity not required
- Low-voltage drive (V_{CC} = 2.7V to 3.6V)
- No V-sag
- Sextic LPF incorporated (fc = 7.5MHz)
- Current drain of 0μA in the standby mode
- Amplifier gain selectable from three options (6, 12, and 9dB) (Pin control (GND/Open/V_{CC}))
- Output drive capable of covering maximum 75Ω output, one channel

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		4.0	V
Allowable power dissipation	Pd max	Ta ≤ 80°C, *Mounted on a specified board	160	mW
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

*: Mounted on a specified board: 10mm×20mm×0.8mm, Paper phenol

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Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended Operating supply voltage	V_{CC}STD		3.1	V
Operating supply voltage range	V_{CC}RANGE		2.7 to 3.6	V

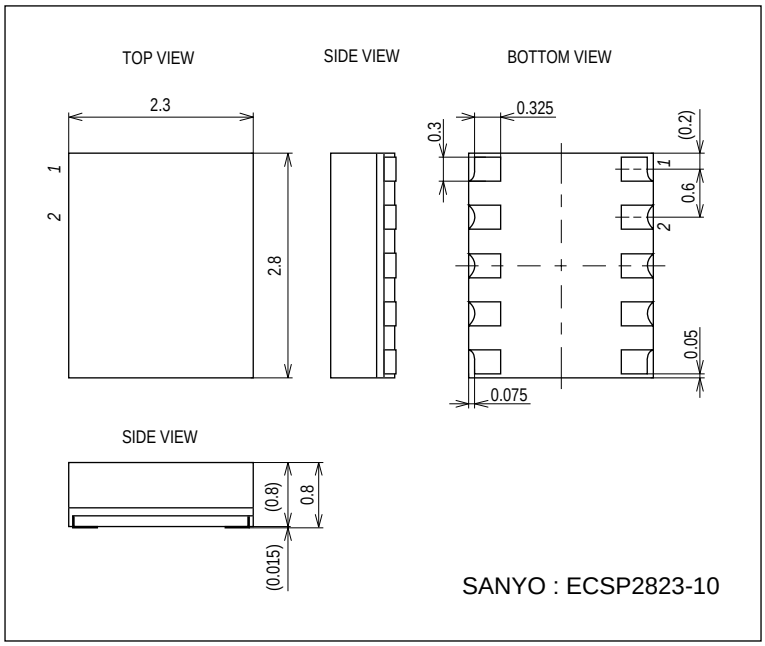
Electrical Characteristics at Ta = 25°C, V_{CC} = 3.1V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current Drain Block						
Current dissipation 1 (V_{IN} = White50%)	I_{CC}	4pin = Low Input = White50%	14	22	30	mA
Current dissipation 2 (Non-signal mode)	$I_{CC}2$	4pin = Low Input = No signal	7	11.5	15	mA
Current dissipation 3 (Standby mode)	I_{CC}-STBY	4pin = Open (High)		0	5	μA
Video Block						
Voltage gain V6	V_{G-L}	V_{IN} = 1Vp-p 100% white 2pin = Low (GND)	5.7	6.2	6.7	dB
Voltage gain V12	V_{G-M}	V_{IN} = 0.5Vp-p 100% white 2pin = MID (Open)	11.7	12.2	12.7	dB
Voltage gain V9	V_{G-H}	V_{IN} = 710mVp-p 100% white 2pin = High (V_{CC})	8.7	9.2	9.7	dB
Freq. Characteristics	V_f	f = 100kHz/5MHz	-1.5	-0.5	+0.5	dB
Differential Gain	D_G	V_{OUT} = 2Vp-p (Modulated Ramp)	-2.0	0	-2.0	%
Differential Phase	D_P	V_{OUT} = 2Vp-p (Modulated Ramp)	-2.0	0	-2.0	deg
Output leak current at standby 1	$I_{OUT}H$	Leak current when 3V is applied to pin 9, with pin 4 at H (Standby Mode) and pin 9 (V_{OUT})	-5.0	0	+5.0	μA
Output leak current at standby 2	$I_{OUT}L$	Leak current when 0.1V is applied to pin 9, with pin 4 at H (Standby Mode) and pin 9 (V_{OUT})	-5.0	0	+5.0	μA
Control Terminal Block						
Stand-by control pin H voltage (SET = STANDBY MODE)	$V_{TH-STBY-H}$	Pin 4 pin voltage range at which $I_{CC} \leq 5\mu A$	V_{CC}-0.5		3.6	V
Stand-by control pin L voltage (SET = ACTIVE MODE)	$V_{TH-STBY-L}$	Pin 4 pin voltage range at which the operation mode is effective.	GND		0.3	V
Gain selection control pin H voltage (SET = 9dB)	V_{TH-G-H}	Pin 2 pin voltage range at which Amp Gain becomes 9dB.	V_{CC}-0.3		V_{CC}	V
Gain selection control pin M voltage (SET = 12dB)	V_{TH-G-M}	Pin 2 pin voltage range at which Amp Gain becomes 12dB.	1.0	1.2 (OPEN)	1.4	V
Gain selection control pin L voltage (SET = 6dB)	V_{TH-G-L}	Pin 2 pin voltage range at which Amp Gain becomes 6dB.	GND		0.3	V

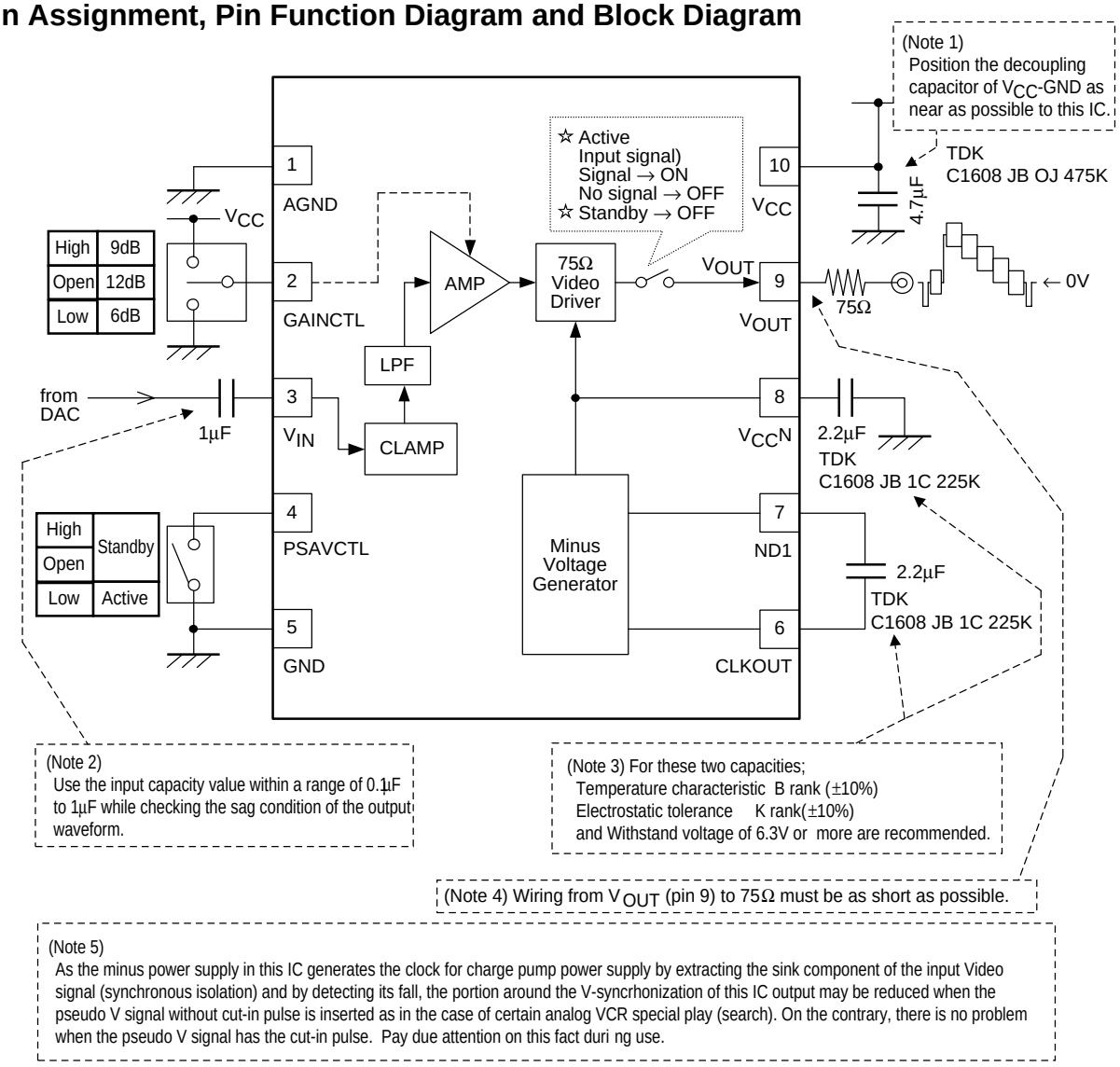
Package Dimensions

unit : mm (typ)

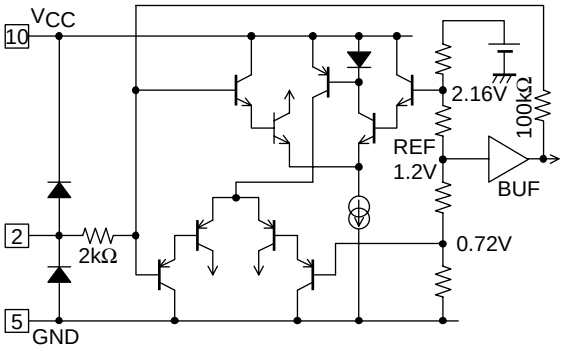
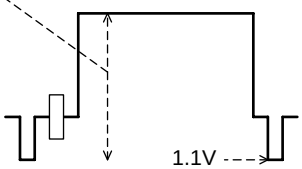
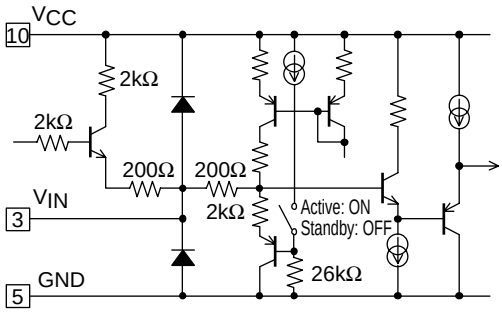
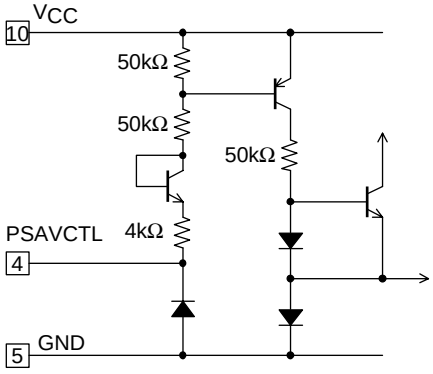
3334



Pin Assignment, Pin Function Diagram and Block Diagram



Pin Functions

<table>
<tr><th>Pin No</th><th>Symbol</th><th>Voltage</th><th>Description</th><th>Equivalent Circuit</th></tr>
<tr><td>1</td><td>AGND</td><td>0V</td><td>Analog GND</td><td></td></tr>
<tr><td>2</td><td>GAINCTL</td><td>1.2V</td><td>Gain select pin
<table><tr><td>Control of Pin2</td><td></td><td>GAIN</td></tr><tr><td>H(V_{CC})</td><td>⇒</td><td>9dB</td></tr><tr><td>M(OPEN)</td><td>⇒</td><td>12dB</td></tr><tr><td>L(GND)</td><td>⇒</td><td>6dB</td></tr></table></td><td> 
</td></tr>
<tr><td>3</td><td>V_{IN}</td><td>1.1V</td><td>Video input pin
(Sync-chip clamp
(input High-impedance))
GAIN SET: 6dB⇒1.0Vp-p
GAIN SET: 12dB⇒500mVp-p
GAIN SET: 9dB⇒710mVp-p
 
</td><td> 
</td></tr>
<tr><td>4</td><td>PSAVCTL</td><td>V_{CC}
or
0V</td><td>Power save mode select pin
<table><tr><td>Control of Pin4</td><td></td><td></td><td>MODE</td></tr><tr><td>H(V_{CC})</td><td>OPEN
or
V_{CC}±0.5V</td><td>⇒</td><td>STANDBY</td></tr><tr><td>L(GND)</td><td>0V to 0.3V</td><td>⇒</td><td>ACTIVE</td></tr></table></td><td> 
</td></tr>
<tr><td>5</td><td>GND</td><td>0V</td><td></td><td></td></tr>
</table>

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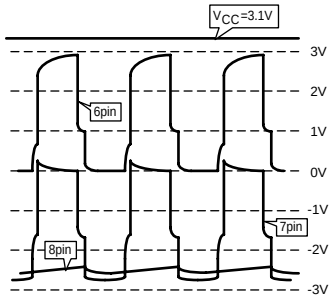
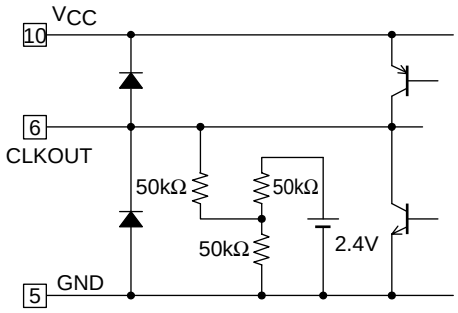
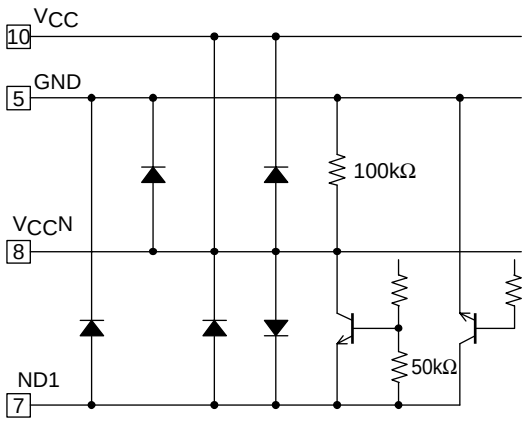
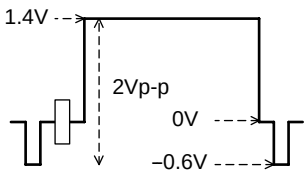
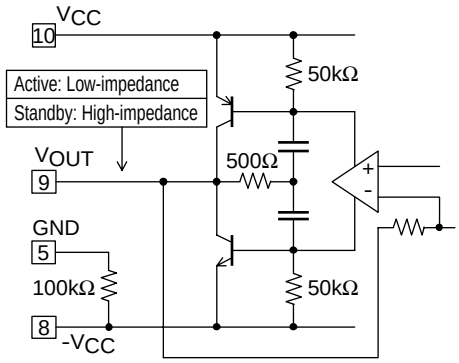
Pin No	Symbol	Voltage	Description	Equivalent Circuit
6	CLKOUT	+3.0V ↑↓ 0V	Pin : Clock output terminal 	
7	ND1	+0.5V ↑↓ -2.6V (-V_{CC})	Pin7 : The terminal which transmits an electric charge	
8	$V_{CC}N$	0V ↑↓ -2.5V (-V_{CC})	Pin8 : Negative V_{CC}	
9	V_{OUT}	0V	Video output terminal (Push-pull output Low-impedance) 	
10	V_{CC}	2.9V to 3.6V		

Test Circuit Diagram