FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21379-1E

ASSP

Single Serial Input PLL Frequency Synthesizer On-chip 3.0 GHz Prescaler

MB15E06SR

■ DESCRIPTION

The Fujitsu MB15E06SR is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 3.0 GHz prescaler. The 3.0 GHz prescaler has a dual modulus division ratio of 64/65 or 128/129 enabling pulse swallowing operation.

The supply voltage range is between 2.7 V and 4.0 V. A refined charge pump supplies well-balanced output currents of 4.0 mA.

The phase noise of MB15E06SR was drastically improved comparing with the former single PLL, MB15E06. The data format of serial data and the pin assignments except for ϕP and ϕR pins are same as the former one, so it is easy to replace the former one.

MB15E06SR is ideally suited for the high frequency wireless system such as ETC (Electronic Toll Collection System).

■ FEATURES

- High frequency operation: 3.0 GHz Max
- Low power supply voltage: V_{CC} = 2.7 V to 4.0 V
- Ultra Low power supply current: I_{CC} = 8.0 mA Typ (V_{CC} = Vp = 3.0 V, Ta = +25°C, in locking state)
- Direct power saving function: Power supply current in power saving mode
  Typ 0.1 µA (V_{CC} = Vp = 3.0 V, Ta = +25°C)

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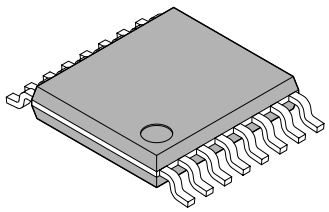
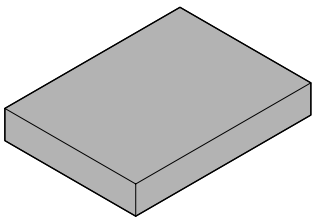
■ PACKAGES

16-pin plastic TSSOP



(FPT-16P-M07)

16-pad plastic BCC



(LCC-16P-M06)

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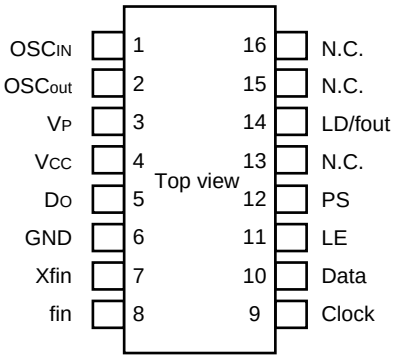
- Dual modulus prescaler: 64/65 or 128/129
- Serial input 14-bit programmable reference divider: R = 3 to 16,383
- Serial input programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 3 to 2,047
- Software selectable charge pump current
- On-chip phase control for phase comparator
- Built-in digital locking detector circuit to detect PLL locking and unlocking.
- Operating temperature: Ta = –40 °C to +85 °C

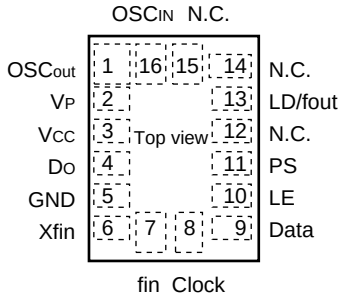
■ PIN ASSIGNMENTS

16-pin TSSOP



(FPT-16P-M07)

16-pad BCC

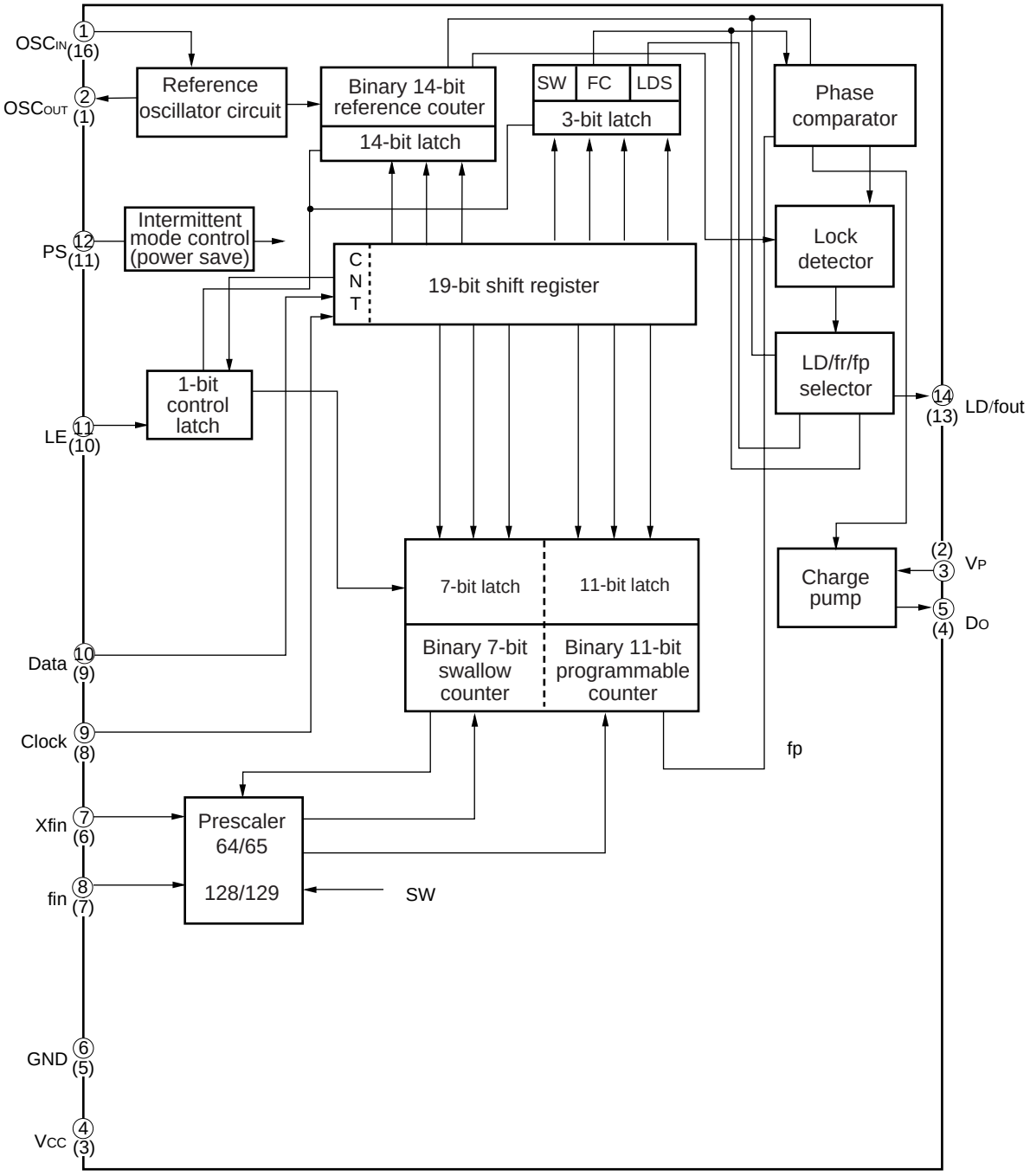


(LCC-16P-M06)

■ PIN DESCRIPTIONS

Pin no.		Pin name	I/O	Descriptions
TSSOP	BCC			
1	16	OSC_{IN}	I	Programmable reference divider input. Connection to a TCXO.
2	1	OSC_{OUT}	O	Oscillator output.
3	2	V_P	–	Power supply voltage input for the charge pump.
4	3	V_{CC}	–	Power supply voltage input.
5	4	D_O	O	Charge pump output. Phase of the charge pump can be selected via programming of the FC bit.
6	5	GND	–	Ground.
7	6	Xfin	I	Prescaler complementary input, which should be grounded via a capacitor.
8	7	fin	I	Prescaler input. Connection to an external VCO should be done via AC coupling.
9	8	Clock	I	Clock input for the 19-bit shift register. Data is shifted into the shift register on the rising edge of the clock. (Open is prohibited.)
10	9	Data	I	Serial data input using binary code. The last bit of the data is a control bit. (Open is prohibited.)
11	10	LE	I	Load enable signal input. (Open is prohibited.) When LE is set high, the data in the shift register is transferred to a latch according to the control bit in the serial data.
12	11	PS	I	Power saving mode control. This pin must be set at “L” at Power-ON. (Open is prohibited.) PS = “H”; Normal mode PS = “L”; Power saving mode
13	12	N.C.	–	No connection.
14	13	LD/fout	O	Lock detect signal output (LD)/phase comparator monitoring output (fout). The output signal is selected via programming of the LDS bit. LDS = “H”; outputs fout (fr/fp monitoring output) LDS = “L”; outputs LD (“H” at locking, “L” at unlocking.)
15	14	N.C.	–	No connection.
16	15	N.C.	–	No connection.

■ BLOCK DIAGRAM



○ : TSSOP
( ) : BCC

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit	Remark
			Min	Max		
Power supply voltage	V_{CC}	–	–0.5	5.0	V	
	V_P	–	V_{CC}	6.0	V	
Input voltage	V_I	–	–0.5	V_{CC} +0.5	V	
Output voltage	V_O	Except Do	GND	V_{CC}	V	
	V_O	Do	GND	V_P	V	
Storage temperature	Tstg	–	–55	+125	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Power supply voltage	V_{CC}	2.7	3.0	4.0	V	
	V_P	V_{CC}	–	5.5	V	
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	Ta	–40	–	+85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 V to 4.0 V, Ta = –40 °C to +85 °C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power supply current*1		I_{CC}	fin = 3000 MHz, V_{CC} = V_P = 3.0 V	6.0	8.0	11.5	mA
Power saving current		I_{PS}	PS = “L”	–	0.1*2	20	µA
Operating frequency	fin	f_{IN}	–	700	–	3000	MHz
	OSC_{IN}	fosc	–	3	–	40	MHz
Input sensitivity	fin*3	Pfin	50 Ω system (Refer to the measurement circuit.)	–10	–	+2	dBm
	OSC_{IN}*3	V_{OSC}	–	0.5	–	V_{CC}	Vp-p
“H” level input voltage	Data, Clock, LE, PS	V_{IH}	–	$V_{CC} \times 0.7$	–	–	V
“L” level input voltage		V_{IL}	–	–	–	$V_{CC} \times 0.3$	
“H” level input current	Data, Clock, LE, PS	I_{IH}*4	–	–1.0	–	+1.0	µA
“L” level input current		I_{IL}*4	–	–1.0	–	+1.0	
“H” level input current	OSC_{IN}	I_{IH}	–	0	–	+100	µA
“L” level input current		I_{IL}*4	–	–100	–	0	
“H” level output voltage	LD/fout	V_{OH}	V_{CC} = V_P = 3.0 V, I_{OH} = –1 mA	V_{CC} – 0.4	–	–	V
“L” level output voltage		V_{OL}	V_{CC} = V_P = 3.0 V, I_{OL} = 1 mA	–	–	0.4	
“H” level output voltage	Do	V_{DOH}	V_{CC} = V_P = 3.0 V, I_{DOH} = –0.5 mA	V_P – 0.4	–	–	V
“L” level output voltage		V_{DOL}	V_{CC} = V_P = 3.0 V, I_{DOL} = 0.5 mA	–	–	0.4	
High impedance cutoff current	Do	I_{OFF}	V_{CC} = V_P = 3.0 V, V_{OFF} = 0.5 V to V_P – 0.5 V	–	–	2.5	nA
“H” level output current	LD/fout	I_{OH}	V_{CC} = V_P = 3.0 V	–	–	–1.0	mA
“L” level output current		I_{OL}	V_{CC} = V_P = 3.0 V	1.0	–	–	
“H” level output current	Do	I_{DOH}*4	V_{CC} = V_P = 3.0 V, V_{DO} = V_P/2, Ta = +25°C	–5.2	–4.0	–2.8	mA
“L” level output current		I_{DOL}		2.8	4.0	5.2	
Charge pump current rate	I_{DOL}/ I_{DOH}	I_{DOMT}*5	V_{DO} = V_P/2	–	5	–	%
	vs V_{DO}	I_{DOVD}*6	0.5 V ≤ V_{DO} ≤ V_P – 0.7 V	–	10	–	%
	vs Ta	I_{DOTA}*7	– 40°C ≤ Ta ≤ +85°C, V_{DO} = V_P/2	–	5	–	%

*1: Conditions; fosc = 13 MHz, Vosc = 1.2 V_{PP}, Ta = +25°C, in locking state.

*2: V_{CC} = V_P = 3.0 V, fosc = 13 MHz, Vosc = 1.2 V_{PP}, Ta = +25°C, in power saving mode

*3: AC coupling. 1000 pF capacitor is connected under the condition of min. operating frequency.

*4: The symbol “–” (minus) means direction of current flow.

*5: V_{CC} = V_P = 3.0 V, Ta = +25°C $(||I_3| - |I_4||) / [(|I_3| + |I_4|) /2] \times 100(\%)$

*6: V_{CC} = V_P = 3.0 V, Ta = +25°C $[(||I_2| - |I_1||) /2] / [(|I_1| + |I_2|) /2] \times 100(\%)$ (Applied to each I_{DOL}, I_{DOH})

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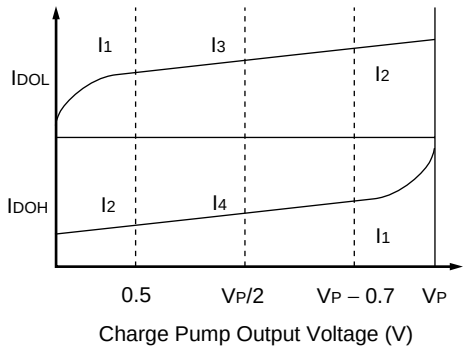
*7: $V_{CC} = V_P = 3.0$ V, $V_{DO} = V_P/2$ ($|I_{DO(+85°C)}| - |I_{DO(-40°C)}|$ /2) / ($|I_{DO(+85°C)}| + |I_{DO(-40°C)}|$ /2) × 100(%)
(Applied to each I_{DOL}, I_{DOH})



■ FUNCTIONAL DESCRIPTION

1. Pulse Swallow Function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(P \times N) + A] \times f_{OSC} \div R \quad (A < N)$

- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)
- P : Preset divide ratio of modulus prescaler (64 or 128)

2. Serial Data Input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the programmable reference divider and the programmable divider separately.
Binary serial data is entered through the Data pin.
One bit of data is shifted into the shift register on the rising edge of the Clock. When the LE signal pin is taken high, stored data is latched according to the control bit data as follows:

Table 1. Control Bit

Control bit (CNT)	Destination of serial data
H	For the programmable reference divider
L	For the programmable divider

(1) Shift Register Configuration

Programmable Reference Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CNT	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	SW	FC	LDS

CNT	: Control bit	[Table 1]
R1 to R14	: Divide ratio setting bit for the programmable reference counter (3 to 16,383)	[Table 2]
SW	: Divide ratio setting bit for the prescaler (64/65 or 128/129)	[Table 5]
FC	: Phase control bit for the phase comparator	[Table 7]
LDS	: LD/f_{OUT} signal select bit	[Table 6]

Note: Start data input with MSB first.

Programmable Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
CNT	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

CNT : Control bit [Table 1]
N1 to N11: Divide ratio setting bits for the programmable counter (3 to 2,047) [Table 3]
A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127) [Table 4]

Note: Data input with MSB first.

Table 2. Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio(R)	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

Table 3. Binary 11-bit Programmable Counter Data Setting

Divide ratio(N)	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

Table 4. Binary 7-bit Swallow Counter Data Setting

Divide ratio (A)	A7	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Table 5. Prescaler Data Setting

SW	Prescaler divide ratio
1	64/65
0	128/129

Table 6. LD/fout Output Select Data Setting

LDS	LD/fout output signal
1	fout signal
0	LD signal

(2) Relation between the FC Input and Phase Characteristics

The FC bit changes the phase characteristics of the phase comparator. The internal charge pump output level (D_O) is reversed according to the FC bit. Also, the monitor pin (fout) output is controlled by the FC bit. The relationship between the FC bit and D_O is shown below.

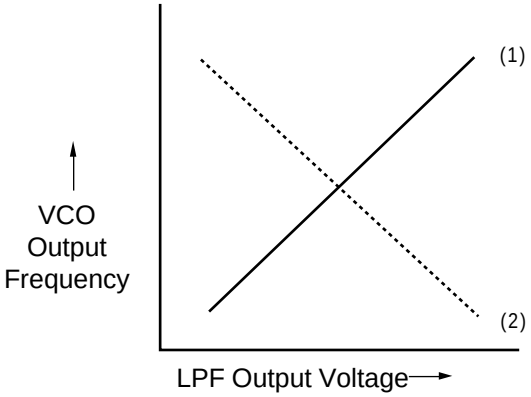
Table 7. FC Bit Data Setting (LDS = "1")

	FC = 1		FC = 0	
	D_O	LD/fout	D_O	LD/fout
$fr > f_P$	H	fout = fr	L	fout = fp
$fr < f_P$	L		H	
$fr = f_P$	Z		Z	

Z : High impedance

When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.

- When the LPF and VCO characteristics are similar to (1), set FC bit high.
- When the VCO characteristics are similar to (2), set FC bit low.



Note : Give attention to the polarity for using active type LPF.

3. Power Saving Mode (Intermittent Mode Control Circuit)

Table 10. PS Pin Setting

PS pin	Status
H	Normal mode
L	Power saving mode

The intermittent mode control circuit reduces the PLL power consumption.

By setting the PS pin low, the device enters into the power saving mode, reducing the current consumption. See the Electrical Characteristics chart for the specific value.

The phase detector output, Do, becomes high impedance.

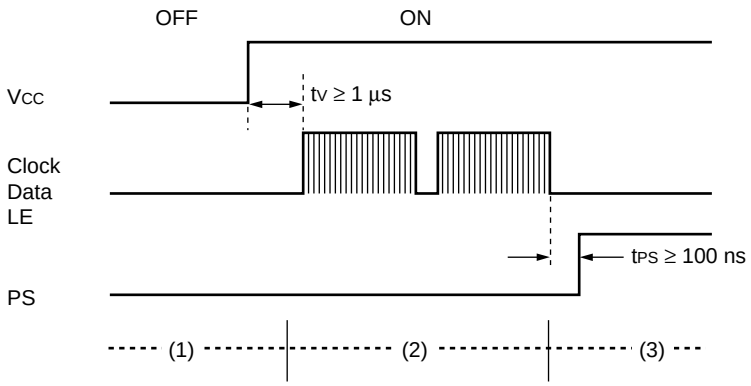
For the signal PLL, the lock detector, LD, remains high, indicating a locked condition.

Setting the PS pin high, releases the power saving mode, and the device works normally.

The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation. When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because of the unknown relationship between the comparison frequency (fp) and the reference frequency (fr) which can cause a major change in the comparator output, resulting in a VCO frequency jump and an increase in lockup time.

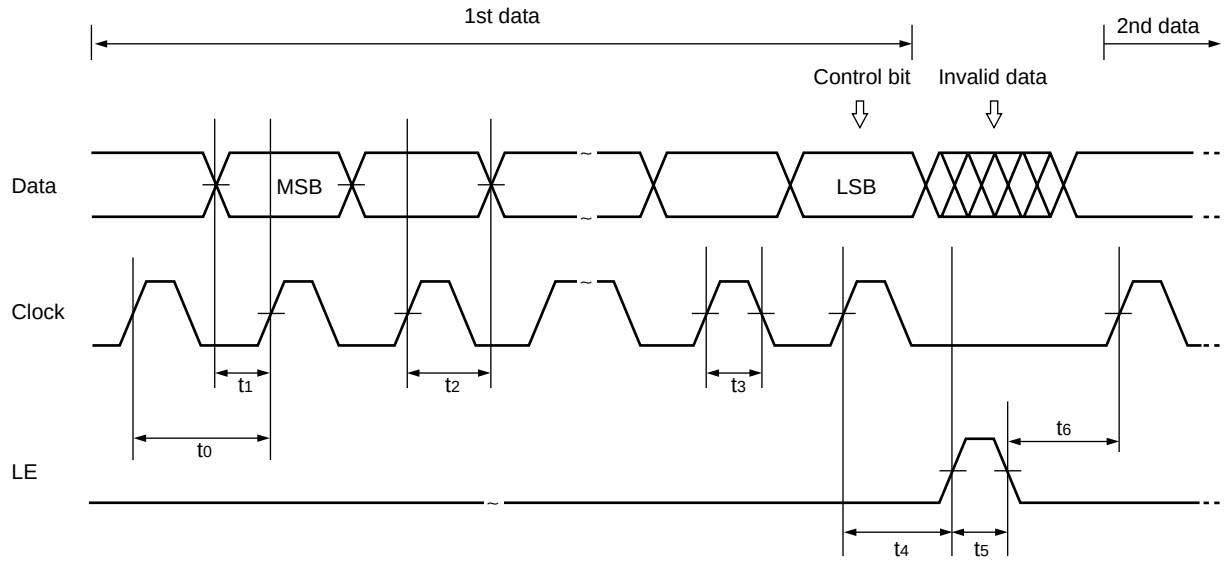
To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

Notes :
- When power (V_{CC}) is first applied, the device must be in standby mode, PS = Low.
- The serial data input after the power supply becomes stable and the the power saving mode is released after completed the data input..



(1) PS = L (power saving mode) at Power ON
(2) Set serial data 1 µs later after power supply remains stable ($V_{CC} \geq 2.2$ V).
(3) Release power saving mode (PS: “L” → “H”) 100 ns later after setting serial data.

■ SERIAL DATA INPUT TIMING



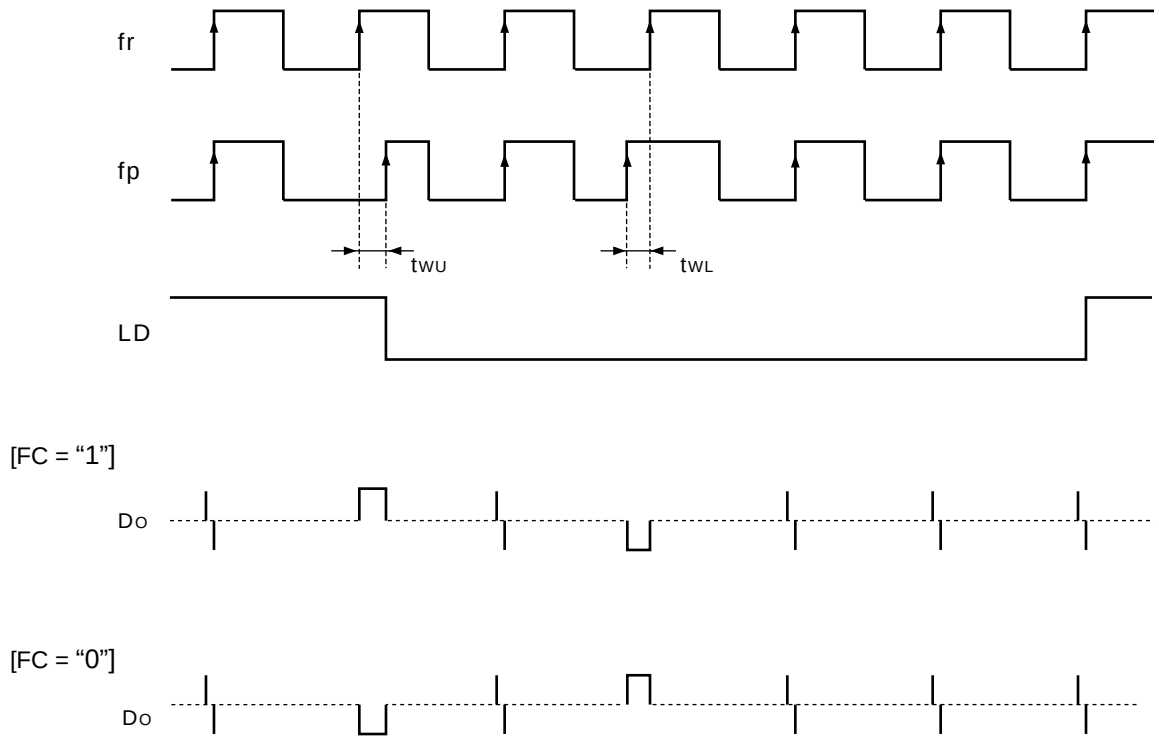
On the rising edge of the clock, one bit of data is transferred into the shift register.

Parameter	Min	Typ	Max	Unit
t_1	20	–	–	ns
t_2	20	–	–	ns
t_3	30	–	–	ns
t_4	30	–	–	ns

Parameter	Min	Typ	Max	Unit
t_5	100	–	–	ns
t_6	20	–	–	ns
t_7	100	–	–	ns

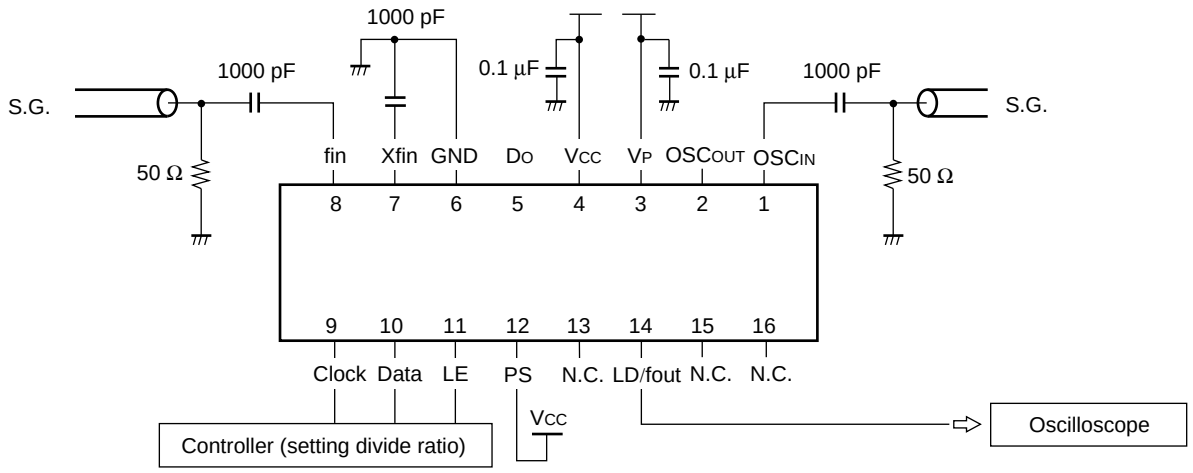
Note: LE should be “L” when the data is transferred into the shift register.

■ PHASE COMPARATOR OUTPUT WAVEFORM



Notes:
- Phase error detection range: –2π to +2π
- Pulses on Do signal during locked state are output to prevent dead zone.
- LD output becomes low when phase is t_{WU} or more. LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
- t_{WU} and t_{WL} depend on OSC_{IN} input frequency.
  t_{WU} > 2/fosc (s) (e. g. t_{WU} > 153.8 ns, fosc = 13 MHz)
  t_{WU} < 4/fosc (s) (e. g. t_{WL} < 307.7 ns, fosc = 13 MHz)
- LD becomes high during the power saving mode (PS = "L").

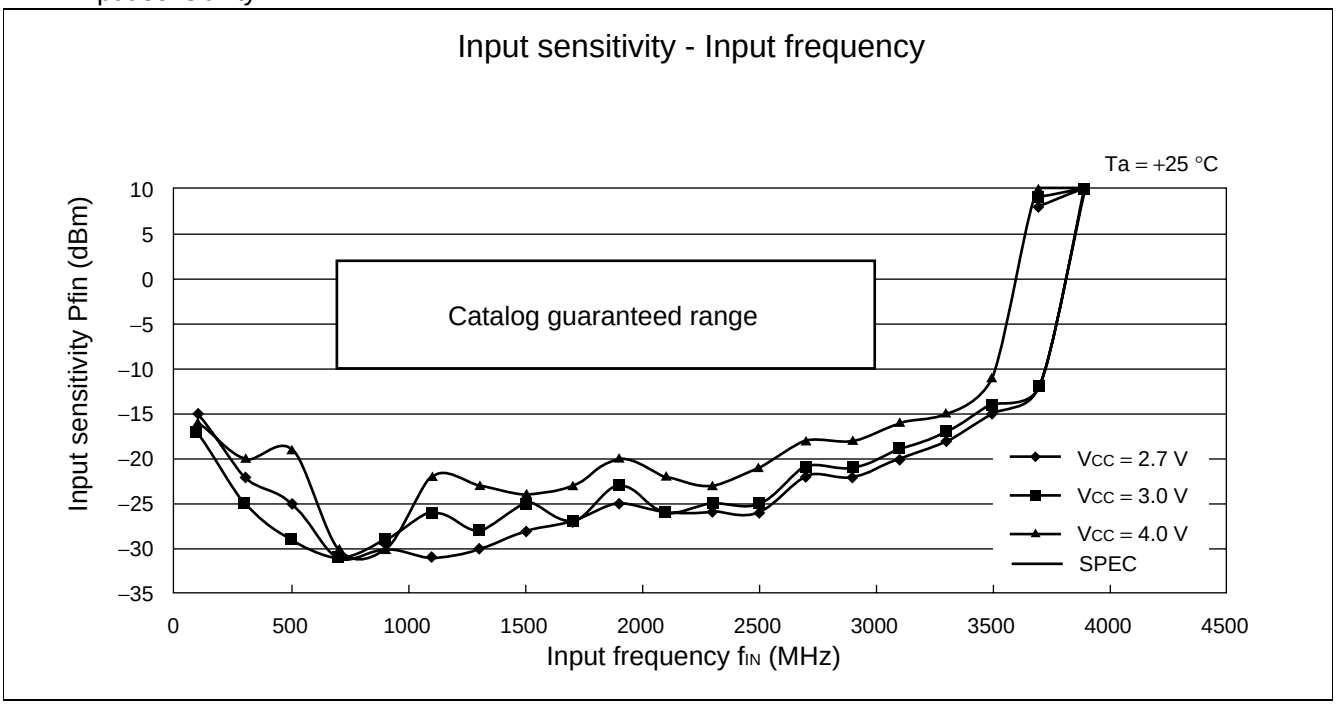
■ MEASURMENT CIRCUIT (for Measuring Input Sensitivity fin/OSC_{IN})



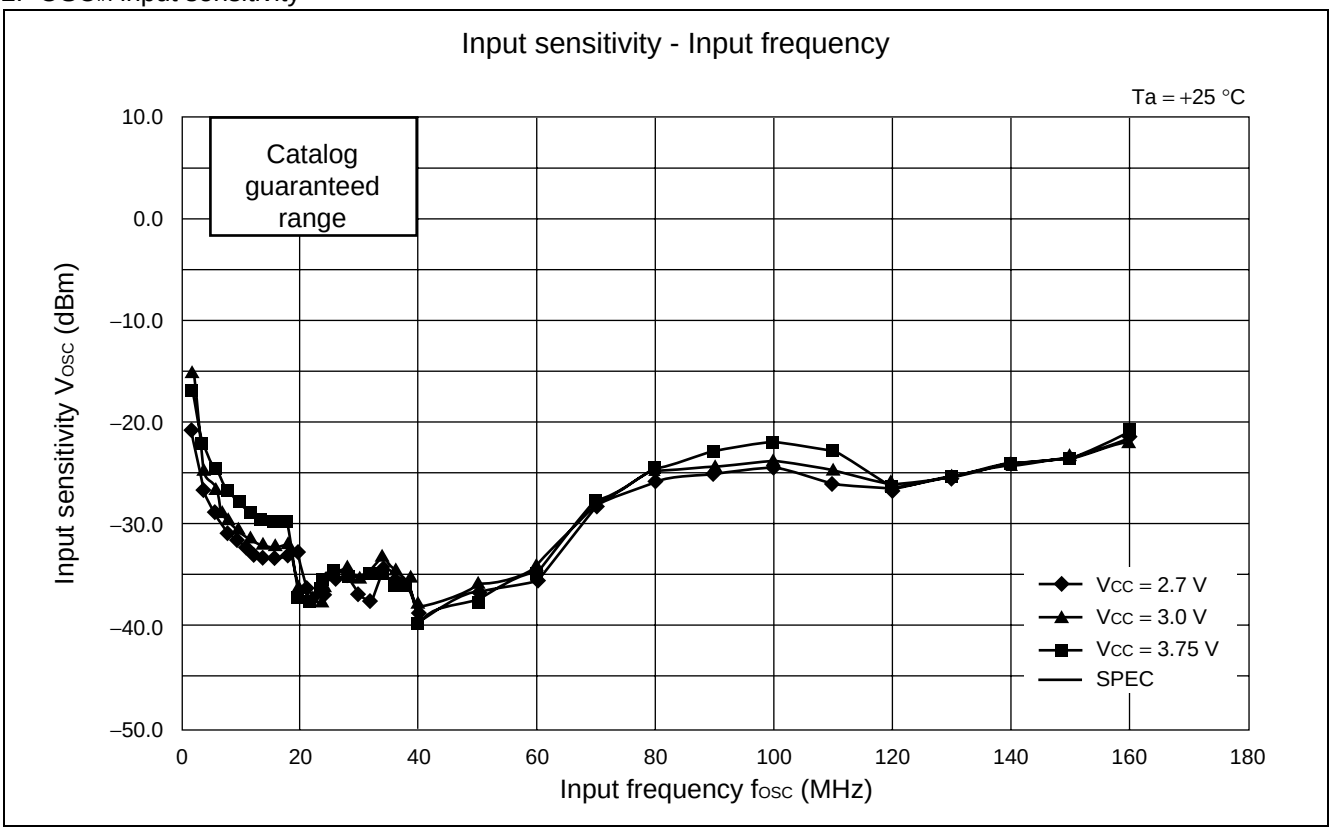
Note: TSSOP-16

■ TYPICAL CHARACTERISTICS

1. fin input sensitivity

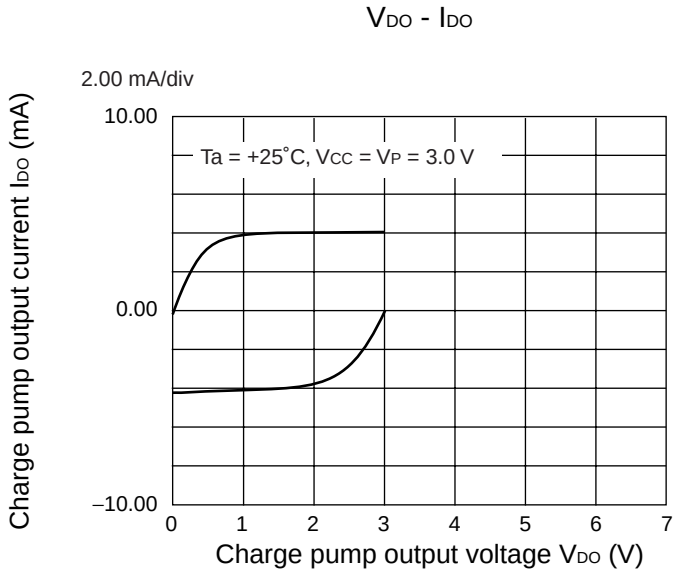


2. OSC_{IN} input sensitivity

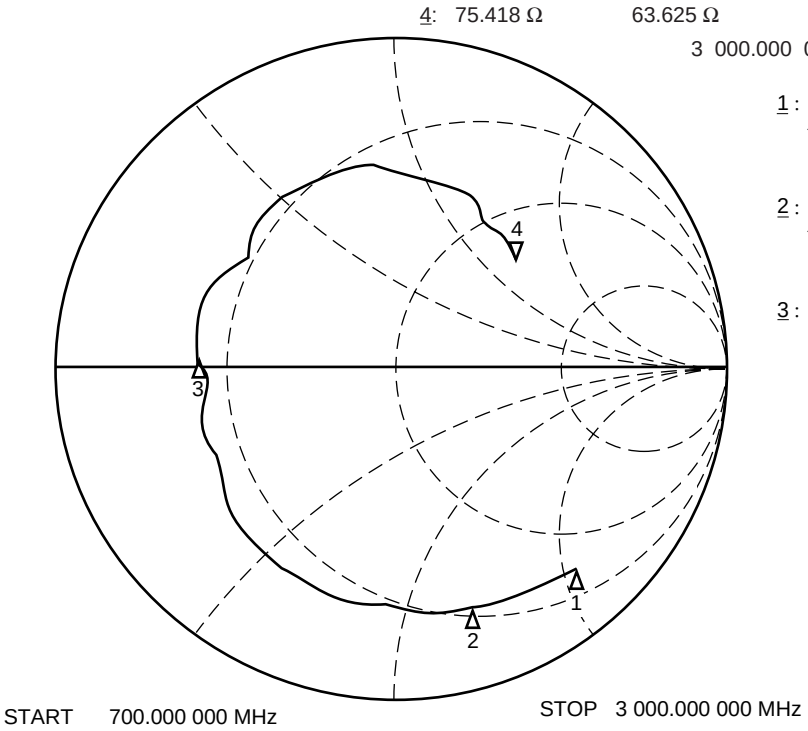


3. Do output current

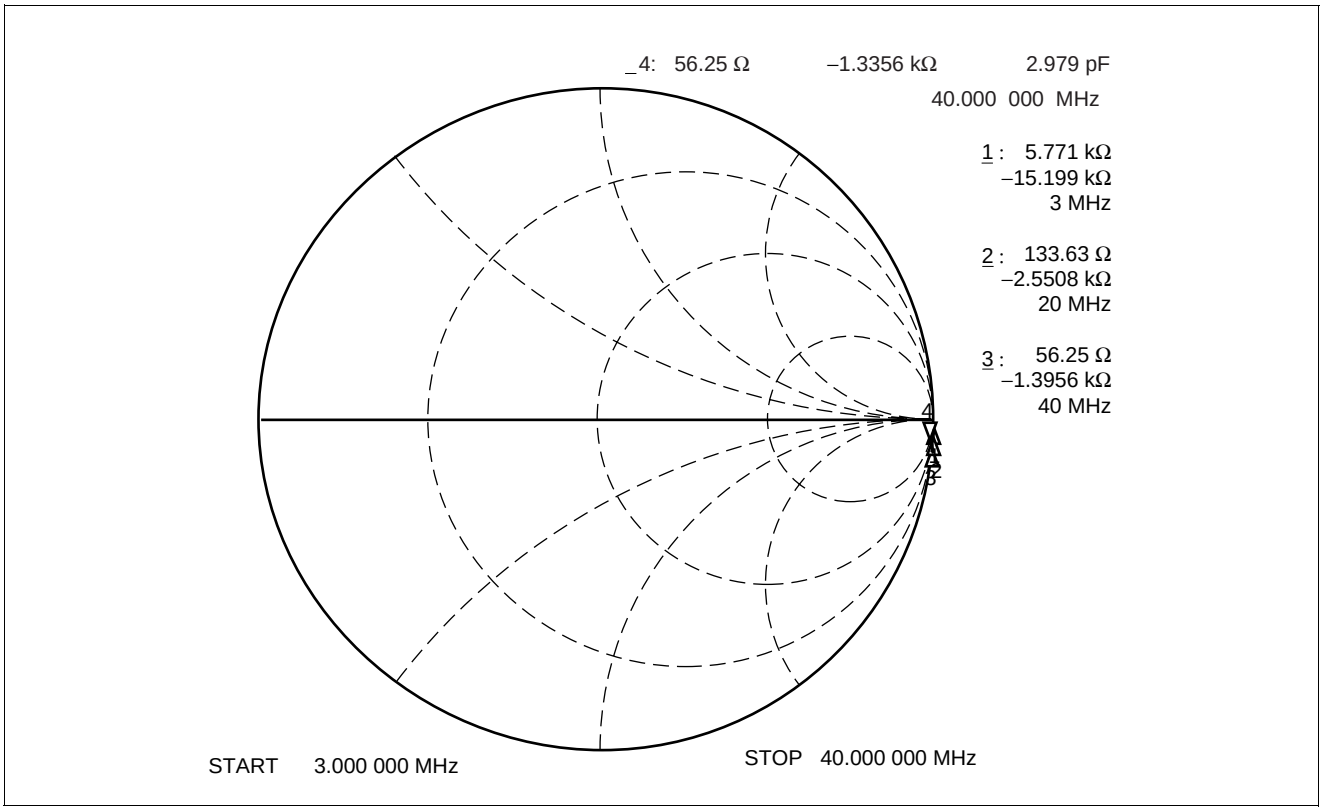
- 4.0 mA



4. fin input impedance

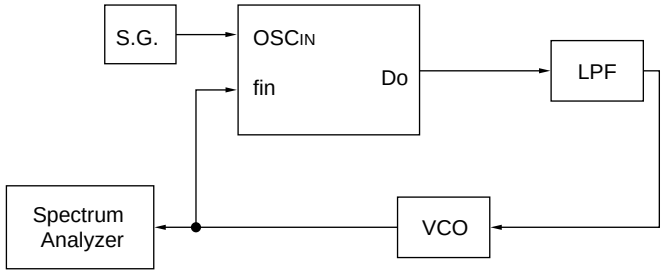


5. OSC_{IN} input impedance



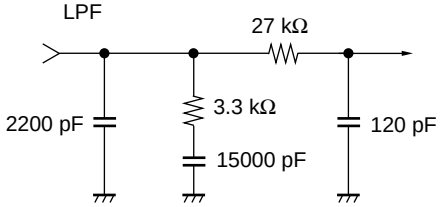
■ REFERENCE INFORMATION

Test Circuit

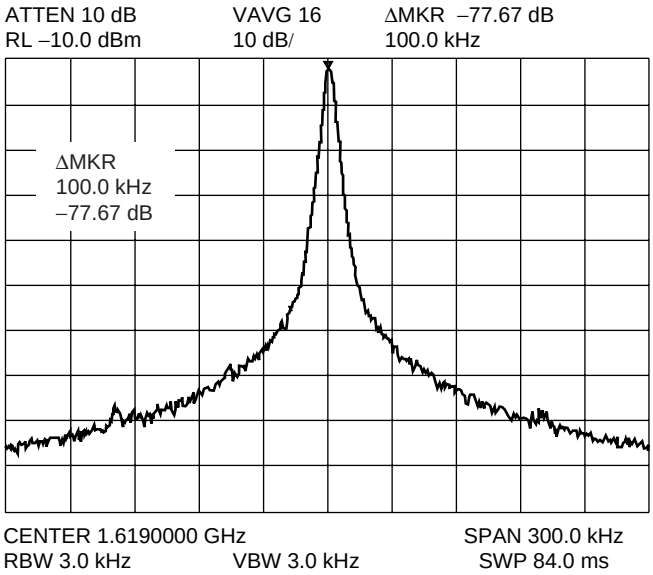


f_{VCO} = 1619 MHz
K_V = 44 MHz/V
fr = 100 kHz
f_{OSC} = 10 MHz (1.2 V_{PP})
V_{CC} = V_P = 3.0 V
V_{VCO} = 3.0 V
Ta = +25 °C
CP : 4 mA

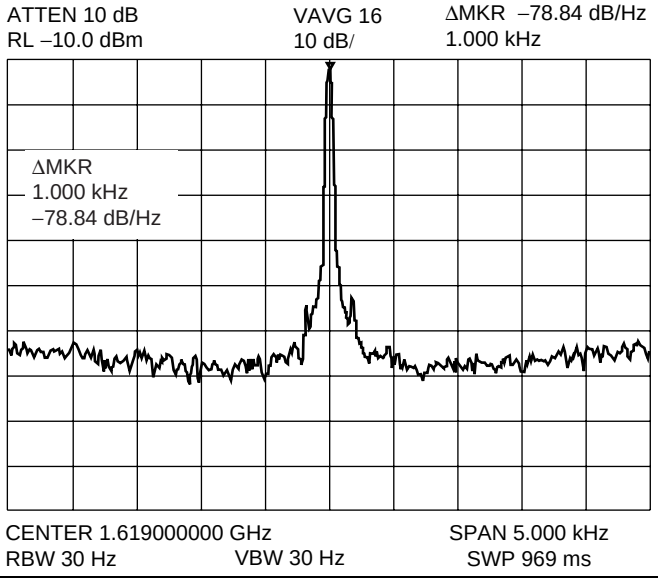
LPF



- PLL Reference Leakage



- PLL Phase Noise



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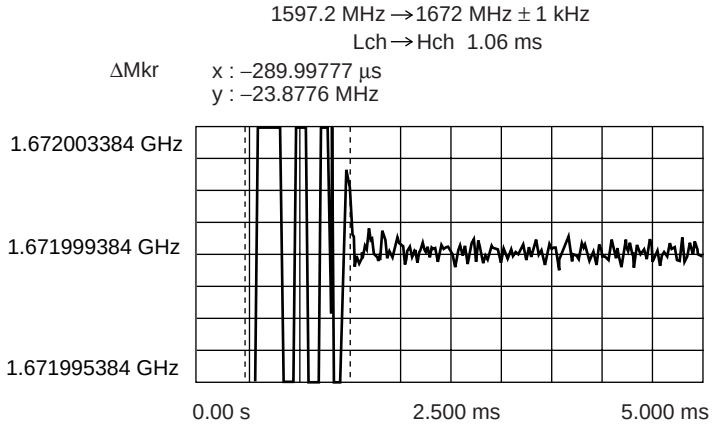
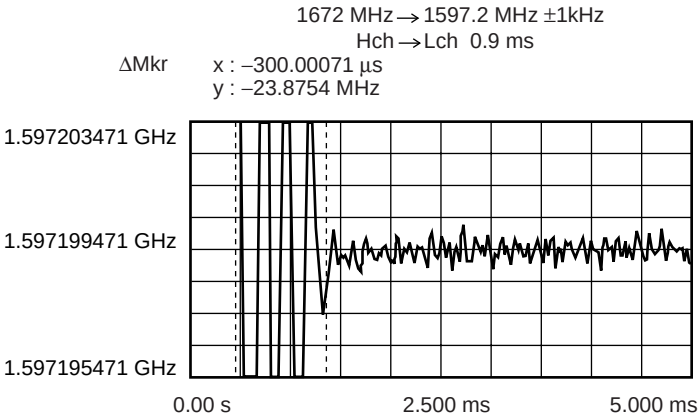
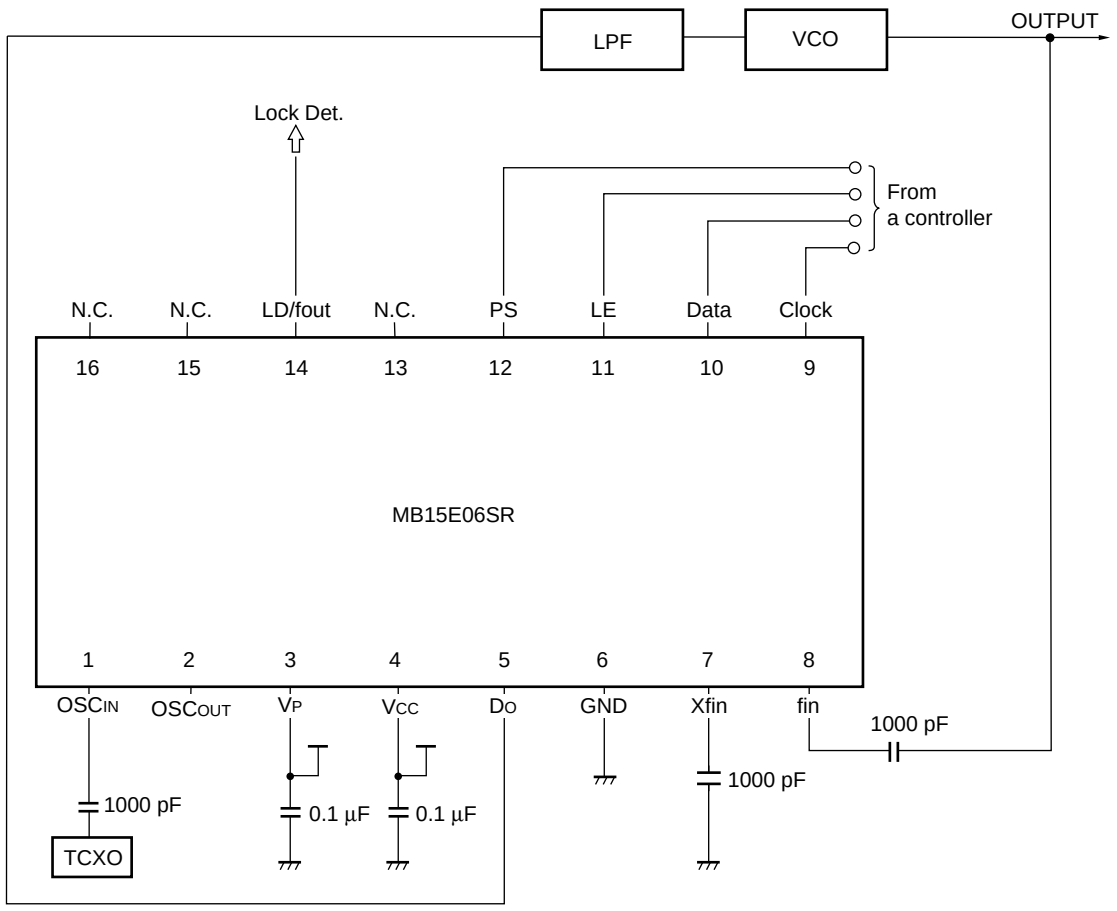
- PLL Lock Up time



- PLL Lock Up time



■ APPLICATION EXAMPLE



V_P: 5.5 V Max

Note: TSSOP-16

■ USAGE PRECAUTIONS

To protect against damage by electrostatic discharge, note the following handling precautions:
-Store and transport devices in conductive containers.
-Use properly grounded workstations, tools, and equipment.
-Turn off power before inserting device into or removing device from a socket.
-Protect leads with a conductive sheet when transporting a board-mounted device.

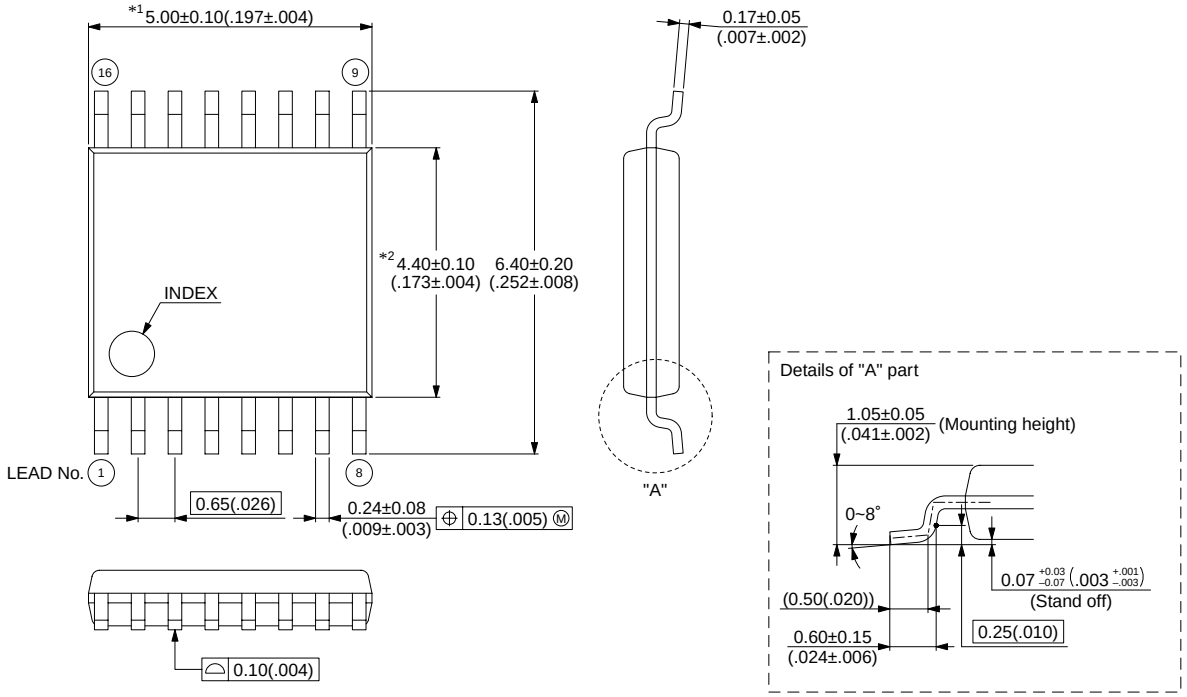
■ ORDERING INFORMATION

Part number	Package	Remarks
MB15E06SRPFT	16-pin, Plastic TSSOP (FPT-16P-M07)	
MB15E06SRPV1	16-pad, Plastic BCC (LCC-16P-M06)	

■ PACKAGE DIMENSIONS

16-pin, Plastic TSSOP
(FPT-16P-M07)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max) .
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.

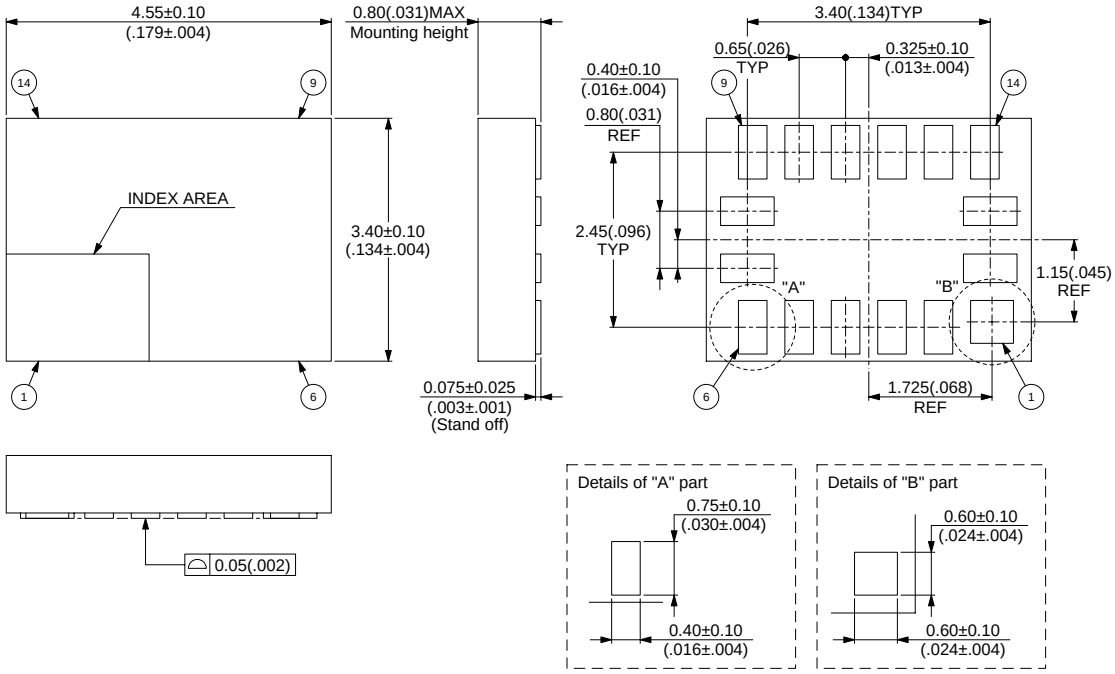


Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

(Continued)

(Continued)

16-pad plastic BCC
(LCC-16P-M06)



Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

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