

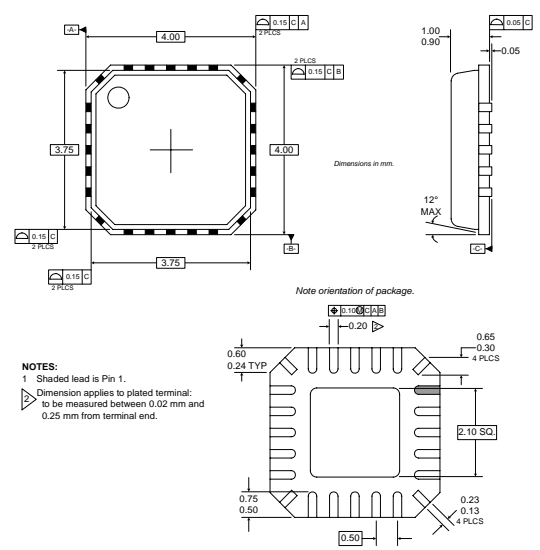
**RoHS Compliant & Pb-Free Product**

Typical Applications

- CDMA PCS Handsets
- GPS Receiver
- W-CDMA Handsets
- General Purpose Downconverter
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment

Product Description

The RF2460 is a receiver front-end designed for the receive section of PCS CDMA and W-CDMA applications. It is designed to amplify and downconvert RF signals while providing 29dB of stepped gain control range and features digital control of LNA gain, mixer gain, and power down mode. A further feature of the chip is adjustable IIP3 of the LNA and mixer using an off-chip current setting resistor. Noise Figure, IP3, and other specs are designed to be compatible with the IS-98B for CDMA PCS communications. The IC is manufactured on an advanced Silicon Germanium Bi-CMOS process and is assembled in a 20-pin, QFN package with an exposed die flag.



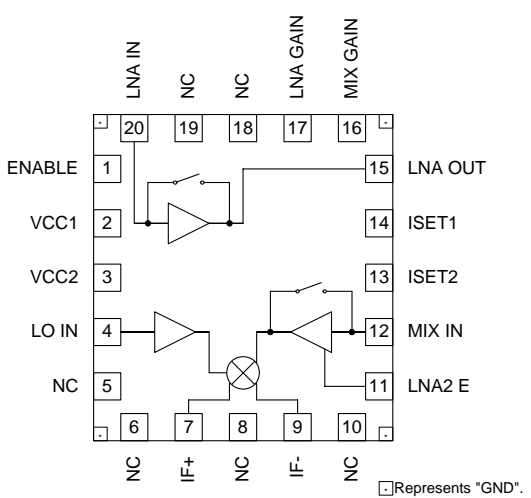
Package Style: QFN, 20-Pin, 4 x 4

Optimum Technology Matching® Applied

- |                                     |                                   |  |
|-------------------------------------|-----------------------------------|--|
| <input type="checkbox"/> Si BJT     | <input type="checkbox"/> GaAs HBT | <input type="checkbox"/> GaAs MESFET             |
| <input type="checkbox"/> Si Bi-CMOS | <input type="checkbox"/> SiGe HBT | <input type="checkbox"/> Si CMOS                 |
| <input type="checkbox"/> InGaP/HBT  | <input type="checkbox"/> GaN HEMT | <input checked="" type="checkbox"/> SiGe Bi-CMOS |

Features

- Complete Receiver Front-End
- Stepped LNA/Mixer Gain Control
- Adjustable LNA/Mixer Bias Current
- 24dB Gain and 2.2dB Noise Figure at Maximum Cascade Gain



Functional Block Diagram

Ordering Information

RF2460                      MPCD CDMA Low Noise Amplifier/Mixer 1500MHz  
to 2200MHz Downconverter  
RF2460PCBA-41X      Fully Assembled Evaluation Board

RF Micro Devices, Inc.                      Tel (336) 664 1233  
7628 Thorndike Road                      Fax (336) 664 0454  
Greensboro, NC 27409, USA                      <http://www.rfmd.com>

# RF2460

## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V <sub>DC</sub>
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C



Caution! ESD sensitive device.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Overall</b>					T = 25°C, V <sub>CC</sub> = 2.75V, RF = 1.96GHz, LO = 2170MHz @ -7dBm, IF = 210MHz
RF Frequency Range		1500 to 2200		MHz	
LO Frequency Range		1200 to 2600		MHz	
IF Frequency Range		0.1 to 250		MHz	
Bias Current		2.5	2.8	mA	LNA, mixer and preamp for bias circuitry.
<b>US PCS - LNA</b>					
Gain	13.5	15.0		dB	IIP3 is adjustable (see plots for setting). ISET1 (pin 14) external resistor sets current consumption and performance.
Noise Figure		1.4	1.8	dB	
Input IP3	+6.0	+7.0		dBm	
Input VSWR			2:1		
Output VSWR			2:1		
Current at Input IP3		7	7.5	mA	
<b>US PCS - LNA Bypass</b>					
Gain	-6	-5		dB	1 kΩ balanced load.
Noise Figure		5	5.5	dB	
Input IP3	+23.0	+26.0		dBm	
Input VSWR			2:1		
Output VSWR			2:1		
Current		0		mA	
<b>US PCS - Mixer - High Gain Mode</b>					
Gain	10	12		dB	1 kΩ balanced load.
Noise Figure		6.5	7.5	dB	
Input IP3	+3.0	+4.0		dBm	
RF to IF Isolation		>45		dB	
Input VSWR			2:1		
Output VSWR			2:1		
Current		12	13	mA	
<b>US PCS - Mixer - Low Gain Mode</b>					
Gain	0	1.5		dB	1 kΩ balanced load.
Noise Figure		15	16	dB	
Input IP3	+13.0	+14.0		dBm	
RF to IF Isolation		>45		dB	
Input VSWR			2:1		
Output VSWR			2:1		
Current		7.5	8.0	mA	

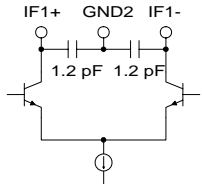
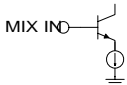
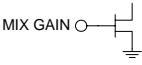
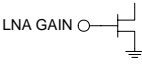
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>KPCS - LNA</b> Gain Noise Figure Input IP3  Input VSWR Output VSWR Current at Input IP3	14.5  +5.0	16.0 1.4 +6.0  7	1.8  2:1 2:1 7.5	dB dB dBm  mA	IIP3 is adjustable (see plots for setting). ISET1 (pin 14) external resistor sets current consumption and performance.
<b>KPCS - LNA Bypass</b> Gain Noise Figure Input IP3 Input VSWR Output VSWR Current	-6  +23.0	-5 5.0 +26.0  0	5.5  2:1 2:1	dB dB dBm  mA	
<b>KPCS - Mixer - High Gain Mode</b> Gain Noise Figure Input IP3 RF to IF Isolation  Input VSWR Output VSWR Current	10  +2.5	12 6.5 +3.5 >45  12	7.5  2:1 2:1 13	dB dB dBm dB  mA	1 k $\Omega$ balanced load.  IIP3 is adjustable (see plots for setting). ISET2 (pin 13) external resistor sets current consumption and performance.
<b>KPCS - Mixer - Low Gain Mode</b> Gain Noise Figure Input IP3 RF to IF Isolation  Input VSWR Output VSWR Current	0  +13.0	1.5 15 +14.0 >45  7.5	16  2:1 2:1 8.0	dB dB dBm dB  mA	1 k $\Omega$ balanced load.  IIP3 is adjustable ISET2 (pin 13) external resistor sets current consumption and performance.

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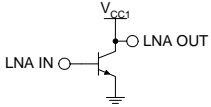
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>GPS - LNA</b> Gain Noise Figure Input IP3  Current at Input IP3		16 1.4 +7.0 7		dB dB dBm mA	IIP3 is adjustable. ISET1 (pin 14) external resistor sets current consumption and performance.
<b>GPS - Mixer</b> Gain Noise Figure Input IP3  Current at Input IP3		17 6 -5.0 16		dB dB dBm mA	IIP3 is adjustable. ISET1 (pin 14) external resistor sets current consumption and performance.
<b>GPS - Cascaded</b> Gain Noise Figure Input IP3  Current at Input IP3		31 1.8 -19.0 23		dB dB dBm mA	IIP3 is adjustable. ISET1 (pin 14) external resistor sets current consumption and performance.
<b>Local Oscillator Input</b> Input Level LO to RF Isolation LO to LNA Isolation LO Current Buffer	-10	-7 >40 >60 4.5	0   5.0	dBm dB dB mA	Any gain state. Any gain state. I <sub>CC2</sub> when LO signal is present
<b>US PCS - Cascade - LNA High/Mixer High</b> Gain Noise Figure Input IP3 Total Current		24 2.2 -8.0 26		dB dB dBm mA	LNA High Gain/Mixer High Gain Assuming 3dB loss of filter IF 1, 1kΩ balanced load. Single sideband.
<b>US PCS - Cascade - LNA High/Mixer Low</b> Gain Noise Figure Input IP3 Total Current		13.5 5.3 +1.0 21		dB dB dBm mA	LNA High Gain/Mixer Low Gain Assuming 3dB loss of filter IF 1, 1kΩ balanced load. Single sideband.
<b>US PCS - Cascade - LNA Low/Mixer High</b> Gain Noise Figure Input IP3 Total Current		4 14.5 +12.0 19		dB dB dB mA	LNA Low Gain/Mixer High Gain Assuming 3dB loss of filter IF 1, 1kΩ balanced load. Single sideband.
<b>US PCS - Cascade - LNA Low/Mixer Low</b> Gain Noise Figure Input IP3 Total Current		-6.5 23 +20.5 14		dB dB dB mA	LNA Low Gain/Mixer Low Gain Assuming 3dB loss of filter IF 1, 1kΩ balanced load. Single sideband.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>KPCS - Cascade - LNA High/Mixer High</b> Gain Noise Figure Input IP3 Total Current		25 2.2 -9.5 26		dB dB dBm mA	LNA High Gain/Mixer High Gain Assuming 3dB loss of filter IF 1, 1 kΩ balanced load. Single sideband.
<b>KPCS - Cascade - LNA High/Mixer Low</b> Gain Noise Figure Input IP3 Total Current		14.5 5.3 +1.0 21		dB dB dBm mA	LNA High Gain/Mixer Low Gain Assuming 3dB loss of filter IF 1, 1 kΩ balanced load. Single sideband.
<b>KPCS - Cascade - LNA Low/Mixer High</b> Gain Noise Figure Input IP3 Total Current		4 14.5 +12.0 19		dB dB dB mA	LNA Low Gain/Mixer High Gain Assuming 3dB loss of filter IF 1, 1 kΩ balanced load. Single sideband.
<b>KPCS - Cascade - LNA Low/Mixer Low</b> Gain Noise Figure Input IP3 Total Current		-6.5 23 +22 14		dB dB dB mA	LNA Low Gain/Mixer Low Gain Assuming 3dB loss of filter IF 1, 1 kΩ balanced load. Single sideband.
<b>Power Supply</b> Voltage	2.7	3.0	3.3	V	

# RF2460

Pin	Function	Description	Interface Schematic
1	<b>ENABLE</b>	Power down pin. A logic "low" turns the part off. A logic "high" (>1.6V) turns the part on.	
2	<b>VCC1</b>	Supply Voltage for the LNA, mixer, bias, and logic circuitry. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	See pin 20.
3	<b>VCC2</b>	Supply Voltage for the LO buffer amplifier. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
4	<b>LO IN</b>	Mixer LO Input Pin.	
5	<b>NC</b>	No connection. For isolation purposes, this pin is connected to the ground plane.	
6	<b>NC</b>	No connection. For isolation purposes, this pin is connected to the ground plane.	
7	<b>IF+</b>	CDMA IF Output pin. This is a balanced output. The internal circuitry, in conjunction with an external matching/bias inductor to $V_{CC}$ , sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The part is designed to drive a 1 k $\Omega$ load. Because this pin is biased to $V_{CC}$ , a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	
8	<b>NC</b>	No connection. For isolation purposes, this pin is connected to the ground plane.	
9	<b>IF-</b>	Same as pin 7, except complementary output.	See pin 6.
10	<b>NC</b>	No connection. For isolation purposes, this pin is connected to the ground plane.	
11	<b>LNA2 E</b>	Emitter for LNA2. Increasing the inductance on this pin will reduce the mixer gain, increase IP3 and noise figure.	
12	<b>MIX IN</b>	Mixer RF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. External matching network sets RF and IF impedance for optimum performance.	
13	<b>ISET2</b>	This pin is used to set the bias current and IIP3 of the mixer amplifier using a resistor to ground. See plots for values and current settings.	
14	<b>ISET1</b>	This pin is used to set the bias current and IIP3 of the LNA amplifier using a resistor to ground. See plots for values and current settings.	
15	<b>LNA OUT</b>	LNA output pin. Open collector.	See pin 20.
16	<b>MIX GAIN</b>	CMOS compatible signal controlling mixer gain mode. Setting this signal high places the mixer in the high gain mode. Setting this signal low places the mixer in low gain mode by bypassing and shutting off the mixer buffer amplifier current.	
17	<b>LNA GAIN</b>	CMOS compatible signal controlling LNA gain mode. Setting this signal high places the LNA in the high gain mode. Setting this signal low bypasses the LNA and shuts off the LNA bias current.	
18	<b>NC</b>	No connection. For isolation purposes, this pin is connected to the ground plane.	
19	<b>NC</b>	No connection. For isolation purposes, this pin is connected to the ground plane.	

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Pin	Function	Description	Interface Schematic
20	LNA IN	RF Input pin. This pin is internally matched for optimum noise figure from a 50Ω source.	 <p>The schematic shows a common-emitter amplifier configuration. The input terminal is labeled 'LNA IN' and is connected to the base of a transistor. The base is biased through a resistor connected to a supply terminal labeled 'V<sub>CC1</sub>'. The emitter is connected to ground. The output terminal is labeled 'LNA OUT' and is connected to the collector of the transistor.</p>
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias.	

## Output Interface Network of the Mixer

L1, C1, C2, and R form a current combiner which performs a differential to single-ended conversion at the IF frequency and sets the output impedance. In most cases, the resonance frequency is independent of R and can be set according to the following equation:

$$f_{IF} = \frac{1}{2\pi\sqrt{\frac{L1}{2}(C_1 + 2C_2 + C_{EQ})}}$$

Where  $C_{EQ}$  is the equivalent stray capacitance and capacitance looking into pins 7 and 9. An average value to use for  $C_{EQ}$  is 2.5pF.

R can then be used to set the output impedance according to the following equation:

$$R = \left( \frac{1}{4 \cdot R_{OUT}} - \frac{1}{R_P} \right)^{-1}$$

where  $R_{OUT}$  is the desired output impedance and  $R_P$  is the parasitic equivalent parallel resistance of L1.

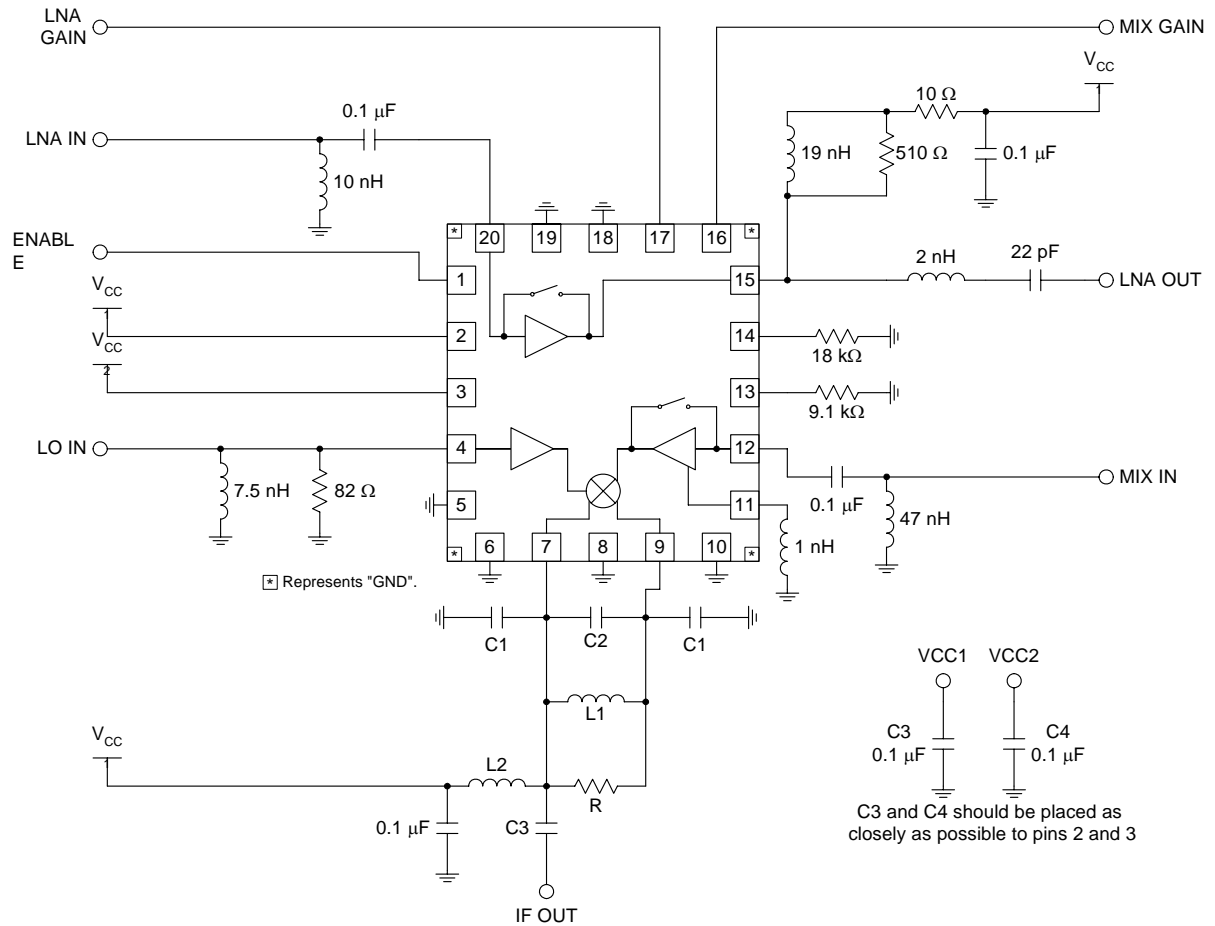
$C_2$  should first be set to 0 and C1 should be chosen as high as possible (suggested less than 20pF), while maintaining an  $R_P$  of L1 that allows for the desired  $R_{OUT}$ . If the self-resonant frequencies of the selected C1 produce unsatisfactory linearity performance, their values may be reduced and compensated for by including C2 capacitor with a value chosen to maintain the desired  $F_{IF}$  frequency.

L2 and C3 serve dual purposes. L2 serves as an output bias choke, and C3 serves as a series DC block.

In addition, L2 and C3 may be chosen to form an impedance matching network if the input impedance of the IF filter is not equal to  $R_{OUT}$ . Otherwise, L2 is chosen to be large (suggested 120nH) and C3 is chosen to be large (suggested 22nF) if a DC path to ground is present in the IF filter, or omitted if the filter is DC blocked.



## Application Schematic - US PCS

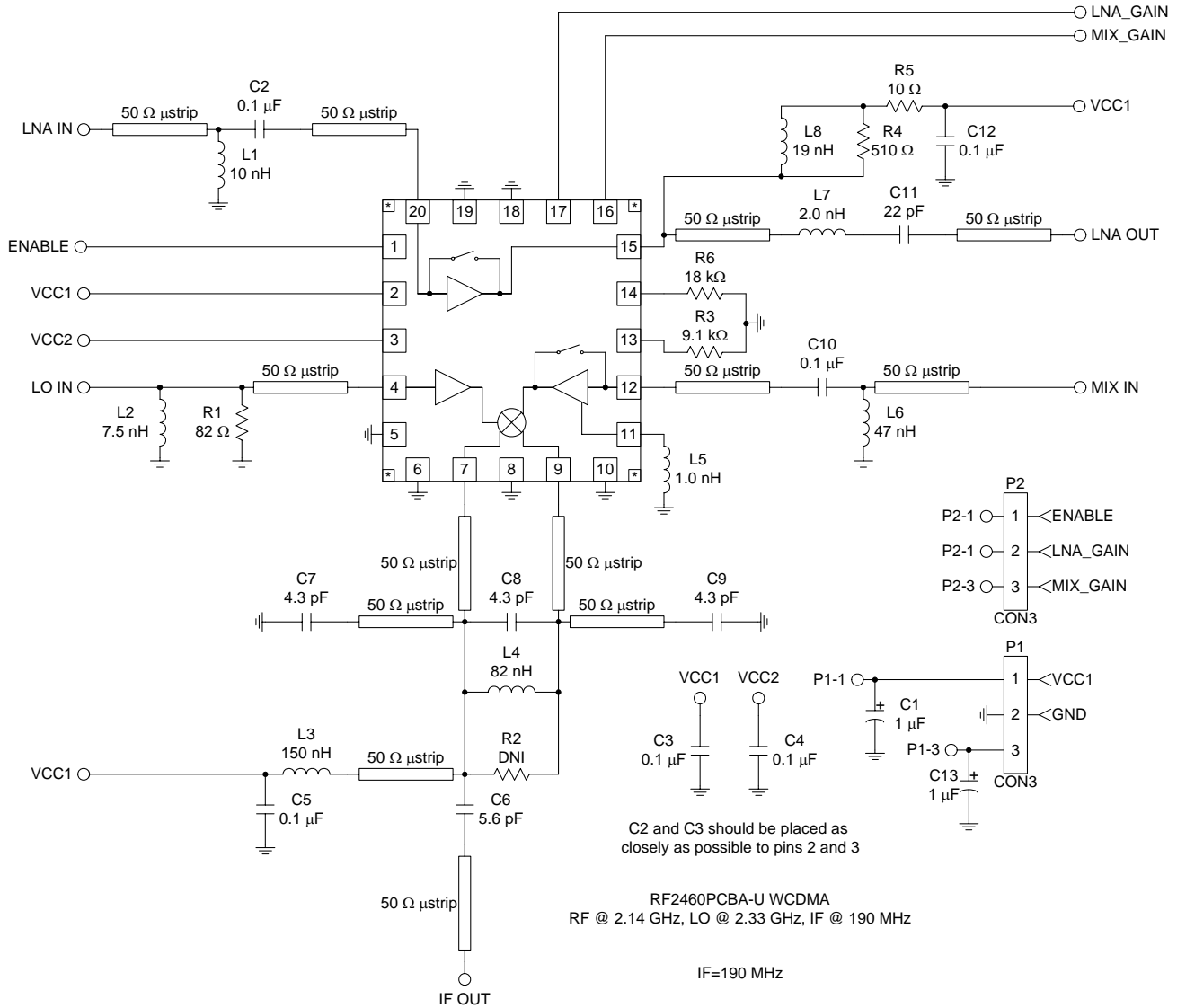


	C1 (pF)	C2 (pF)	C3 (pF)	L1 (nH)	L2 (nH)	R (Ω)
US PCS, IF = 210 MHz	4	3	6	82	110	4.7 k
Korean PCS, IF = 220 MHz	3.6	2	7	82	120	4.7 k
GPS, IF = 184 MHz	8.2	DNI	6.2	120	180	10 k
US PCS, IF = 184 MHz	8	3	6	82	110	4.7 k

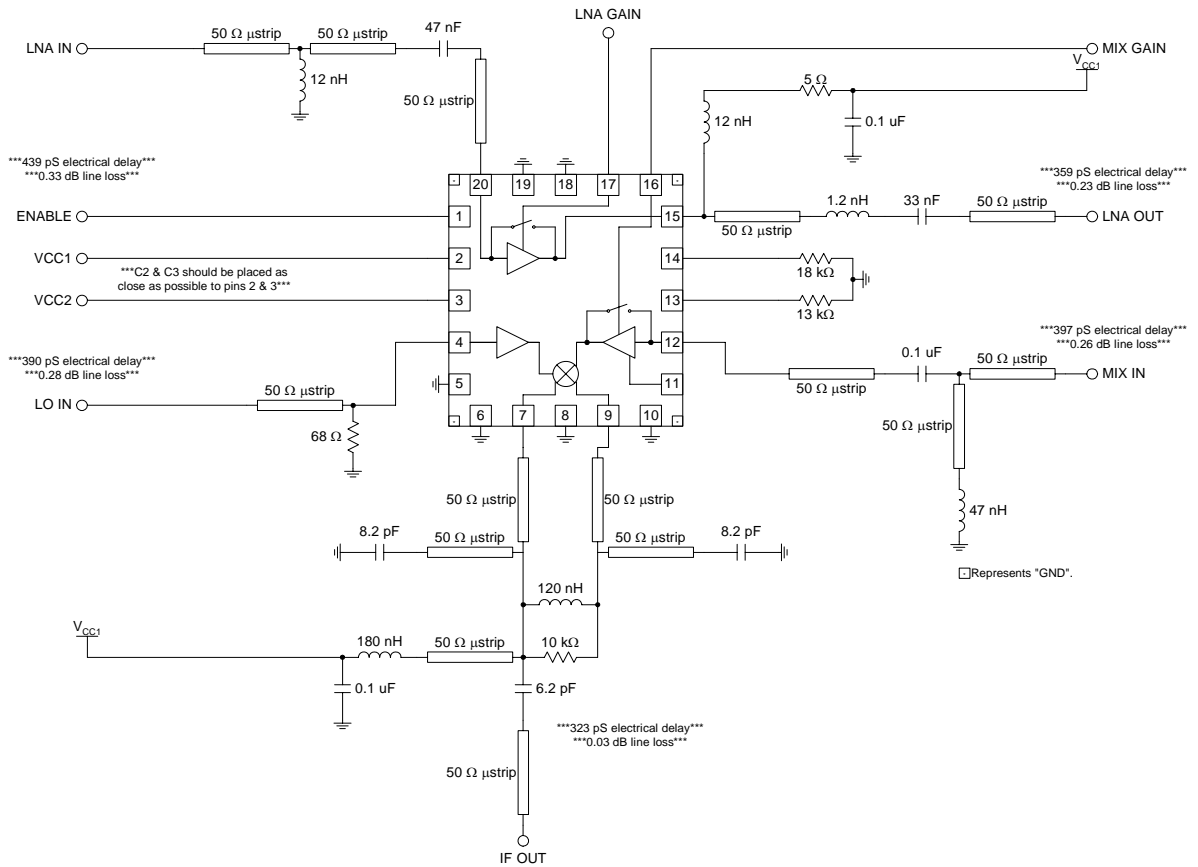
# RF2460

## Application Schematic - W-CDMA

(See W-CDMA charts for lab measurements at the end of the data sheet)



## Application Schematic - GPS RF = 1575MHz, IF = 184MHz, LO = 1759MHz



## Current Measurement

To measure only the current of the different circuitry in the evaluation board, use the following procedure.

First, replace the bias choke inductor at the output of the mixer (L3 for US-PCS) with a 1Ω resistor. The voltage across the resistor will represent the mixer current. Terminate all SMA connections at 50Ω.

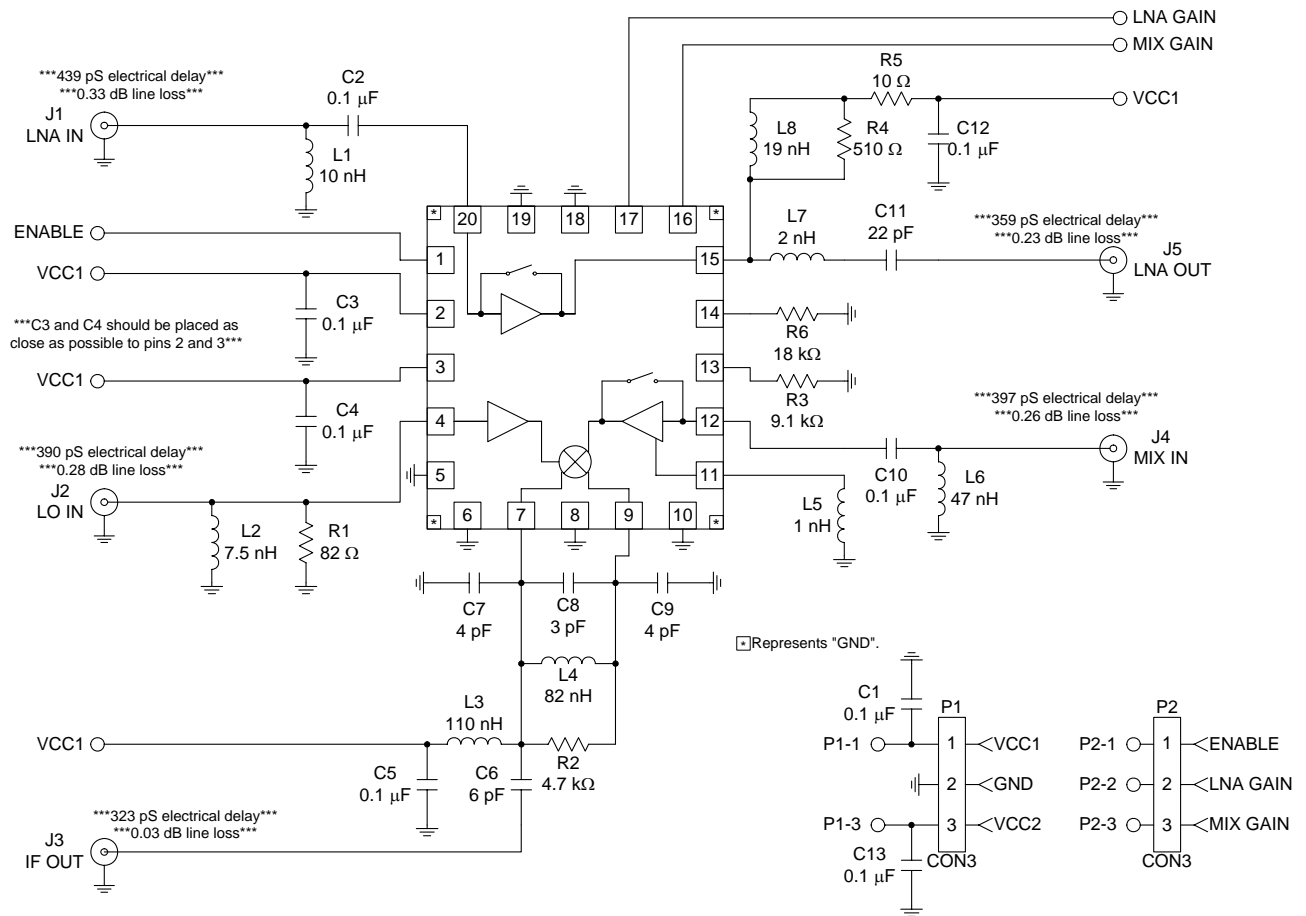
Second, follow the table below.

	CONDITION					
	Current (mA)	V <sub>CC1</sub>	V <sub>CC2</sub>	EN	LNA Gain	Mix Gain
I <sub>CC</sub> Total	25.82	1	1	1	1	1
LNA Off	18.77	1	1	1	0	1
Mixer Preamp Off	14.28	1	1	1	0	0
V <sub>CC2</sub> Off	10.05	1	0	1	0	0
Mixer Current	7.72	1	0	1	0	0

Therefore,

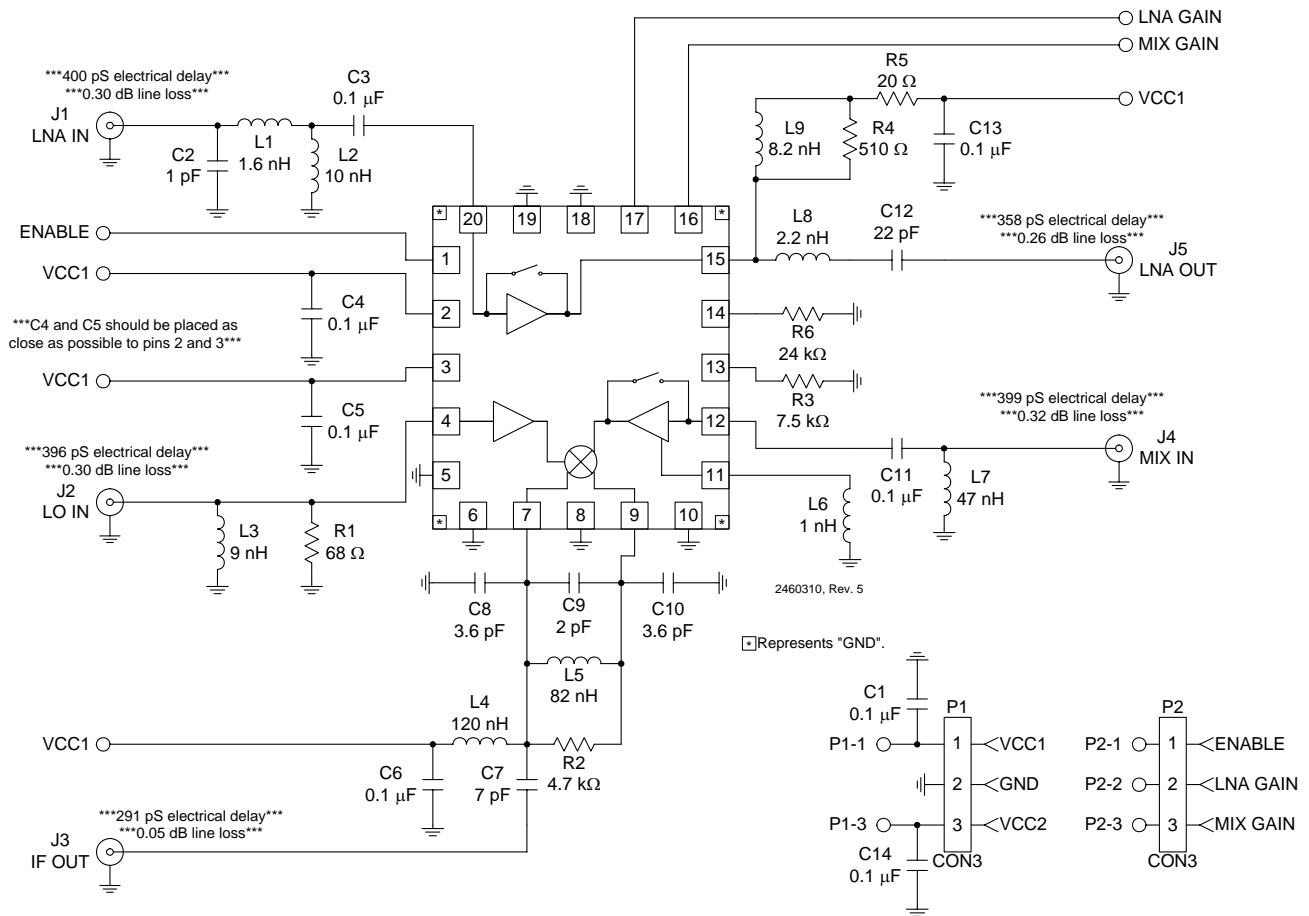
$$\begin{array}{rcl}
 \text{LNA (Bypass) = (Computer Simulation)} & = & 0\text{mA} \\
 \text{LNA (High Gain) = } & 25.82 - 18.77 & = 7.05\text{mA} \\
 \text{Mixer (Preamp) = } & 18.77 - 14.28 & = 4.49\text{mA} \\
 \text{Mixer = (Measured)} & = & 7.70\text{mA} \\
 \text{Bias = } & 10.05 - 7.7 & = 2.35\text{mA} \\
 \text{LO Circuitry (V}_{CC2}\text{) = } & 14.28 - 10.05 & = 4.23\text{mA} \\
 & & \hline
 & & 25.82\text{mA}
 \end{array}$$

## Evaluation Board Schematic US-PCS, IF = 210MHz (Download [Bill of Materials](http://www.rfmd.com) from www.rfmd.com.)



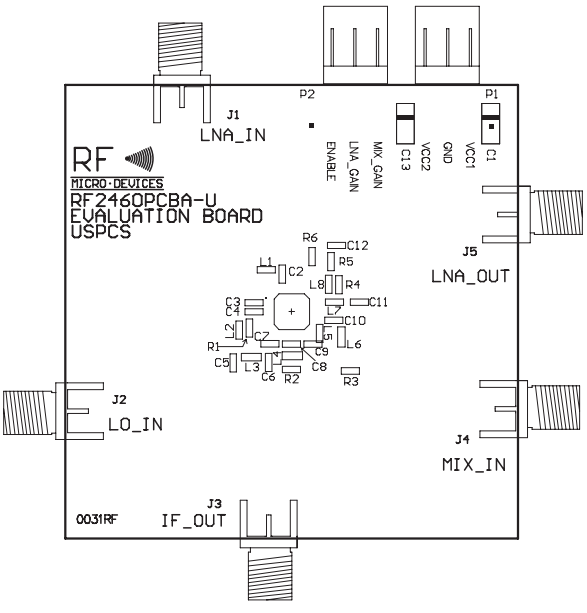
# RF2460

## Evaluation Board Schematic Korean-PCS, IF = 220MHz

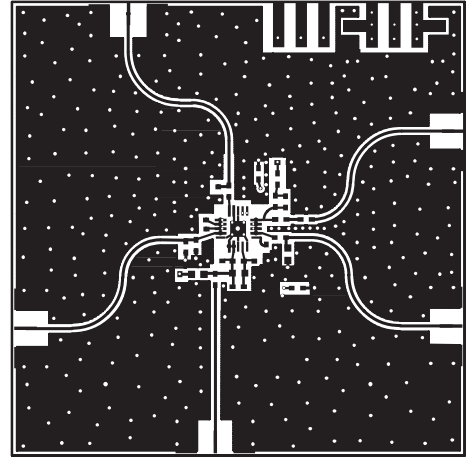
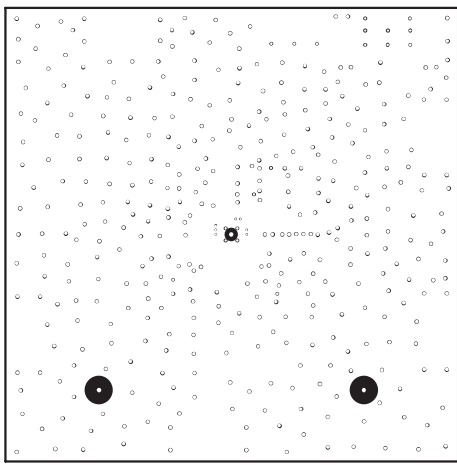


**Evaluation Board Layout - US PCS  
Board Size 2.0" x 2.0"**

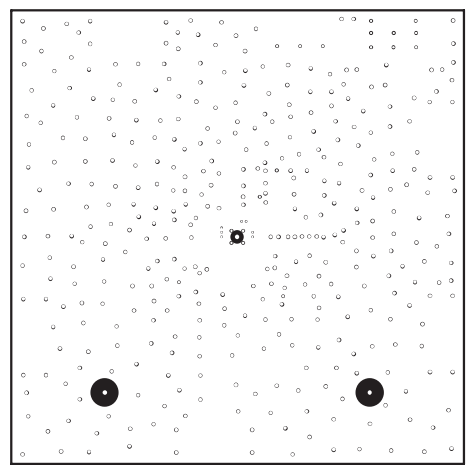
Board Thickness 0.034", Board Material FR-4, Multi-Layer  
Assembly Top



Power Plane 1



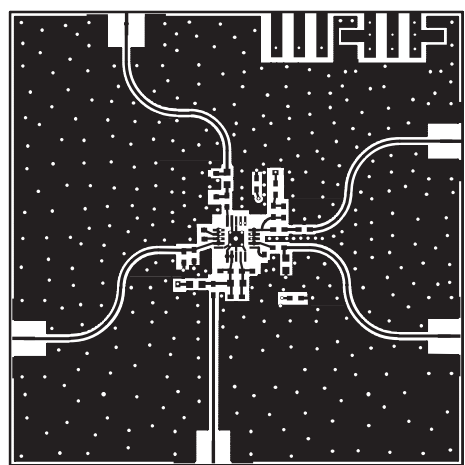
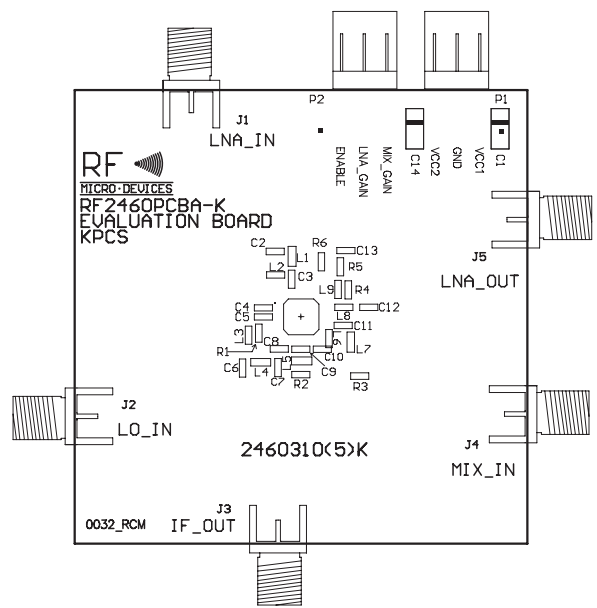
Power Plane 2



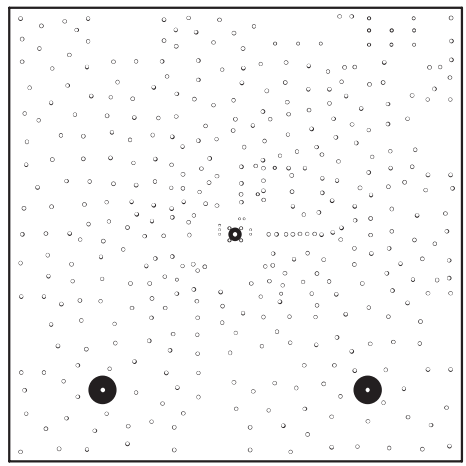




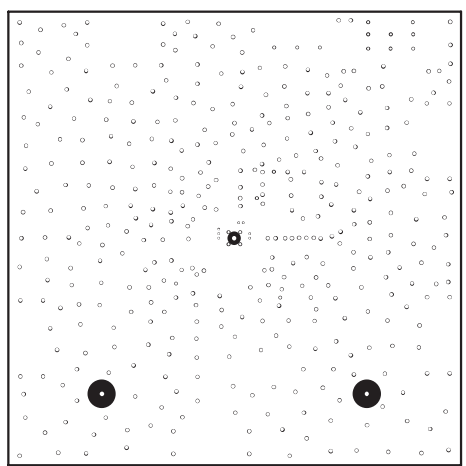
## Evaluation Board Layout - Korean PCS



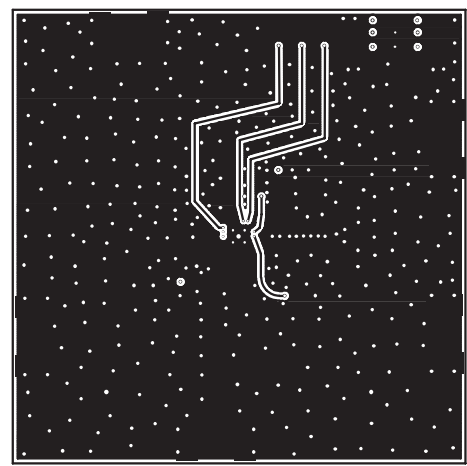
Power Plane 1



Power Plane 2

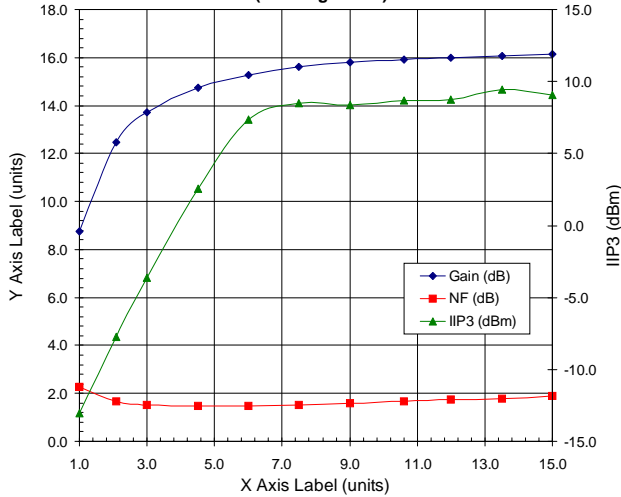


Back

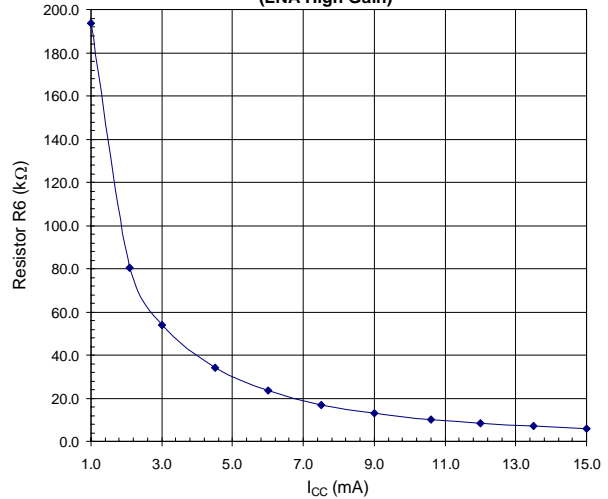


## US-PCS

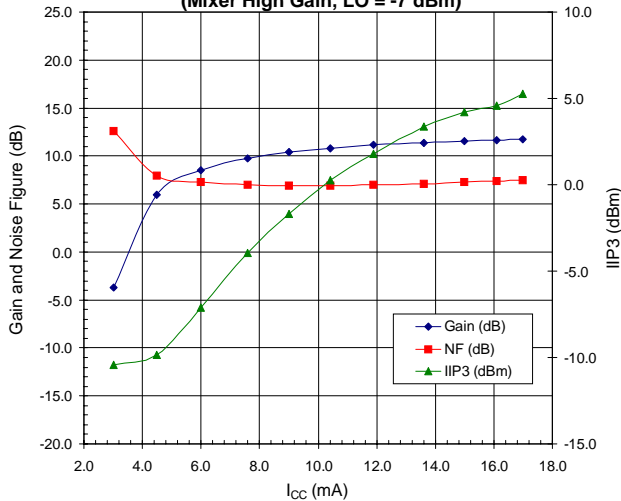
**LNA Gain, Noise Figure and IIP3 versus  $I_{CC}$  - LNA Only**  
(LNA High Gain)



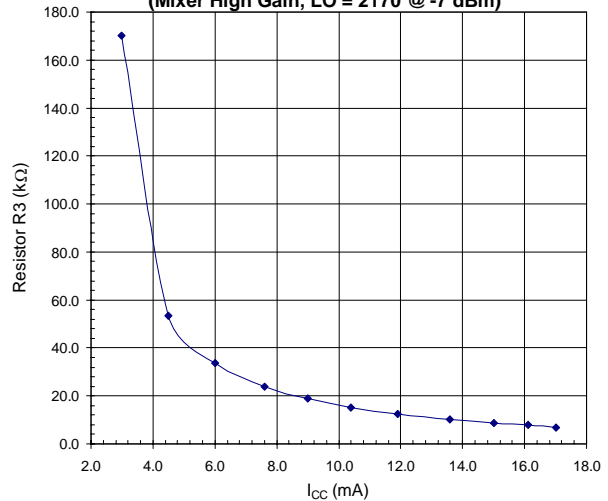
**Resistor (R6) versus  $I_{CC}$  (mA) - LNA Only**  
(LNA High Gain)



**Mixer Gain, Noise Figure and IIP3 versus  $I_{CC}$  - Mixer**  
(Mixer High Gain, LO = -7 dBm)



**Resistor (R3) versus  $I_{CC}$  - Mixer**  
(Mixer High Gain, LO = 2170 @ -7 dBm)



### Special Instructions (Board loss, taking into consideration description in the schematic)

#### LNA

$V_{CC1} = V_{CC2} = \text{Enable} = 2.75\text{V}$ ; Mix Gain = 0.0V

To measure  $I_{CC}$  LNA only:

LNA Gain was switched between 0V and 2.75V, and record the delta current.

#### Mixer

$V_{CC1} = V_{CC2} = \text{Enable} = \text{Mix Gain} = 2.75\text{V}$ ; LNA Gain = 0.0V

To measure  $I_{CC}$  Mixer (LNA should be in bypass mode and LO signal should be present):

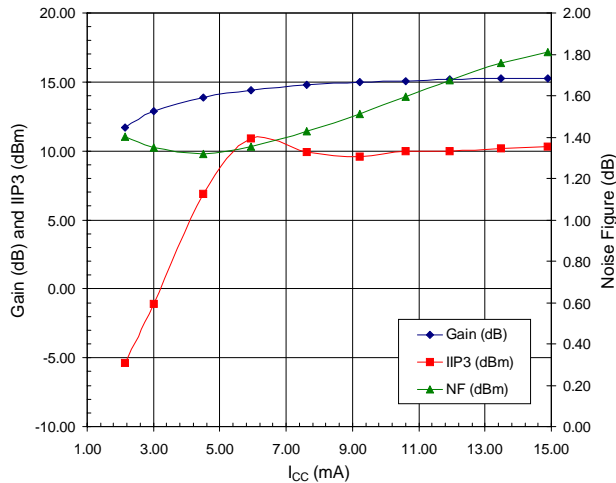
Mixer Current = Total IC Current - LO Circuitry (~4.23mA) (See "Current Measurement" section for more details)

$V_{CC2}$  only affects LO current buffer and R6 doesn't affect the mixer current.

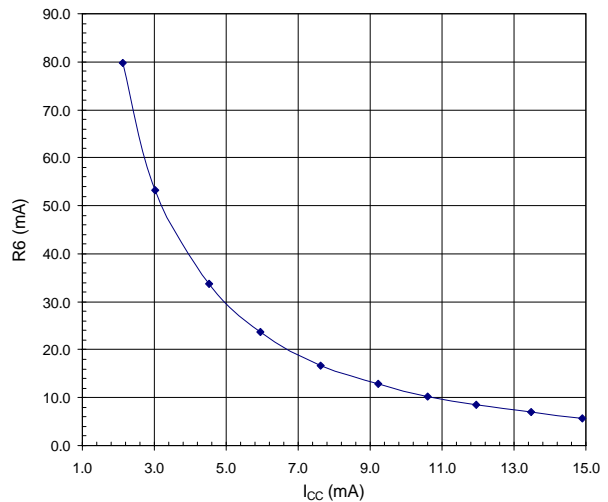
## W-CDMA

(See W-CDMA Application Schematic)

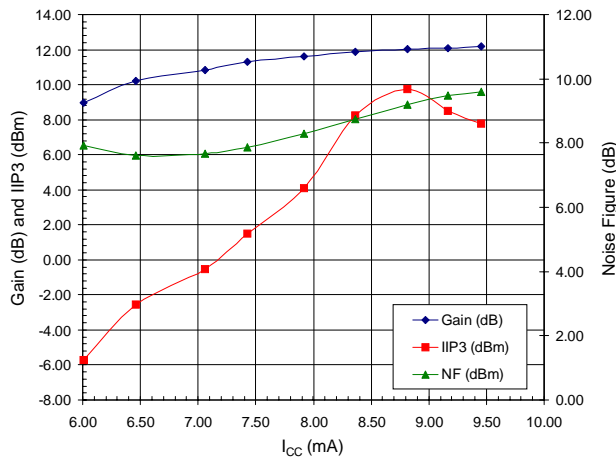
**LNA Gain, Noise Figure, and IIP3 versus  $I_{CC}$  - LNA Only**  
(LNA High Gain)



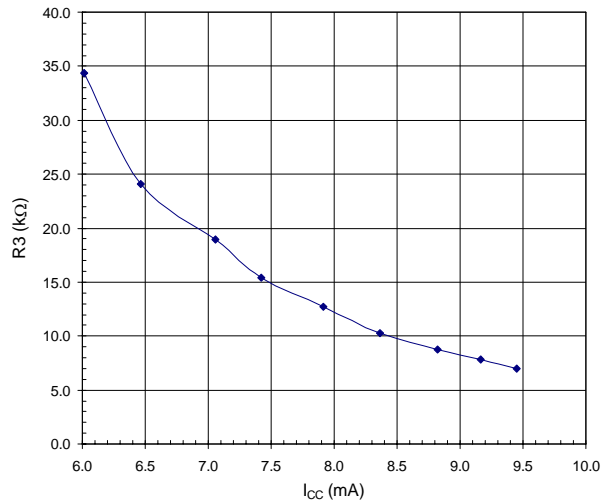
**R6 versus  $I_{CC}$  for LNA**



**Mixer Gain, Noise Figure and IIP3 versus  $I_{CC}$  - Mixer and Bias Circuits**  
(Mixer High Gain, LO=-7dBm)



**R3 versus  $I_{CC}$  for Mixer and Bias Circuits**



**Instructions** (Board loss, taking into consideration description in the W-CDMA schematic)

LNA

$I_{CC}$  LNA current=total current ( $V_{CC}$ =LNA Gain=2.75)-total current ( $V_{CC}$ =2.75; LNA Gain=0)

To measure  $I_{CC}$  LNA only:

LNA Gain was switched between 0V and 2.75V, and record the delta current.

Mixer

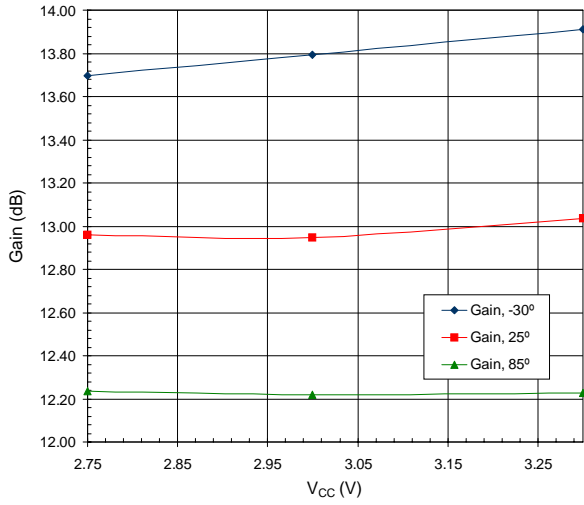
$I_{CC}$  Mix and Bias Current=Total Current ( $V_{CC1}$ =EN= $V_{CC2}$ =Mix Gain=2.75; LNA Gain=0)-total current ( $V_{CC1}$ =EN=2.75; Mix Gain=LNA Gain= $V_{CC2}$ =0)

LO signal should be present.  $V_{CC2}$  only affects LO current buffer and R6 doesn't affect the mixer current.

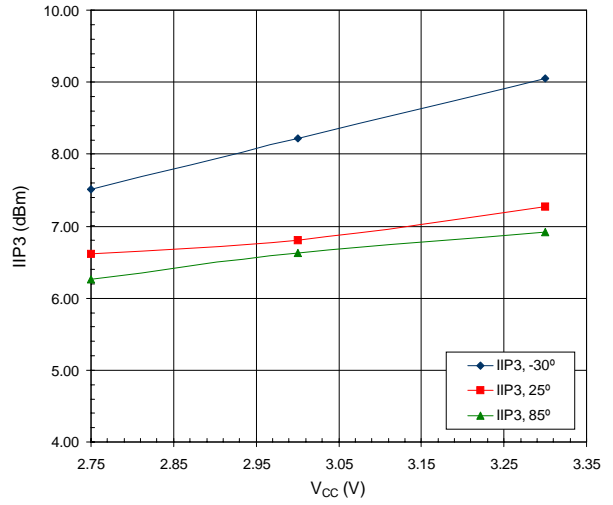
# RF2460

By using a R6=39kΩ and R3=24kΩ, the following results were obtained. RF=2140MHz, LO=2330MHz, IF=190MHz.

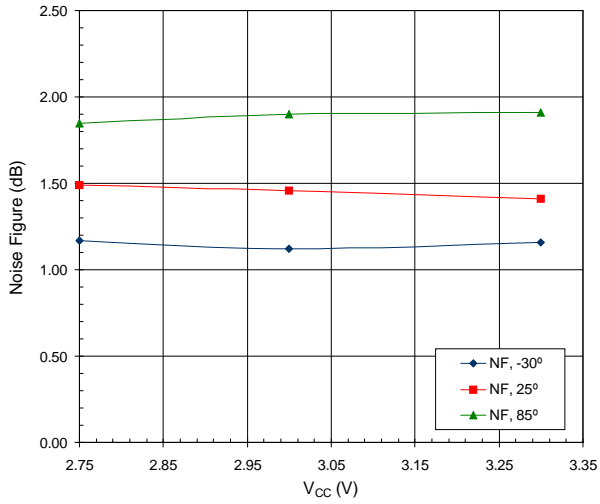
LNA (High Gain Mode) WCDMA



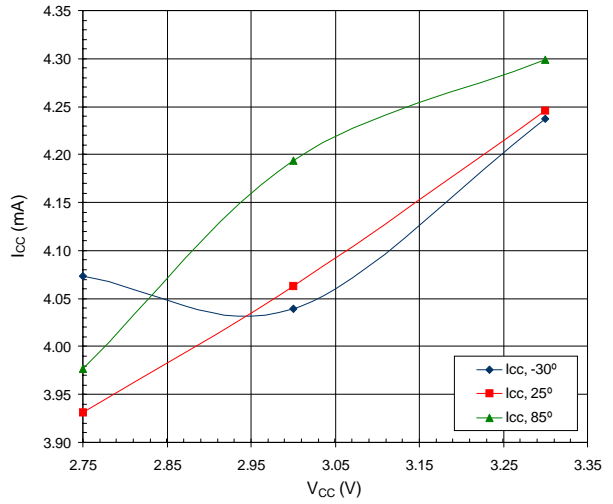
LNA (High Gain Mode) W-CDMA



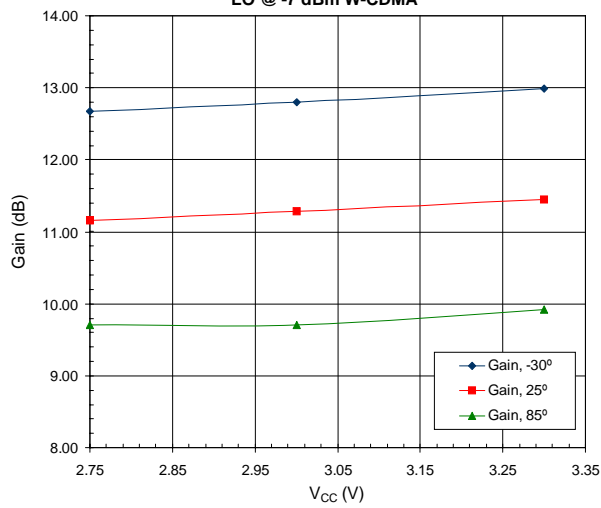
LNA (High Gain Mode) W-CDMA



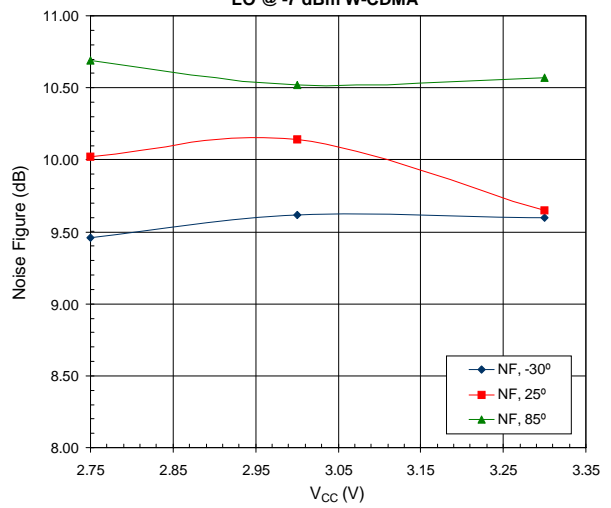
LNA Current W-CDMA



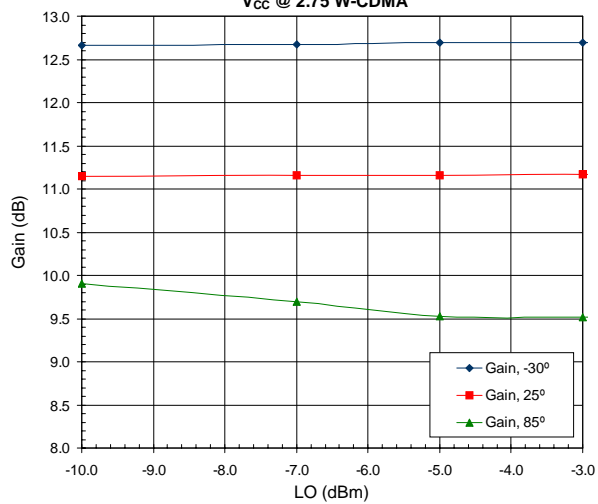
**Mixer High Gain Mode,  
LO @ -7 dBm W-CDMA**



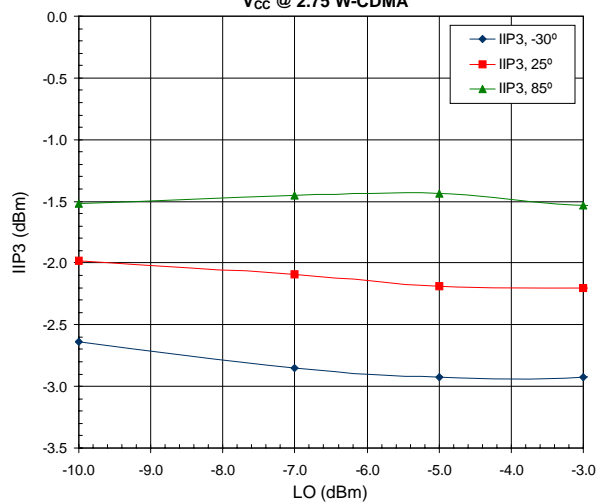
**Mixer High Gain Mode,  
LO @ -7 dBm W-CDMA**



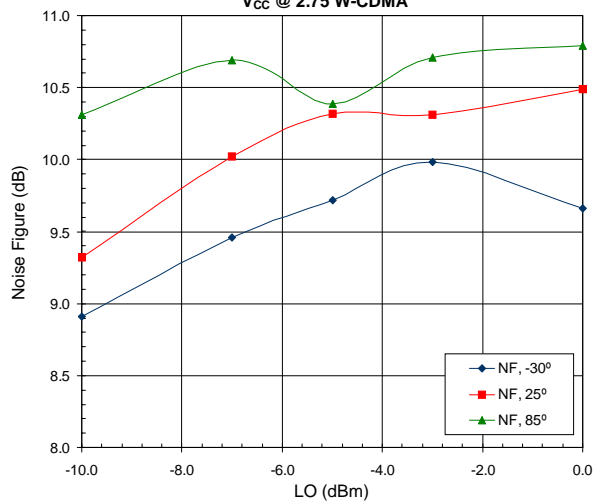
**Mixer High Gain Mode,  
V<sub>CC</sub> @ 2.75 W-CDMA**



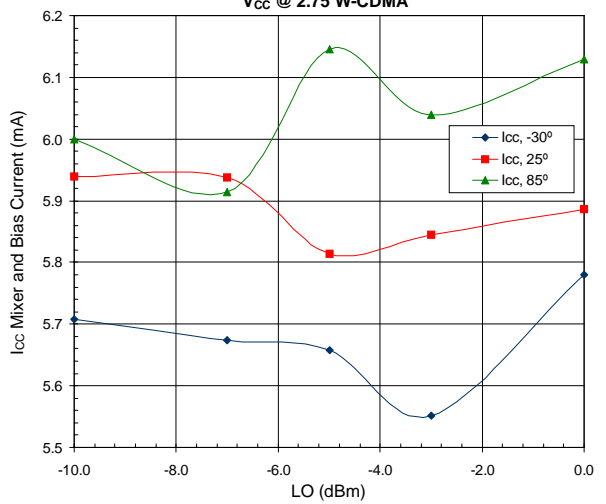
**Mixer IF High Gain Mode,  
V<sub>CC</sub> @ 2.75 W-CDMA**



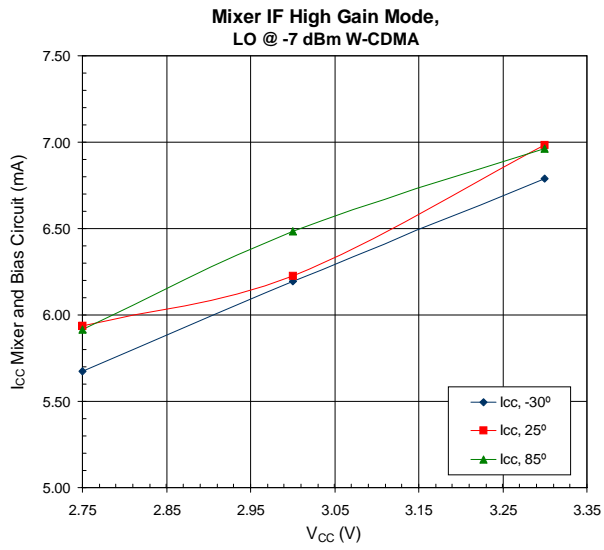
**Mixer IF High Gain Mode,  
V<sub>CC</sub> @ 2.75 W-CDMA**



**Mixer IF High Gain Mode,  
V<sub>CC</sub> @ 2.75 W-CDMA**



# RF2460



## PCB Design Requirements

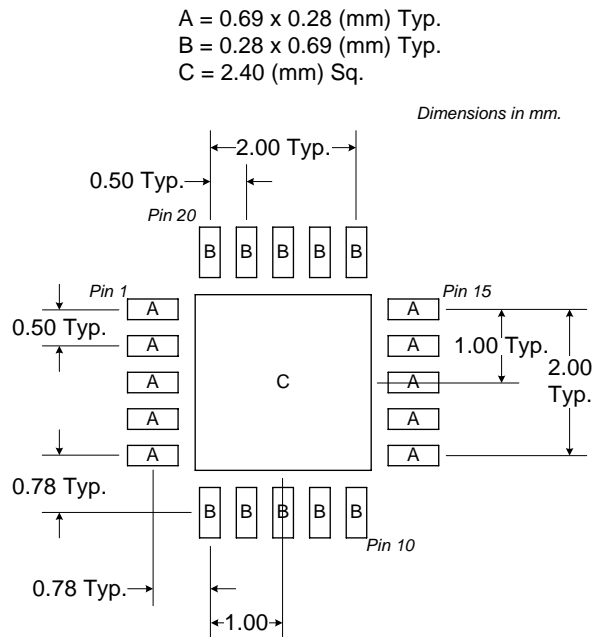
### PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

### PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

### PCB Metal Land Pattern



**Figure 1. PCB Metal Land Pattern (Top View)**

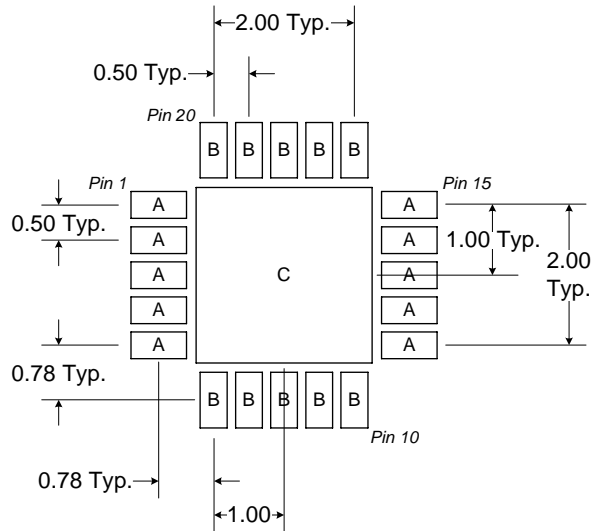
# RF2460

## PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

A = 0.79 x 0.38 (mm) Typ.  
B = 0.38 x 0.79 (mm) Typ.  
C = 2.50 (mm) Sq.

*Dimensions in mm.*



**Figure 2. PCB Solder Mask Pattern (Top View)**

## Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.