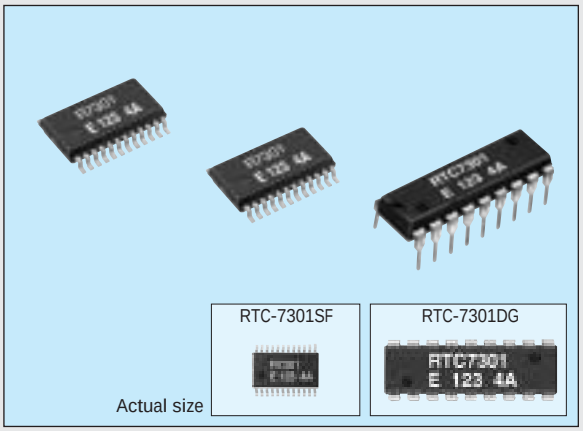
4-bit REAL TIME CLOCK MODULE

RTC-7301SF/DG

Product number (please refer to page 2)

Q4273018x000200
Q4273011x000200

- Built-in crystal oscillator 32.768 kHz with frequency adjusted
- Frequency selectable clock output (32.768 kHz to 1/30 Hz)
- Built-in 30 second adjustment function, digital pace adjustment function (Max. adjustment: ±192 x 10^{-6})
- Built-in alarm and timer interrupt functions.
- Built-in semiconductor temperature sensor (Voltage output: -7.8 mV / °C, RTC-7301SF)
- Operating voltage range:2.4 V to 5.5 V, time keeping voltage range: 1.6 V to 5.5 V
- Low current consumption (0.6 µA / 3 V Typ.)
- High speed parallel interface compatible with SRAM



The details are mentioned in the application manual.

http://www.epsondevice.com

Specifications (characteristics)

Absolute Max. ratings

GND=0V

Item	Symbol	Condition	Min.	Max.	Unit
Supply voltage	V_{DD}	V_{DD} to GND	-0.3	+ 7.0	V
Input voltage	V_{IN}	Input terminal,D0 to D3 pins	GND -0.3	V_{DD}+ 0.3	
Output voltage(1)	V_{OUT1}	$\overline{IRQ}$ pin	GND -0.3	+ 8.0	
Output voltage(2)	V_{OUT2}	FOUT, D0-D3 pins, VTEMP pin	GND -0.3	V_{DD}+ 0.3	
Storage temperature	T_{STG}	Stored as bare product after unpacking	-55	+125	°C

Operating conditions

GND=0V

Item	Symbol	Condition	Min.	Max.	Unit
Power voltage	V_{DD}	——	2.4	5.5	V
Clock voltage	V_{CLK}	——	1.6	5.5	V
Operating temperature	T_{OPR}	No condensation	- 40	+ 85	°C

Frequency characteristics

Item	Symbol	Condition	Range	Unit
Frequency precision	Δf/fo	Ta=+25 °C, V_{DD}= 3.0 V	5 ± 23 *	x 10^{-6}
Oscillation start-up time	t_{STA}	Ta=+25 °C, V_{DD}= 2.4 V	3 Max.	s
Frequency temperature characteristics	T_{OP}	Ta=-10 °C to +70 °C, V_{DD}= 3.0 V	+10/-120	x 10^{-6}
Frequency voltage characteristics	f/V	Ta=+25 °C, V_{DD}= 1.6 V to 5.5V	±2	x 10^{-6}/V
Aging	fa	Ta=+25 °C, V_{DD}= 3.0 V	±5	x 10^{-6}/year

* Please ask tighter tolerance

DC characteristics

GND=0 V,V_{DD}=1.6 V to 5.5 V,Ta= - 40 °C to + 85 °C

Item	Symbol		Condition	Min.	Typ.	Max.	Unit
Current consumption (When non-accessed) FOUT =Output OFF VTEMP =Output OFF	I_{DD1}	V_{DD}= 5 V	$\overline{CS0}$,$\overline{RD}$,$\overline{WR}$=V_{DD} A0-A3,CS1=GND D0-D3,IRQ=Hi-z FOUT=Hi-z(OFF) V_{TEMP}=Hi-z(OFF)	—	1.0	2.0	µA
	I_{DD2}	V_{DD}= 3 V		—	0.6	1.0	µA

Note)There is no VTEMP pin on the RTC-7301DG so standards for the VTEMP pin within the conditions described above do not apply.

Temperature sensor characteristics

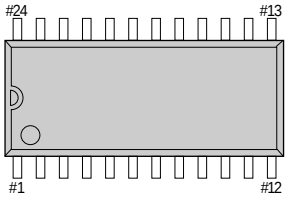
GND=0 V,Ta= - 40 °C to + 85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Temperature output voltage	VTEMP	Ta= +25 °C, GND based output voltage VTEMP pins, V_{DD}=2.7 V to 5.5 V		1.470		V
Output precision	T_{ACR}	Ta= +25 °C, V_{DD}=2.7 V to 5.5 V			±5.0	°C
Temperature sensitivity	V_{SE}	-40 °C ≤ Ta ≤ +85 °C, V_{DD}=2.7 V to 5.5 V	-7.3	-7.8	-8.3	mV/°C
Linearity	ΔNL	-40 °C ≤ Ta ≤ +85 °C, V_{DD}=2.7 V to 5.5 V			±2.0	%
Temperature detection range	T_{SOP}	ΔNL ≤ ± 2.0 %, V_{DD}=2.7 V to 5.5 V	-40		+85	°C
Output resistance	R_O	Ta= +25 °C, VTEMP pins, V_{DD}=2.7 V to 5.5 V GND standard and V_{DD} standard		1.0	3.0	kΩ
Load condition	C_L	V_{DD}=2.7 V to 5.5 V			100	pF
	R_L	V_{DD}=2.7 V to 5.5 V	500			kΩ
Response time	t_{RSP}	V_{DD}=3.3 V C_L=50 pF, R_L= 500 kΩ, Max. ±1 °C			200	µs

Note)There is no temperature sensor function on the RTC-7301DG.

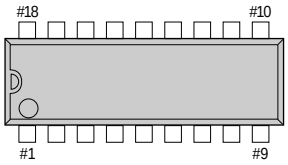
Terminal connection

RTC-7301SF



No.	Pin terminal	No.	Pin terminal
1	$\overline{CS_0}$	24	V_{DD}
2	F_{CON}	23	(V_{DD})
3	F_{OUT}	22	(V_{DD})
4	VTEMP	21	(V_{DD})
5	(V_{DD})	20	(V_{DD})
6	$\overline{IRQ}$	19	(V_{DD})
7	A_0	18	CS_1
8	A_1	17	D_0
9	A_2	16	D_1
10	A_3	15	D_2
11	$\overline{RD}$	14	D_3
12	GND	13	$\overline{WR}$

RTC-7301DG



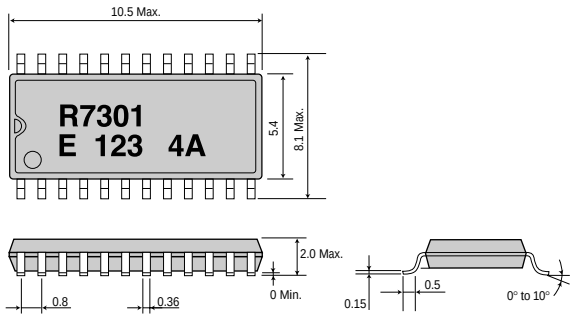
No.	Pin terminal	No.	Pin terminal
1	$\overline{CS_0}$	18	V_{DD}
2	FOUT	17	(V_{DD})
3	$\overline{IRQ}$	16	(V_{DD})
4	A_0	15	CS_1
5	A_1	14	D_0
6	A_2	13	D_1
7	A_3	12	D_2
8	$\overline{RD}$	11	D_3
9	GND	10	$\overline{WR}$

● (V_{DD}) and V_{DD} are to have the same level of voltage. Do not connect it to any external terminals.

External dimensions

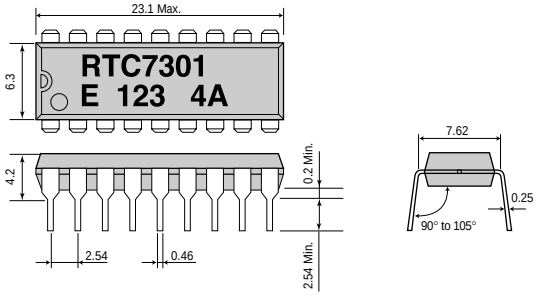
(Unit: mm)

RTC-7301SF (SSOP 24-pin)



Metal may be exposed on the top or bottom of this product. This won't affect any quality, reliability or electrical spec.

RTC-7301DG (DIP 18-pin)



Register table

Bank0 Clock and calendar registers

Address	Register	bit 3	bit 2	bit 1	bit 0
0	1 second digit	8	4	2	1
1	10 second digit	Fos	40	20	10
2	1 minute digit	8	4	2	1
3	10 minute digit	o	40	20	10
4	1hour digit	8	4	2	1
5	10 hour digit	o	o	20	10
6	Day digit	o	4	2	1
7	1 day digit	8	4	2	1
8	10 day digit	o	o	20	10
9	1 month digit	8	4	2	1
A	10 month digit	o	o	o	10
B	1 year digit	8	4	2	1
C	10 year digit	80	40	20	10
D	100 year digit	800	400	200	100
E	1000 year digit	TEST	TEMP	2000	1000
F	Control registers	Bank Sel 1	Bank Sel 0	STOP	BUSY/ADJ

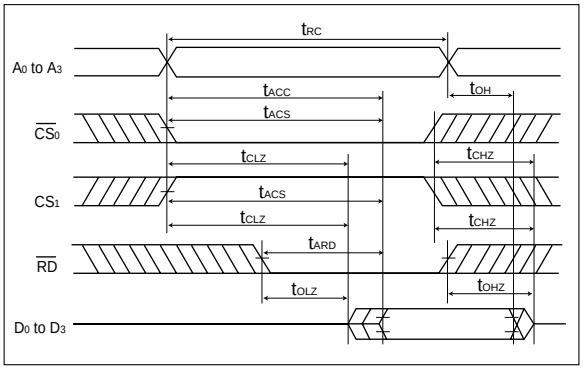
Bank1 Alarms and FOUT registers

Address	Register	bit 3	bit 2	bit 1	bit 0
0	1 second digit	8	4	2	1
1	10 second digit	AE	40	20	10
2	1 minute digit	8	4	2	1
3	10 minute digit	AE	40	20	10
4	1hour digit	8	4	2	1
5	10 hour digit	AE	•	20	10
6	Day digit	AE	4	2	1
7	1 day digit	8	4	2	1
8	10 day digit	AE	•	20	10
9	—	•	•	•	•
A	—	•	•	•	•
B	CS1 Controller	CTEMP	CDT_ON	•	•
C	FOUT divider ratio setting register	o	FD2	FD1	FD0
D	FOUT divider ratio setting register	FE	o	FD4	FD3
E	Alarm control	TEST	TEMP	AF	AIE
F	Control register	Bank Sel 1	Bank Sel 0	STOP	BUSY/ADJ

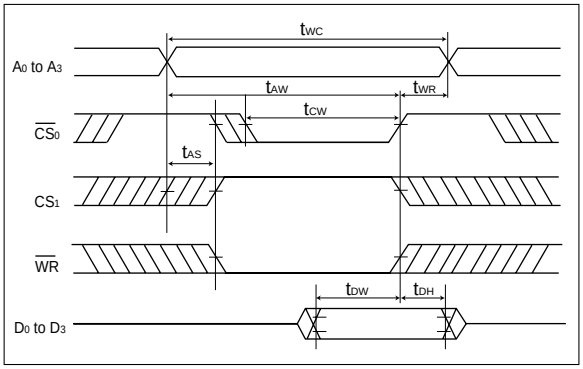
Bank2 Digital offset and timer registers

Address	Registers	bit 3	bit 2	bit 1	bit 0
0	Digital offset	DT3	DT2	DT1	DT0
1		DT_ON	DT6	DT5	DT4
2	—	o	o	o	o
3	—	o	o	o	o
4	Timer counter	8	4	2	1
5	preset value	128	64	32	16
6	Timer counter	8	4	2	1
7	data	128	64	32	16
8	Timer settings	TE	TI/TP	TD1	TD0
9	—	o	o	o	o
A	—	o	o	o	o
B	—	o	o	o	o
C	—	o	o	o	o
D	—	o	o	o	o
E	Timer control	TEST	TEMP	TF	TIE
F	Control register	Bank Sel 1	Bank Sel 0	STOP	BUSY/ADJ

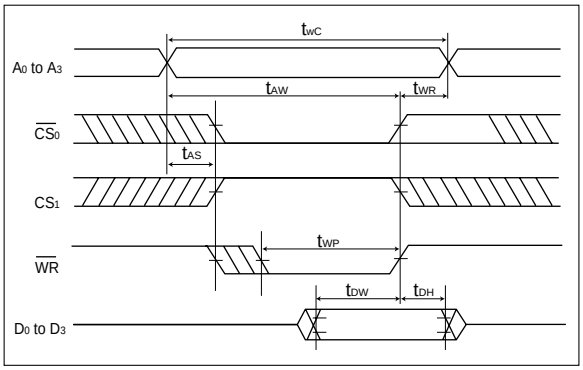
Reading data



Writing data (CS Control)



Writing data (WR Control)

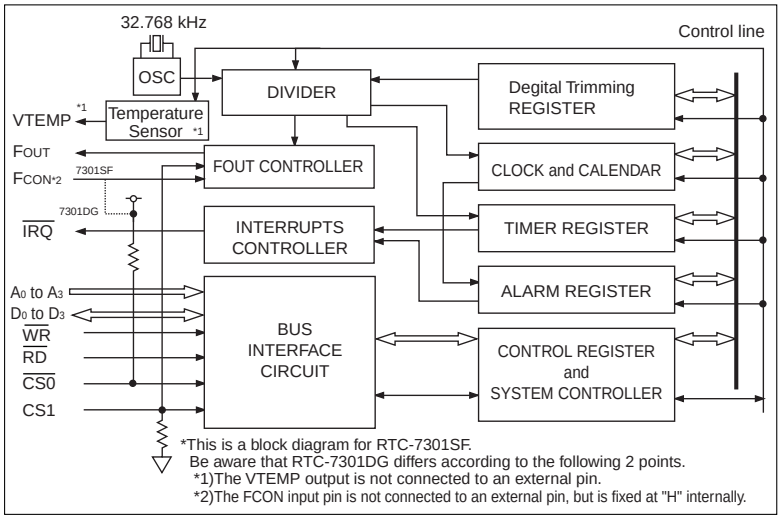


AC characteristics

•GND=0 V, Ta= -40 °C to + 85 °C •Input conditions: VI= 0.5 x VDD, VO= 0.5 x VDD •Output load: CL= 100 pF (tACC,tACS,tARD)

Item	Symbol	Condition	VDD=2.4 to 3.6 V		VDD=4.5 to 5.5 V		Unit
			Min.	Max.	Min.	Max.	
Read cycle time	tRC	—	150	—	85	—	ns
Address access time	tACC	—	—	150	—	85	ns
CE access time	tACS	—	—	150	—	85	ns
RD access time	tARD	—	—	100	—	45	ns
CE output set time	tCLZ	—	5	—	3	—	ns
CE output floating	tCHZ	—	—	60	—	30	ns
RD output set time	tOLZ	—	5	—	3	—	ns
RD output floating	tOHZ	—	—	60	—	30	ns
Output hold time	tOH	—	10	—	5	—	ns
Write cycle time	tWC	—	150	—	85	—	ns
Chip select time	tCW	—	140	—	70	—	ns
Address valid end of write	tAW	—	140	—	70	—	ns
Address setup time	tAS	—	0	—	0	—	ns
Address hold time	tWR	—	0	—	0	—	ns
Write pulse width	tWP	—	130	—	65	—	ns
Input data set time	tDW	—	80	—	35	—	ns
Input data hold time	tDH	—	0	—	0	—	ns
FOUT output frequency duty	DUTY	FOUT= 32.768 kHz	40	60	40	60	%

Block diagram



*This is a block diagram for RTC-7301SF.
Be aware that RTC-7301DG differs according to the following 2 points.
*1)The VTEMP output is not connected to an external pin.
*2)The FCON input pin is not connected to an external pin, but is fixed at "H" internally.