WHITE ELECTRONIC DESIGNS

WED416S8030A-SI

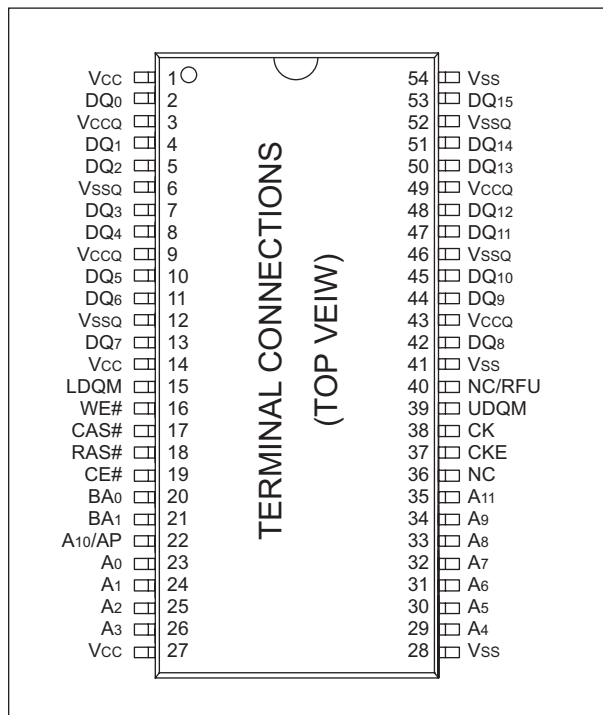# 2Mx16x 4 Banks Synchronous DRAM

FEATURES

- Single 3.3V power supply
- Fully Synchronous to positive Clock Edge
- SDRAM CAS Latentcy = 3 (100MHz), 2 (83MHz)
- Burst Operation
  - Sequential or Interleave
  - Burst length = programmable 1,2,4,8 or full page
  - Burst Read and Write
  - Multiple Burst Read and Single Write
- DATA Mask Control per byte
- Auto Refresh (CBR) and Self Refresh
  - 4096 refresh cycles across 64ms
- Automatic and Controlled Precharge Commands
- Suspend Mode and Power Down Mode

DESCRIPTION

The WED416S8030AxxSI is 134,217,728 bits of synchronous high data rate DRAM organized as 4 x 2,097, 152 words x 16 bits. Synchronous design allows precise cycle control with the use of system clock, I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.
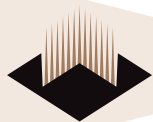
Available in a 54 pin TSOP type II package the WED416S4030AxxSI is tested over the industrial temp range (-40°C to +85°C) providing a solution for rugged main memory applications.
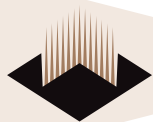
PIN CONFIGURATIONS

TERMINAL CONNECTIONS (TOP VEIW)

Pin	Signal		Pin	Signal
1	Vcc		54	Vss
2	DQ$_0$		53	DQ$_{15}$
3	Vccq		52	Vssq
4	DQ$_1$		51	DQ$_{14}$
5	DQ$_2$		50	DQ$_{13}$
6	Vssq		49	Vccq
7	DQ$_3$		48	DQ$_{12}$
8	DQ$_4$		47	DQ$_{11}$
9	Vccq		46	Vssq
10	DQ$_5$		45	DQ$_{10}$
11	DQ$_6$		44	DQ$_9$
12	Vssq		43	Vccq
13	DQ$_7$		42	DQ$_8$
14	Vcc		41	Vss
15	LDQM		40	NC/RFU
16	WE#		39	UDQM
17	CAS#		38	CK
18	RAS#		37	CKE
19	CE#		36	NC
20	BA$_0$		35	A$_{11}$
21	BA$_1$		34	A$_9$
22	A$_{10}$/AP		33	A$_8$
23	A$_0$		32	A$_7$
24	A$_1$		31	A$_6$
25	A$_2$		30	A$_5$
26	A$_3$		29	A$_4$
27	Vcc		28	Vss

PIN DESCRIPTION

CLK	Clock Input
CKE	Clock Enable
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CE#	Chip Select
A0-A11	Address Inputs
BA0, BA1	Bank Select Address
DQ0-DQ15	Data Input/Output
L(U)DQM	Data Input/Output Mask
Vcc	Power (+3.3V ±10%)
Vccq	Data Output Power
Vss	Ground
Vssq	Data Output Ground
NC	No Connection

INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Signal	Polarity	Function
CK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CK signal when high and deactivates the CK signal when low. By deactivating the clock, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
CE#	Input	Pulse	Active Low	CE# disable or enable device operation by masking or enabling all inputs except CK, CKE and DQM.
RAS#, CAS#, WE#	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, CAS#, RAS#, and WE# define the operation to be WE executed by the SDRAM.
BA0, BA1	Input	Level	-	Selects which SDRAM bank is to be active.
A0-11, A10/AP	Input	Level	-	During a Bank Activate command cycle, A0-11 defines the row address (RA0-11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-8 defines the column address (CA0-8) when sampled at the rising clock edge. In addition to the row address, A10/AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If A10/AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged . If A10/AP is low, autoprecharge is disabled. During a Precharge command cycle, A10/AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If A10/AP is high, all banks will be precharged regardless of the state of BA0, BA1. If A10/AP is low, then BA0, BA1 is used to define which bank to precharge.
DQ0-15	Input/Output	Level	-	Data Input/Output are multiplexed on the same pins.
L(U)DQM	Input	Pulse	Mask Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the Write operation if DQM is high.
V_{CC}, V_{SS}	Supply			Power and ground for the input buffers and the core logic.
V_{CCQ}, V_{SSQ}	Supply			Isolated power and ground for the output buffers to improve noise immunity.

WHITE ELECTRONIC DESIGNS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	-1.0	+4.6	V
Input Voltage	V_{IN}	-1.0	+4.6	V
Output Voltage	V_{OUT}	-1.0	+4.6	V
Operating Temperature	T_{OPR}	-40	+85	°C
Storage Temperature	T_{STG}	-55	+125	°C
Power Dissapation	P_D		1.0	W
Short Circuit Output Current	I_{OS}		50	mA

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Voltage Referenced to: V_{SS} = 0V, -40°C ≤ T_A ≤ +85°C

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	-0.3	—	+0.8	V	
Output High Voltage	V_{OH}	2.4	——	——	V	(I_{OH}=-2mA)
Output Low Voltage	V_{OL}	—	—	0.4	V	(I_{OL}=2mA)
Input Leakage Voltage	I_{IL}	-5	—	5	µA	
Output Leakage Voltage	I_{OL}	-5	—	5	µA	

Capacitance

T_A = 25°C, f = 1MHz, V_{CC} = 3.0V to 3.6V

Parameter	Symbol	Max	Unit
Input Capacitance (A0-11, BA0-1)	C_{I1}	4	pF
Input Capacitance (CK, CKE, RAS#, CAS# WE#, CE#, L(U)DQM)	C_{I2}	4	pF
Input/Output Capacitance (DQ0-15)	C_{OUT}	5	pF

OPERATING CURRENT CHARACTERISTICS

V_{CC} = 3.3V, = -40°C ≤ T_A ≤ +85°C

Parameter	Symbol	Test Conditions	-10	-12	Units	Notes
Operating Current (One Bank Active)	I_{CC1}	Burst Length = 1, t_{RC} ≥ t_{RC} =min	140	125	mA	1
Operating Current (Burst Mode)	I_{CC4}	Page Burst, 2 banks active, t_{CCD} = 2 clocks	200	165	mA	1
Precharge Standby Current in Power Down Mode	I_{CC2P}	CKE ≤ V_{IL} (MAX), t_{CC} = 15ns	2	2	mA	
	I_{CC2PS}	CKE, CK ≤ V_{IL} (MAX), t_{CC} =∞, Input Stable	2	2	mA	
Precharge Standby Current in Non-Power Down Mode	I_{CC1N}	CKE = V_{IH}, t_{CC} = 15ns. Input Change every 30ns	50	50	mA	
	I_{CC1NS}	CKE ≤ V_{IH} (MIN), t_{CC} = ∞, No Input Change	35	35	mA	
Active Standby Current in Non-Power Down Mode	I_{CC3P}	CKE ≤ V_{IL} (MAX), t_{CC} = 15ns	12	12	mA	
	I_{CC3PS}	CKE ≤ V_{IL} (MAX), t_{CC} = ∞	12	12	mA	
Active Standby Current in Power Down Mode	I_{CC2N}	CKE = V_{IH}, t_{CC} = 15ns, Input Change every 30ns	30	30	mA	
	I_{CC2NS}	CKE ≤ V_{IH} (MIN), t_{CC} = ∞, No Input Change	20	20	mA	
Refresh Current	I_{CC5}	t_{RC} ≥ t_{RC} (Min)	210	210	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	3	3	mA	

NOTE:
1. Measured with outputs open.
2. Refresh period is 64ms.
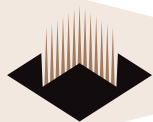
AC CHARACTERISTICS

OPERATING AC PARAMETERS
V_{CC} = 3.3V, = -40°C ≤ T_A ≤ +85°C

Parameter		Symbol	-10		-12		Units	Notes
			Min	Max	Min	Max		
Clock Cycle Time	CAS latency = 3	t_{CC}	10	1000	12	1000	ns	1
	CAS latency = 2		13	1000	15	1000	ns	
Clock to Valid Output Delay		t_{SAC}		7		8	ns	1, 2
Output Dta Hold Time		t_{OH}	3		3		ns	2
Clock High Pulse Width		t_{CH}	3.5		4.0		ns	3
Clock Low Pulse Width		t_{CL}	3.5		4.0		ns	3
Input Setup Time		t_{SS}	2.5		3		ns	3
Input Hold Time		t_{SH}	1		1		ns	3
Clock to Output in Low-Z		t_{SLZ}	1		1		ns	2
Clock to Output in High-Z		t_{SHZ}		7		8	ns	
Row Active to Row Active Delay		t_{RRD}	20		24		ns	4
RAS# to CAS# Delay		t_{RCD}	24		26		ns	4
Row Precharge Time		t_{RP}	24		26		ns	4
Row Active Time		t_{RAS}	50	100,000	60	100,000	ns	4
Row Cycle Time-Operation		t_{RC}	80		90		ns	4
Row Cycle Time-Auto Refresh		t_{RFC}	80		90		ns	4, 8
Last Data In to New Column Address Delay		t_{CDL}	1		1		CK	5
Last Data In to Row Precharge		t_{RDL}	1		1		CK	5
Last Data In to Burst Stop		t_{BDL}	1		1		CK	5
Colunm Address to Column Address Delay		t_{CCD}	1		1		CK	6
Number of Valid Output Data	CAS latency = 3		2		2		ea	7
	CAS latency = 2		1		1			

NOTES:
1. Parameters depend on programmed CAS latency.
2. If clock rise time is longer than 1ns, (t_{RISE}/2 - 0.5ns) should be added to the parameter.
3. Assumed input RISE and fall time = 1ns. If t_{RISE} & t_{FALL} are longer than 1ns, [(t_{RISE} + t_{FALL})/2-1ns] should be added to the parameter.
4. The minimum number of clock cycles required is determined by dividing the minimum time required by the clock cycle time and then rounding up to the next higher integer.
5. Minimum delay is required to complete write.
6. All devices allow every cycle column address changes.
7. In case of row precharge interrupt, auto precharge and read burst stop.
8. A new command may be given t_{RFC} after self refresh exit.

REFRESH CYCLE PARAMETERS

Parameter	Symbol	-10		-12		Units	Notes
		Min	Max	Min	Max		
Refresh Period	t_{REF}	-	64	-	64	ms	1, 2
Self Refresh Exit Time	t_{SREX}	t_{RFC}	-	t_{RFC}	-	ns	3

NOTES:
1. 4096 cycles.
2. Any time that the Refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to "wake-up" the device.
3. The self refresh is exited by restarting the external clock and then asserting CKE high. This must be followed by NOPs for a minimum time of t_{RFC} before the SDRAM reaches idle state to begin normal operation.

CLOCK FREQUENCY AND LATENCY PARAMETERS = 100MHz
(UNITS = NUMBER OF CLOCKS)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		80ns	50ns	24ns	20ns	24ns	10ns	10ns	10ns
100MHz (10.0ns)	3	8	5	3	2	3	1	1	1
83MHz (12.0ns)	3	7	5	2	2	2	1	1	1
75MHz (12.0ns)	2	6	4	2	2	2	1	1	1
66MHz (15.0ns)	2	6	4	2	2	2	1	1	1

CLOCK FREQUENCY AND LATENCY PARAMETERS = 83MHz
(UNITS = NUMBER OF CLOCKS)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		90ns	60ns	26ns	24ns	26ns	12ns	12ns	12ns
83MHz (12ns)	3	8	5	3	2	3	1	1	1
75MHz (12ns)	3	7	5	2	2	2	1	1	1
66MHz (15ns)	2	6	4	2	2	2	1	1	1
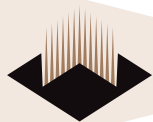
COMMAND TRUTH TABLE

Command		CKE		CE#	RAS#	CAS#	WE#	DQM	BA	A10/AP	A11, A9-0	Notes
		Previous Cycle	Current Cycle									
Register	Mode Register Set	H	X	L	L	L	L	X	OP CODE			
Refresh	Auto(CBR) Refresh	H	H	L	L	L	H	X	X	X	X	
	Entry Self Refresh		L									
Precharge	Single Bank	H	X	L	L	H	L	X	BA	L	X	2
	All Banks								X	H	X	
Bank Activate		H	X	L	L	H	H	X	BA	Row Address		2
Write	Auto Precharge Disable	H	X	L	H	L	L	X	BA	L	Column Address	2
	Auto Precharge Enable	H								H		2
Read	Auto Precharge Disable	H	X	L	H	L	H	X	BA	L	Column Address	2
	Auto Precharge Enable									H		2
Burst Stop		H	X	L	H	H	L	X	X	X	X	3
No Operation		H	X	L	H	H	H	X	X	X	X	
Device Deselect		H	X	H	X	X	X	X	X	X	X	
Clock Suspend/Standby Mode		L	X	X	X	X	X	X	X	X	X	4
Data	Write/Output Enable	H	X	X	X	X	X	L	X	X	X	5
	Mask/Output Disable							H				5
Power Down Mode	Entry	X	L	H	X	X	X	X	X	X	X	6
	Exit		H									6

(X = Don't Care, H = Logic High, L = Logic Low)

NOTES:

1. All of the SDRAM operations are defined by states of CE#, WE#, RAS#, CAS#, and DQM at the positive rising edge of the clock.
2. Bank Select (BA), if BA0, BA1 = 0, 0 then bank A is selected, if BA0, BA1 = 1, 0 then bank B, if BA0, BA1 = 0, 1 then bank C, if BA0, BA1 = 1, 1 then bank D is selected, respectively.
3. During a Burst Write cycle there is a zero clock delay, for a Burst Read cycle the delay is equal to the CAS latency.
4. During normal access mode, CKE is held high and CK is enabled. When it is low, it freezes the internal clock and extends data Read and Write operations. One clock delay is required for mode entry and exit.
5. The DQM has two functions for the data DQ Read and Write operations. During a Read cycle, when DQM goes high at a clock timing the data outputs are disabled and become high impedance after a two clock delay. DQM also provides a data mask function for Write cycles. When it activates, the Write operation at the clock is prohibited (zero clock latency).
6. All banks must be precharged before entering the Power Down Mode. The Power Down Mode does not perform any Refresh operations, therefore the device can't remain in this mode longer than the Refresh period (t_{REF}) of the device. One clock delay is required for mode entry and exit.
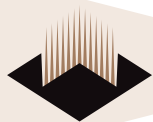
CLOCK ENABLE (CKE0) TRUTH TABLE

Current State	CKE		Command						Action	Notes
	Previous	Current	CE#	RAS#	CAS#	WE#	BA	A0-12		
Self Refresh	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Exit Self Refresh with Device Deselect	2
	L	H	L	H	H	H	X	X	Exit Self Refresh with No Operation	2
	L	H	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	L	X	X	X	ILLEGAL	2
	L	H	L	L	X	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Power Down Mode Exit, all bank idle	2
	L	H	L	X	X	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	X	Maintain Power Down Mode	
All Banks Idle	H	H	H	X	X	X			Refer to the Idle State section of the Current State Truth Table	3
	H	H	L	H	X	X				
	H	H	L	L	H	X				
	H	H	L	L	L	H	X	X	CBR Refresh	
	H	H	L	L	L	L	OP Code		Mode Register Set	4
	H	L	H	X	X	X			Refer to the Idle State section of the Current State Truth Table	3
	H	L	L	H	X	X				
	H	L	L	L	H	X				
	H	L	L	L	L	H	X	X	Entry Self Refresh	4
	H	L	L	L	L	L	OP Code		Mode Register Set	
	L	X	X	X	X	X	X	X	Power Down	4
Any State other than listed above	H	H	X	X	X	X	X	X	Refer to the Operations in the Current State Truth Table	
	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle	5
	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle	
	L	L	X	X	X	X	X	X	Maintain Clock Suspend	

NOTES:

1. For the given Current State CKE must be low in the previous cycle.
2. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. The minimum setup time for CKE (t_{CKS}) must be satisfied before any command other than Exit is issued.
3. The address inputs (A11-0) depend on the command that is issued. See the Idle State section of the Current State Truth Table for more information.
4. The Power Down Mode, Self Refresh Mode, and the Mode Register Set can only be entered from the all banks idle state. Must be a legal command as defined in the Current State Truth Table.
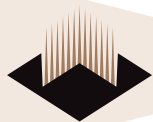5. Must be a legal command as defined in the Current State Truth Table.

CURRENT STATE TRUTH TABLE

Current State	CE#	RAS#	CAS#	WE#	BA	A11, A10/AP-A0	Description	Action	Notes
Idle	L	L	L	L		OP Code	Mode Register Set	Set the Mode Register	2
	L	L	L	H	X	X	Auto or Self Refresh	Start Auto or Self Refresh	2,3
	L	L	H	L	X	X	Precharge	No Operation	
	L	L	H	H	BA	Row Address	Bank Activate	Activate the specified bank and row	
	L	H	L	L	BA	Column	Write w/o Precharge	ILLEGAL	4
	L	H	L	H	BA	Column	Read w/o Precharge	ILLEGAL	4
	L	H	H	L	X	X	Burst Termination	No Operation	
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation or Power Down	5
Row Active	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Precharge	6
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	Start Write; Determine if Auto Precharge	7,8
	L	H	L	H	BA	Column	Read	Start Read; Determine if Auto Precharge	7,8
	L	H	H	L	X	X	Burst Termination	No Operation	
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation	
Read	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Terminate Burst; Start the Precharge	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	Terminate Burst; Start the Write cycle	8,9
	L	H	L	H	BA	Column	Read	Terminate Burst; Start a new Read cycle	8,9
	L	H	H	L	X	X	Burst Termination	Terminate the Burst	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Write	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Terminate Burst; Start the Prechage	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	Terminate Burst; Start a new Write cycle	8,9
	L	H	L	H	BA	Column	Read	Terminate Burst; Start the Read cycle	8,9
	L	H	H	L	X	X	Burst Termination	Terminate the Burst	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Read with Auto Precharge	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	

CURRENT STATE TRUTH TABLE (cont'd)

Current State	CE#	RAS#	CAS#	WE#	BA	A11, A10/AP-A0	Description	Action	Notes
Write with Auto Precharge	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Precharging	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	No Operation; Bank(s) idle after t_{RP}	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	ILLEGAL	4
	L	H	L	H	BA	Column	Read	ILLEGAL	4
	L	H	H	L	X	X	Burst Termination	No Operation; Bank(s) idle after t_{RP}	
	L	H	H	H	X	X	No Operation	No Operation; Bank(s) idle after t_{RP}	
	H	X	X	X	X	X	Device Deselect	No Operation; Bank(s) idle after t_{RP}	
Row Activating	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4,10
	L	H	L	L	BA	Column	Write	ILLEGAL	4
	L	H	L	H	BA	Column	Read	ILLEGAL	4
	L	H	H	L	X	X	Burst Termination	No Operation; Row active after t_{RCD}	
	L	H	H	H	X	X	No Operation	No Operation; Row active after t_{RCD}	
	H	X	X	X	X	X	Device Deselect	No Operation; Row active after t_{RCD}	
Write Recovering	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	Start Write; Determine if Auto Precharge	9
	L	H	L	H	BA	Column	Read	Start Write; Determine if Auto Precharge	9
	L	H	H	L	X	X	Burst Termination	No Operation; Row active after t_{DPL}	
	L	H	H	H	X	X	No Operation	No Operation; Row active after t_{DPL}	
	H	X	X	X	X	X	Device Deselect	No Operation; Row active after t_{DPL}	

CURRENT STATE TRUTH TABLE (cont'd)

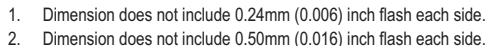| Current State	Command							Action	Notes
	CE#	RAS#	CAS#	WE#	BA	A11, A10/AP-A0	Description		
Write Recovering with Auto Precharge	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	4
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Column	Write	ILLEGAL	4,9
	L	H	L	H	BA	Column	Read	ILLEGAL	4,9
	L	H	H	L	X	X	Burst Termination	No Operation; Precharge after t_{DPL}	
	L	H	H	H	X	X	No Operation	No Operation; Precharge after t_{DPL}	
	H	X	X	X	X	X	Device Deselect	No Operation; Precharge after t_{DPL}	
Refreshing	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	No Operation; idle after t_{RC}	
	L	H	H	H	X	X	No Operation	No Operation; idle after t_{RC}	
	H	X	X	X	X	X	Device Deselect	No Operation; idle after t_{RC}	
Mode Register Accessing	L	L	L	L		OP Code	Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	No Operation; Idle after two clock cycles	
	H	X	X	X	X	X	Device Deselect	No Operation; Idle after two clock cycles	

NOTES:
1. CKE is assumed to be active (high) in the previous cycle for all entries. The Current State is the state of the bank that the command is being applied to.
2. All Banks must be idle otherwise it is an illegal action.
3. If CKE is active (high) the SDRAM starts the Auto (CBR) Refresh operation, if CKE is inactive (low) then the Self Refresh mode is entered.
4. The Current State refers only to one of the banks, if BA0, BA1 selects this bank then the action is illegal. If BA0, BA1 selects the bank not being referenced by the Current State then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low) then the Power Down mode is entered, otherwise there is a No Operation.
6. The minimum and maximum Active time (t_{RAS}) must be satisfied.
7. The RAS# to CAS# Delay (t_{RCD}) must occur before the command is given.
8. Address A10 is used to determine if the Auto Precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements. The command is illegal if the minimum bank to bank delay time (t_{RRD}) is not satisfied.

ORDERING INFORMATION

Part Number	Organization	Operating Frequency	Height*
WED416S8030A10SI	2Mx16bitsx4banks	100MHz	11.76 (0.463")
WED416S8030A12SI	2Mx16bitsx4banks	83MHz	11.76 (0.463")

NOTE: This product does not include the prefix "WED" for part marking due to package size constraints.

PACKAGE OUTLINE, JEDEC MS-024-FA, ISSUE C

22.62 (0.89) MAX   Note 1

10.16 (0.40)
Note 2

11.76 ±0.20
(0.463 ±0.008)

0.80 (0.03)
TYP

0.35 ±0.10
(0.01 ±0.004)

VIEW A

1.20 (0.047)
MAX

0.05
(0.002)

0.75 (0.030)
0.45 (0.018)

SEE VIEW A

0 - 8

0.125 ±0.035
(0.005 ±0.001)

NOTES:
1. Dimension does not include 0.24mm (0.006) inch flash each side.
2. Dimension does not include 0.50mm (0.016) inch flash each side.

*ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

Document Title

2Mx16x 4 Banks Synchronous DRAM

Revision History

Rev #	History	Release Date	Status
Rev 1	Created	5-21-1999	Advanced
Rev 2	2.1 Changed from EDI to WED 2.2 Changed from Advanced to Preliminary	5-15-2000	Advanced Preliminary
Rev 3	3.1 Changed from Preliminary to Final	9-2000	Final
Rev 4	4.1 Changed to WEDC format 4.2 Added Document Title Page	10-2004	Final