TIGRIS is a high density data-termination device supporting 2047 channels operating at an aggregate rate of 2.488Gbps. The device aggregates and terminates both ATM cells and HDLC frames, enabling ATM services such as Cell Relay, IMA, AAL2/5, and frame based services, such as PPP, Frame Relay, and Multi-link PPP and Multi-link Frame Relay. The 2047 individually assignable channels can be configured for Frame Relay, HDLC, PPP, and or ATM services for DS0, NxDS0, DS1/E1, DS3/E3, STS-1c, STS-3c and STS-12c rates.

TIGRIS supports up to 48 channels of subrate DS3 services interoperating with major CSU/DSU vendors protocols and can be combined with AMCC's nP3700 to provide AAL2/5, IMA, and Multilink services for all 2047 channels.

Data Services and Performance Monitoring

- Store and forward architecture with extensive buffering using external DDR SDRAM.
- 2047 bi-directional ATM/HDLC channels that can be assigned to tributaries from STS-12 to DS0.
- Bit synchronous HDLC support all channels (DS3 and lower rate).
- Byte synchronous HDLC support for all channels (STS-1 and higher rate).
- Direct Map ATM support.
- G.832 E3 ATM support.
- Support for up to 48 DS3 PLCP ATM mapped channels.
- Support for up to 48 sub-rate DS3 channels.

FTI-2 Line Interface

- Four independent STS-12 capable interfaces selectable from four serial 622 MHz LVDS Flexible Tributary interfaces (FTI-2) or one Parallel FTI 8-bit x 78MHz Interface. Parallel Interface is compatible with standard Telecom Bus interfaces.

- An expansion mode allows multiple TIGRIS devices to share a single FTI interface (allows up to 8K channels).
- Glueless interface to up to four AMCC Evros framers.

System Interface

- SPI-3 32bit @ 104MHz for cells/packets and error status.
- The SPI-3 supports four interleaved channels (four logical PHY ports).
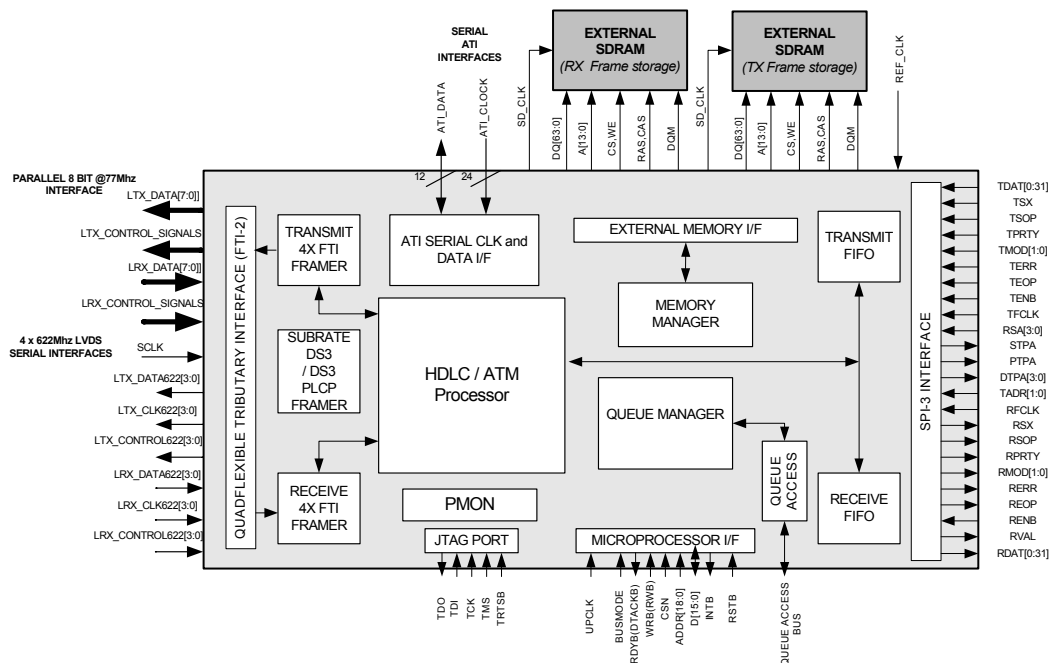- Pre-pended packet tag for channel ID, length, error status, TX queue priority, and TX per packet loopback.

Device Specifications

- 899 PBGA (31x31mm with 1mm ball pitch) package with Green/RoHS compliant option
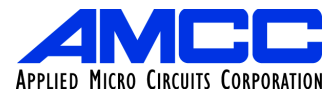- 1.2V core, 2.5V I/O
- 6.0W maximum power consumption

Figure 1: Block Diagram

AMCC
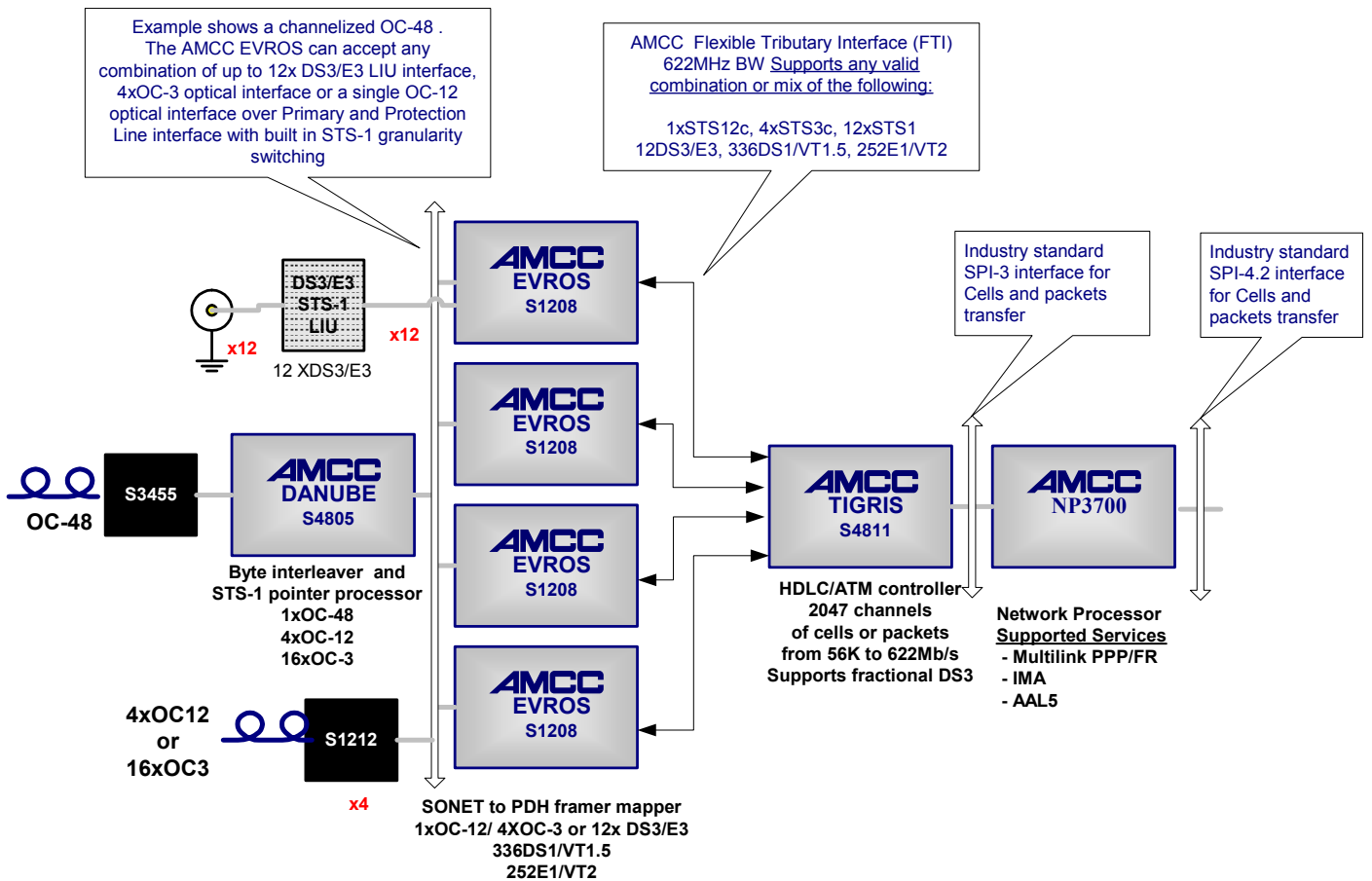APPLIED MICRO CIRCUITS CORPORATION

Applications

• Supports Frame Relay, PPP, HDLC as well as ATM protocols within one device to allow easy software scalable solutions.

• Dense channelization of fiber connections to client tributaries (DS1/E1/J1 and DS3/E3) and termination for data applications in multi-service switches and Aggregation routers.

• Packet Over SONET application.

• ATM mapping into SONET applications.

• Packet and cell based DSLAM equipment.

• Frame Relay switches and multiplexors.

• ATM or SMDS switches, multiplexors, and routers.

• Internet/Intranet termination equipment.

• Frame Relay inter-networking service for ATM switches and multiplexors.

• Multiservice platforms supporting a combination of Frame Relay, Multi Link Frame Relay, Multi Link PPP, IMA, AAL2, AAL3/4 and AAL5 ATM protocols.

Figure 2: OC-48/4xOC-12/16xOC-3/12xDS3/E3 Channelized Data Termination

Example shows a channelized OC-48 . The AMCC EVROS can accept any combination of up to 12x DS3/E3 LIU interface, 4xOC-3 optical interface or a single OC-12 optical interface over Primary and Protection Line interface with built in STS-1 granularity switching

AMCC Flexible Tributary Interface (FTI) 622MHz BW Supports any valid combination or mix of the following:

1xSTS12c, 4xSTS3c, 12xSTS1
12DS3/E3, 336DS1/VT1.5, 252E1/VT2

Industry standard SPI-3 interface for Cells and packets transfer

Industry standard SPI-4.2 interface for Cells and packets transfer

DS3/E3 STS-1 LIU
x12
x12
12 XDS3/E3

AMCC EVROS S1208

OC-48
S3455

AMCC DANUBE S4805

Byte interleaver and STS-1 pointer processor
1xOC-48
4xOC-12
16xOC-3

AMCC EVROS S1208

AMCC EVROS S1208

AMCC TIGRIS S4811

HDLC/ATM controller 2047 channels of cells or packets from 56K to 622Mb/s Supports fractional DS3

AMCC NP3700

Network Processor
Supported Services
- Multilink PPP/FR
- IMA
- AAL5

4xOC12 or 16xOC3
S1212

AMCC EVROS S1208

x4
SONET to PDH framer mapper
1xOC-12/ 4XOC-3 or 12x DS3/E3
336DS1/VT1.5
252E1/VT2

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FUNCTIONAL BLOCKS OVERVIEW

FTI Interface

• Provides a high-speed interconnection between a SONET/SDH physical layer device and a Link layer device, or a SONET/SDH physical layer device and one or more PDH physical layer devices.

• High bandwidth interface, capable of carrying an STS-12 bandwidth carrying 1xSTS-12c, 4xSTS-3c, 12xSTS-1,12xDS3, 12xE3, 336xDS1/VT1.5/TU11 or 252xE1/VT2/TU12 payloads, or any valid mix of the above.

• The Parallel version runs at a 77.76 MHz speed, transferring 8-bits of data on every clock cycle and is compatible with standard Telecom bus.

• The serial version transfers data bits in a 622.08 Mb/s across a LVDS serial link.

• Supports byte floating (byte aligned) tributary bytes aligned to system boundaries.

• Support both asynchronous (DS3/E3/DS1/E1) and synchronous(VT1.5/VT2/TU11/TU12) payloads time division multiplexed into the system frame.

• Support synchronous SONET mappings (STS-1/STS-3c/STS-12c/VT1.5/VT2 synchronous payload envelopes).

SPI-3 Interface

• Industry standard variable length packet interface supporting transmit and receive data transfers at rates independent of the line bit rate.

• Defines both byte-level and packet-level transfer control in the transmit and receive direction.

• Support SPI-3 direct mode transfers.

• Support 52 byte and 56 byte cell formats transferred as packets.

• 25MHz to 104MHz operation supported

HDLC Processor

• 2047 user assignable channels.

• HDLC frame structure is configurable to support POS/PPP, HDLC, and direct map modes of operation.

• Bit/Byte synchronization and byte alignment together with bit/byte stuffing and destuffing.

• RFC1662 standards compliant framing.

• Optional insertion and removal of PPP address and control bytes.

• Optional generation and deletion of 16/32 bit frame check sequence field (FCS).

• Payload transparency processing support in both the receive and the transmit direction.

• Optional pre format ($X^{43}+1$) frame scrambling and post de-format scrambling support on channels 0 to 47.

• Octet Alignment checking.

• Min/Max frame length checking.

• Abort sequence checking.

• 56Kb/s support with Idle bit control.

• Inter-frame fill control.

• Data Inversion control.

• Force bad CRC for diagnostics.

• Optional pass/discard errored frames per RX channel.

• Extensive Per channel statistics that include:
  • Good Frame/Byte counts on both TX and RX.
  • FCS/CRC error counts on RX.
  • Octet alignment error counts on RX.
  • Frame length violations on RX.
  • Received frame aborts counts.
  • RX overrun events count.
  • TX aborts sent count.

ATM Processor

• 2047 user assignable channels.

• Supports direct ATM cell mappings for STS12c, STS3c, STS1c, DS3, DS1, E1, DS0, and NxDS0.

• Supports G.832 ATM cell mapping for E3.

• Supports PLCP ATM cell mapping for DS3.

• Generates TX HEC and allows pass through of HEC when configured for 56B cell mode on SPI-3.

• Optional TX Idle cell insertion.

• Configurable Idle cell format for inserted TX Idle cells.

• Performs RX cell delineation.

• Optional RX HEC checking.

• Optional RX HEC single bit correction.

• Optional payload scrambling using $X^{43}+1$ polynomial.

• Optional RX Idle and/or Unassigned cell removal.

• Configurable Unassigned cell format for RX removal.

• Optional pass/discard error cells per channel in RX.

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• Extensive per channel statistics that include:

  • Good RX cells.
  • Good TX cells.
  • RX loss of cell delineation events.
  • RX HEC errors single bit corrected.
  • RX HEC errors uncorrected.
  • RX PLCP BIP errors.
  • RX PLCP Remote Alarm Detected indicator.
  • RX PLCP OOF indication.

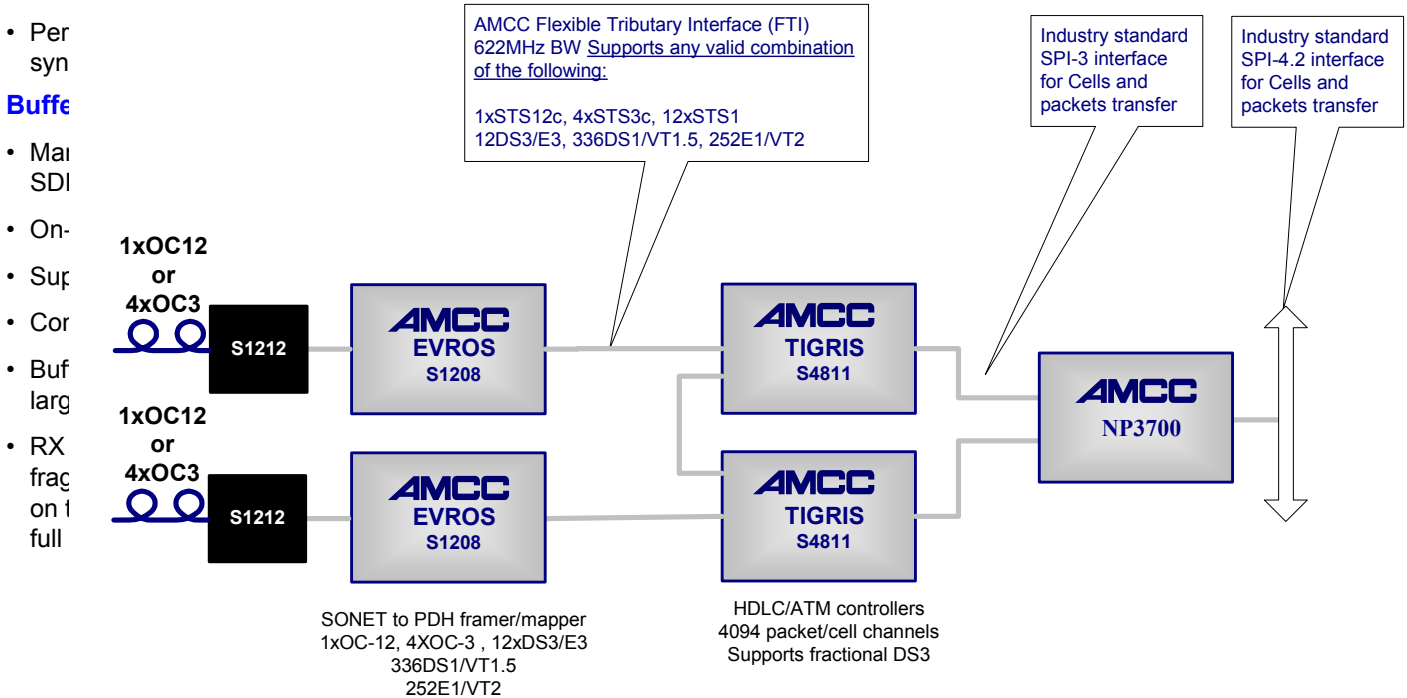• Global count of TX HEC errors received over SPI-3 in 56B mode.

Queue Management

• On chip queue management.

• Multiple RX High/Low priority queues with programmable service priority arbitration.

• Per channel TX High/Low priority queues with programmable watermarks and optional discard at high threshold.

• Full "out of band" access to on chip queue threshold status via a 16 pin Queue Access Bus interface. Useful for monitoring the fill level of TX and RX queues for flow control operation.

• Per
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Buffe

• Mar
  SDI

• On-

• Sup

• Cor

• Buf
  larg

• RX
  frag
  on t
  full

Figure 3: TIGRIS Expansion Mode used for a 2 x OC-12 solution with 4k channels

AMCC Flexible Tributary Interface (FTI) 622MHz BW Supports any valid combination of the following:

1xSTS12c, 4xSTS3c, 12xSTS1 12DS3/E3, 336DS1/VT1.5, 252E1/VT2

Industry standard SPI-3 interface for Cells and packets transfer

Industry standard SPI-4.2 interface for Cells and packets transfer

1xOC12 or 4xOC3

S1212

AMCC EVROS S1208

AMCC TIGRIS S4811

AMCC NP3700

1xOC12 or 4xOC3

S1212

AMCC EVROS S1208

AMCC TIGRIS S4811

SONET to PDH framer/mapper 1xOC-12, 4XOC-3 , 12xDS3/E3 336DS1/VT1.5 252E1/VT2

HDLC/ATM controllers 4094 packet/cell channels Supports fractional DS3

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External Memory Support

• Industry standard DDR333 SDRAM support.

• Separate 64b DRAM memory banks for Transmit and Receive frame storage.

• Supports 256Mb, 512Mb, and 1Gb DRAM technology.

• Supports x16 discrete.

Sub Rate DS3 Support

• Subrate Services supported for all 48 DS3 payloads.

• Interoperates with the following subrate DS3 protocols:

- • Quick Eagle (formerly Digital Link)
- • ADC/Kentrox
- • Larscom
- • Adtran
- • Verilink

Loopbacks

• Wire Level FTI loopback.

• DS0 loopback on FTI interfaces.

• Packet level loopbacks per channel for packets received/ transmitted on FTI, ATI, and SPI interfaces.

• All packet level loopbacks occur at internal queueing points in the on chip MMU (Memory Management Unit).

External CPU Interface

• General purpose 16-bit microprocessor interface for device initialization, control and monitoring. The interface supports both Intel and Motorola type microprocessors.

• Supports processor-based packet/cell injection and retrieval to/from the line interface as well as to/from the system interface.

• Operation up to 66 Mhz.

• Maskable interrupt support for errors and statistics counter threshold events.

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