ULTRA-ACCURATE/HIGH SLEW RATE INVERTING OPERATIONAL AMPLIFIER

739

M.S.KENNEDY CORP.

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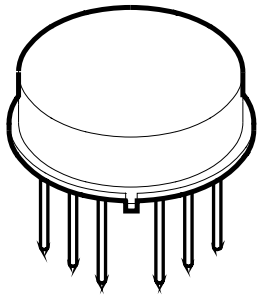
FEATURES:

- Very Fast Setting Time - 10nS to 0.1% Typical
- Very Fast Slew Rate - 5500 V/μS Typical
- Unity Gain Bandwidth - 220 MHz Typical
- Low Noise - 0.15uVrms Typical (f = 0.1Hz to 10Hz)
- Very Accurate (Low Offset) $\pm$75μV Max.
- Pin Compatable with AD9610

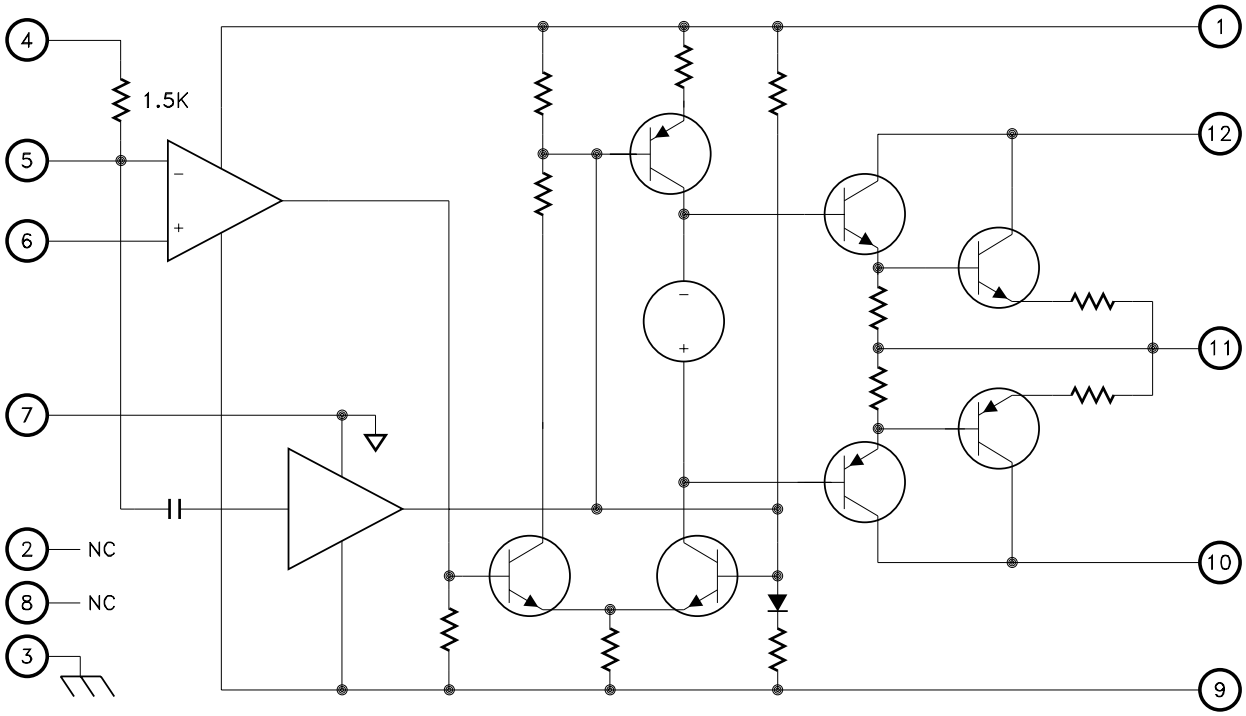
MIL-PRF-38534 QUALIFIED



DESCRIPTION:

The MSK 739 is an inverting composite operational amplifier that combines extremely high bandwidth and slew rate with excellent D.C. accuracy to produce an amplifier perfectly suited for high performance data aquisition and conversion as well as high speed commmunication and line drive. The performance of the MSK 739 is guaranteed over the full military temperature range and for more cost sensitive applications is available in an industrial version. The standard package style is a space efficient 12 pin TO-8. However, alternate package styles are available upon request.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS

- High Performance Data Aquisition
- Coaxial Line Driver
- Data Conversion Circuits
- High Speed Communications
- Ultra High Resolution Video Amplifier

PIN-OUT INFORMATION

1	Positive Power Supply	7	Ground
2	NC	8	NC
3	Case Ground	9	Negative Power Supply
4	Internal Feedback	10	Negative Short Circuit
5	Inverting Input	11	Output
6	Non-Inverting Input	12	Positive Short Circuit

ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	Supply Voltage	T_{ST}	Storage Temperature Range -65°C to +150°C
I_{OUT}	Peak Output Current ±200mA	T_{LD}	Lead Temperature Range 300°C (10 Seconds Soldering)
V_{IN}	Differential Input Voltage ±12V	P_D	Power Dissipation See Curve
R_{TH}	Thermal Resistance 46°C/W Junction to Case Output Devices Only	T_J	Junction Temperature 150°C
		T_C	Case Operating Temperature Range (MSK739B/E) -55°C to +125°C (MSK739) -25°C to +85°C

ELECTRICAL SPECIFICATIONS

±Vcc = ±15V Unless Otherwise Specified

Parameter	Test Conditions	Group A Subgroup	MSK 739B/E Min.	MSK 739B/E Typ.	MSK 739B/E Max.	MSK 739 Min.	MSK 739 Typ.	MSK 739 Max.	Units
STATIC									
Supply Voltage Range ②		-	±12	±15	±18	±12	±15	±18	V
Quiescent Current	Vin = 0V	1	-	±35	±37	-	±37	±40	mA
	Av = -1V/V	2,3	-	±36	±39	-	-	-	mA
Thermal Resistance ②	Output Devices Junction to Case	-	-	45	-	-	48	-	°C/W
INPUT									
Input Offset Voltage	Vin = 0V Av = -100V/V	1	-	±25	±75	-	±50	±100	µV
Input Offset Voltage Drift	Vin = 0V	2,3	-	±0.5	±1.5	-	±0.75	±2.0	µV/°C
Input Bias Current ⑦	Vcm = 0V	1	-	±10	±40	-	±20	±60	nA
	Either Input	2,3	-	±15	±80	-	-	-	nA
Input Offset Current	Vcm = 0V	1	-	5	20	-	10	30	nA
		2,3	-	5	40	-	-	-	nA
Input Impedance ②	F = DC Differential	-	-	5	-	-	5	-	MΩ
Power Supply Rejection Ratio ②	ΔVcc = ±5V	-	-	1	8	-	2	20	µV/V
Input Noise Voltage ②	F = 0.1Hz To 10Hz	-	-	0.15	-	-	0.2	-	µVp-p
Input Noise Voltage Density ②	F = 1KHz	-	-	3.8	-	-	4	-	$nV\sqrt{Hz}$
Input Noise Current Density ②	F = 1KHz	-	-	0.6	-	-	0.7	-	$pA\sqrt{Hz}$
OUTPUT									
Output Voltage Swing	R_L = 100Ω Av = -3V/V F≤10MHz	4	±10	±12.5	-	±10	±12.5	-	V
Output Current	T_J < 150°C	4	±100	±120	-	±100	±120	-	mA
Settling Time ① ②	0.1% 10V step R_L = 1KΩ	-	-	10	35	-	15	45	nS
Full Power Bandwidth	R_L = 100Ω Vo = ±10V	4	20	22	-	15	20	-	MHz
Bandwidth (Small Signal) ②	R_L = 100Ω	-	175	220	-	165	190	-	MHz
TRANSFER CHARACTERISTICS									
Slew Rate	V_{OUT} = ±10V R_L = 1KΩ Av = -1.5V/V	4	4000	5500	-	3500	4000	-	V/µS
Open Loop Voltage Gain ②	R_L = 1KΩ F = 1KHz V_{OUT} = ±10V	4	100	110	-	95	105	-	dB

NOTES:

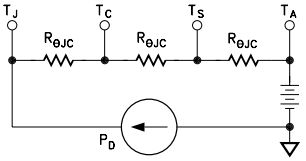
① AV = -1, measured in false summing junction circuit.
② Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only.
③ Industrial grade and "E" suffix devices shall be tested to subgroups 1 and 4 unless otherwise specified.
④ Military grade devices ("B" suffix) shall be 100% tested to subgroups 1,2,3 and 4.
⑤ Subgroups 5 and 6 testing available upon request.
⑥ Subgroup 1,4 $T_A = T_C = +25°C$
Subgroup 2 $T_A = T_C = +125°C$
Subgroup 3 $T_A = T_C = -55°C$
⑦ Measurement taken 0.5 seconds after application of power using automatic test equipment.

APPLICATION NOTES

HEAT SINKING

To determine if a heat sink is necessary for your application and if so, what type, refer to the thermal model and governing equation below.

Thermal Model:



Governing Equation:

$T_J = P_D \times (R_{\theta JC} + R_{\theta CS} + R_{\theta JC}) + T_A$

Where

T_J = Junction Temperature
P_D = Total Power Dissipation
$R_{\theta JC}$ = Junction to Case Thermal Resistance
$R_{\theta CS}$ = Case to Heat Sink Thermal Resistance
$R_{\theta SA}$ = Heat Sink to Ambient Thermal Resistance
T_C = Case Temperature
T_A = Ambient Temperature
T_S = Sink Temperature

Example:

This example demonstrates a worst case analysis for the op-amp output stage. This occurs when the output voltage is 1/2 the power supply voltage. Under this condition, maximum power transfer occurs and the output is under maximum stress.

Conditions:
$V_{CC} = \pm 16$VDC
$V_O = \pm 8$Vp Sine Wave, Freq. = 1KHz
$R_L = 100\Omega$

For a worst case analysis we will treat the +8Vp sine wave as an 8VDC output voltage.

1.) Find Driver Power Dissapation
$P_D = (V_{CC}-V_O)\ (V_O/R_L)$
$= (16V-8V)\ (8V/100\Omega)$
$= 0.64W$
2.) For conservative design, set $T_J = +125°C$
3.) For this example, worst case $T_A = +90°C$
4.) $R_{\theta JC} = 45°C/W$ from MSK 739B Data Sheet
5.) $R_{\theta CS} = 0.15°C/W$ for most thermal greases
6.) Rearrange governing equation to solve for $R_{\theta SA}$

$R_{\theta SA} = ((T_J-T_A)/P_D) - (R_{\theta JC}) - (R_{\theta CS})$
$= ((125°C - 90°C)/0.64W) - 45°C/W - 0.15°C/W$
$= 54.7 - 46.15$
$= 9.5°C/W$

OUTPUT SHORT CIRCUIT PROTECTION

The output section of the MSK 739 can be protected from direct shorts to ground by placing current limit resistors between pins 1 and 12 and pins 9 and 10 as shown in Figure 1.

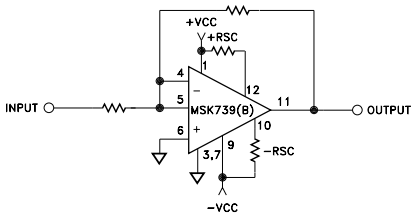


FIGURE 1

The value of the short circuit current limit resistors ($\pm R_{SC}$) can be calculated as follows.

$+R_{SC} = V_{CC}-0.7/+I_{SC}$ $\qquad$ $-R_{SC} = V_{CC}+0.7/-I_{SC}$

Short circuit current limit should be set at least 2X above the highest normal operating output current to keep the value of RSC low enough to ensure that the voltage dropped accross the short circuit current limit resistor doesn't adversely affect normal operation.

INTERNAL FEEDBACK RESISTOR

The MSK 739 is equipped with an internal 1.5KΩ feedback resistor. Bandwidth and slew rate can be optimized by connecting the MSK 739 as shown in Figure 2. Placing the feedback resistor inside the hybrid reduces printed circuit board trace length and its' asscociated capacitance which acts as a capacitive load to the op-amp output. Reducing the capacitive load allows the output to slew faster and greater bandwidths will be realized. Refer to Table 1 for recommended RIN values for various gains.

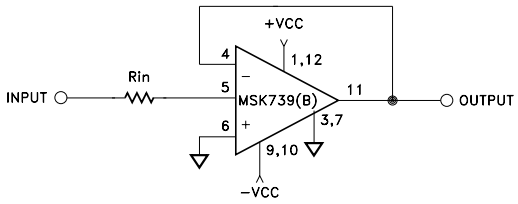


FIGURE 2

TABLE 1

APPROXIMATE DESIRED GAIN	RIN VALUE
-1	1.5KΩ
-2	750Ω
-10	150Ω

Whenever the internal resistor is not being used it is good practice to short pin 4 and 5 to avoid inadvertently picking up spurious signals.

Recommended External Component Selection Guide Using External Rf

TABLE 2

	APPROXIMATE DESIRED GAIN	RI(+)	RI(-)	Rf(Ext)	Cf
①	-1	249Ω	499Ω	499Ω	②
①	-2	160Ω	249Ω	499Ω	②
①	-5	169Ω	200Ω	1KΩ	②
①	-8	100Ω	124Ω	1KΩ	②
①	-10	90.9Ω	100Ω	1KΩ	②
①	-20	100Ω	100Ω	2KΩ	②

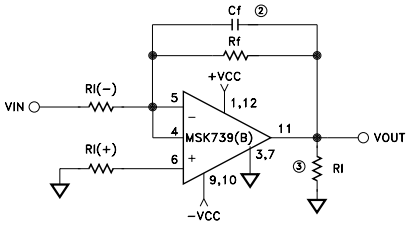


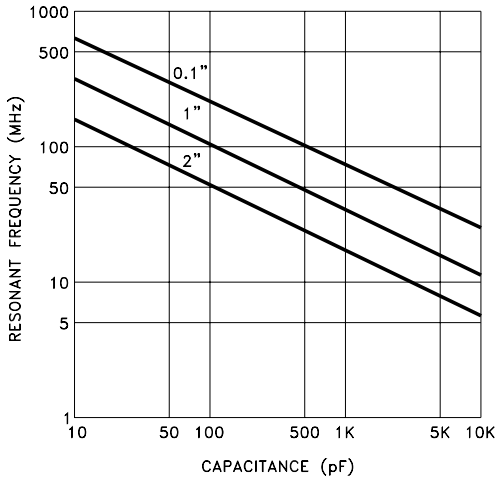
FIGURE 3

① The positive input resistor is selected to minimize any bias current induced offset voltage.
② The feedback capacitor will help compensate for stray input capacitance. The value of this capacitor can be dependent on individual applications. A 0.5 to 5pF capacitor is usually optimum for most applications.
③ Effective load is RL in parallel with Rf.

APPLICATION NOTES CON'T

STABILITY AND LAYOUT CONSIDERATIONS

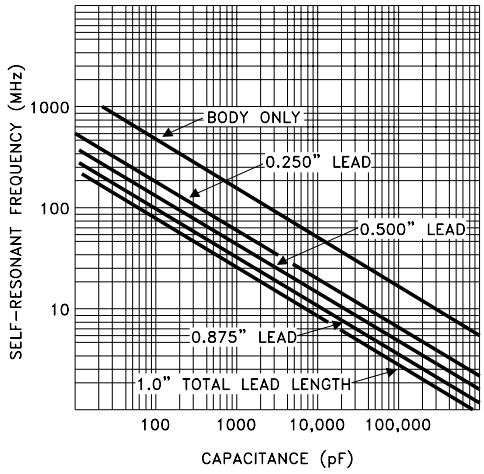
As with all wideband devices, proper decoupling of the power lines is extremely important. The power supplies should be by-passed as near to pins 9 and 1 as possible with a parallel grouping of a 0.01μf ceramic disc and a 4.7μf tantalum capacitor. Wideband devices are also sensitive to printed cicuit board layout. Be sure to keep all runs as short as possible, especially those associated with the summing junction and power lines. Circuit traces should be surrounded by ground planes whenever possible to reduce unwanted resistance and inductance. The curve below shows the relationship between resonant frequency and capacitor value for 3 trace lengths.



FEEDBACK CAPACITANCE

Feedback capacitance is commonly used to compensate for the "input capacitance" effects of amplifiers. Overshoot and ringing, especially with capacitive loads, can be reduced or eliminated with the proper value of feedback capacitance.

All capacitors have a self-resonant frequency. As capacitance increases, self-resonant frequency decreases (assuming all other factors remain the same). Longer lead lengths and PC traces are other factors that tend to decrease the self-resonant frequency. When a feedback capacitor's self-resonant frequency falls within the frequency band for which the amplifier under consideration has gain, oscillation occurs. These influences place a practical upper limit on the value of feedback capacitance that can be used. This value is typically 0.5 to 5pF for the MSK 739(B).



OPTIMIZING SLEW RATE

When measuring the slew rate of the MSK 739, many external factors must be taken into consideration to achieve best results. The closed loop gain of the test fixture should be -1.5V/V or less with the external feedback resistor being 499Ω Lead length on this resistor must be as short as possible and the resistor should be small. No short circuit current limit resistors should be used. (Short pin 1 to pin 12 and pin 9 to pin 10). Pins 2,3,7 and 8 should all be shorted directly to ground for optimum response. Since the internal feedback resistor isn't being used, pin 4 should be shorted to pin 5. SMA connectors are recomended for the input and output connectors to keep external capacitances to a minimum. To compensate for input capacitance, a small 0.5 to 5pF high frequency variable capacitor should be connected in parallel with the feedback resistor. This capacitor will be adjusted to trim overshoot to a minimum. A 5500V/μS slew rate limit from -10V to +10V translates to a transition time of 2.9 nanoseconds. In order to obtain a transition time of that magnitude at the output of the test fixture, the transition time of the input must be much smaller. A rise time at the input of 500 picoseconds or less is sufficient. If the transition time of the input is greater than 500 picoseconds, the following formula should be used, since the input transition time is now affecting the measured system transition time.

$$T_A = \sqrt{T_B^2 + T_C^2}$$

WHERE:

T_A = Transition time measured at output jack on MSK 739 test card.
T_B = Transition time measured at input jack on MSK 739 test card.
T_C = Actual output transition time of MSK 739(note that this quantity will be calculated, not measured directly with the oscilloscope).

THE MSK 739 IS INVERTING, THEREFORE WHEN MEASURING RISING EDGE SLEW RATE:

T_A = Rise time measured at output
T_B = Fall time measured at input
T_C = Actual rise time of output

WHEN MEASURING FALLING EDGE SLEW RATE:

T_A = Fall time measured at output
T_B = Rise time measured at input
T_C = Actual fall time of output

LOAD CONSIDERATIONS

When determining the load an amplifier will see, the capacitive portion must be taken into consideration. For an amplifier that slews at 1000V/μS, each pF will require 1mA of output current.
To minimize ringing with highly capacitive loads, reduce the load time constant by adding shunt resistance.

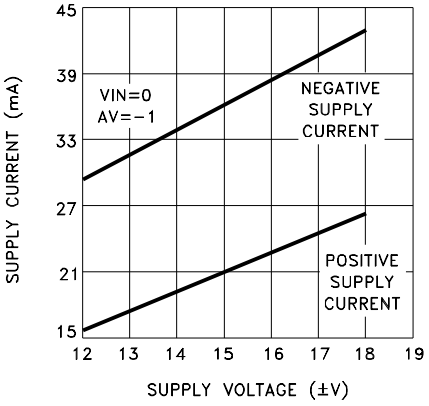
$$I = C(dV/dT)$$

CASE CONNECTION

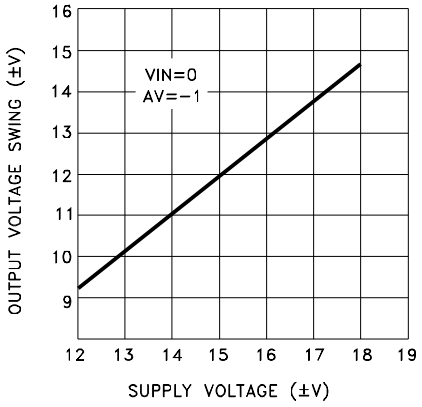
The MSK 739(B) has pin 3 internally connected to the case. The case is not electrically connected to the internal circuit. Pin 3 should be tied to a ground plane for sheilding. For special applications, consult factory.

TYPICAL PERFORMANCE CURVES

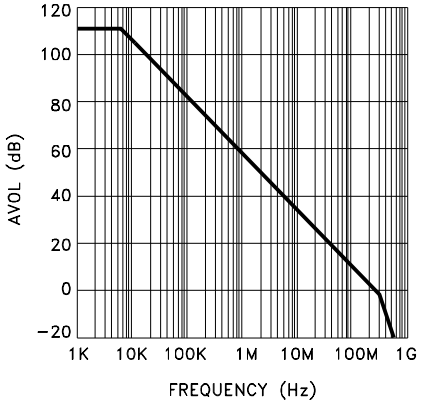
SUPPLY CURRENT vs. SUPPLY VOLTAGE



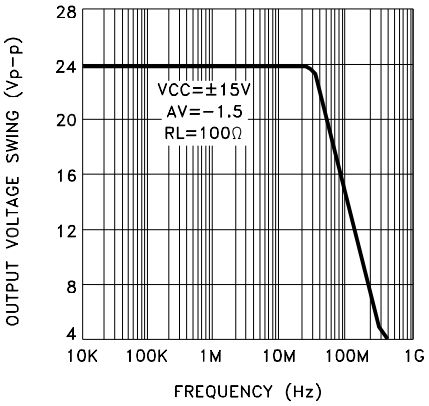
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE



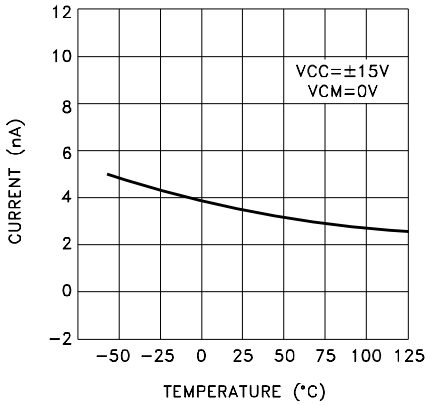
OPEN LOOP VOLTAGE GAIN vs. FREQUENCY



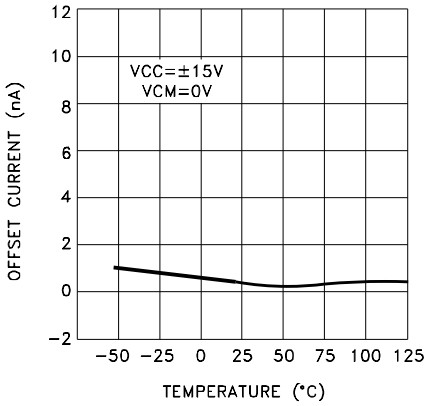
OUTPUT VOLTAGE SWING vs. FREQUENCY



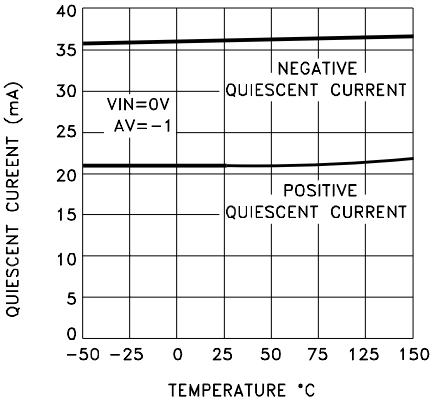
INPUT BIAS CURRENT vs. TEMPERATURE



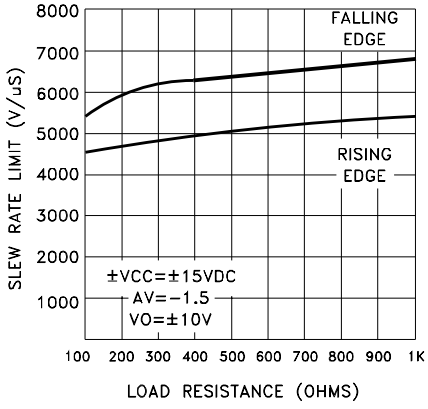
INPUT OFFSET CURRENT vs. TEMPERATURE



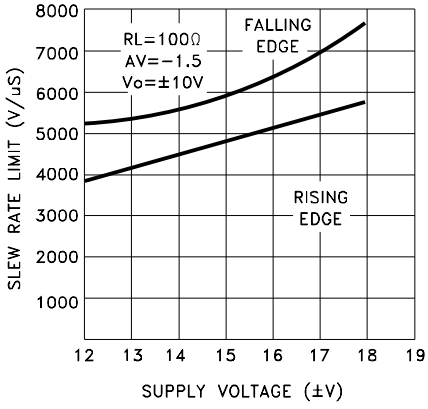
QUIESCENT CURRENT vs. TEMPERATURE



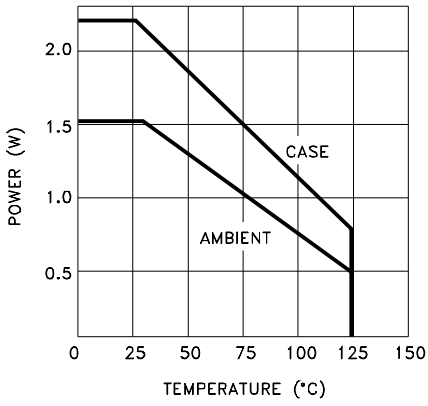
SLEW RATE LIMIT vs. LOAD RESISTANCE



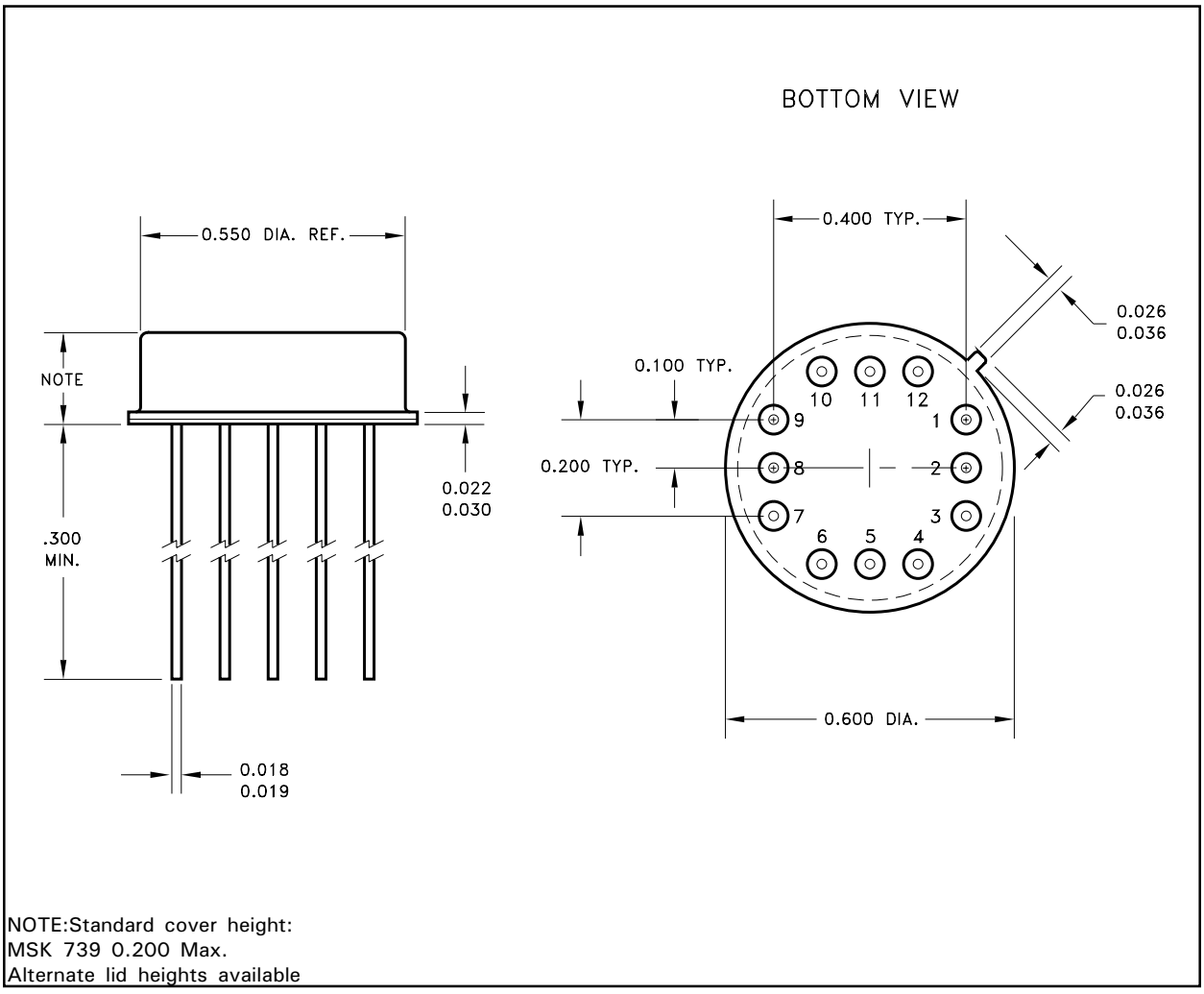
SLEW RATE LIMIT vs. SUPPLY VOLTAGE



POWER DISSIPATION vs. TEMPERATURE (TO−8)



MECHANICAL SPECIFICATIONS



NOTE: ALL DIMENSIONS ARE ±0.010 INCHES UNLESS OTHERWISE LABELED.

ORDERING INFORMATION

MSK739 B

SCREENING

BLANK = INDUSTRIAL; B = MIL-PRF-38534 CLASS H
E = EXTENDED RELIABILITY

GENERAL PART NUMBER

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